User's Guide

ADC364xEVM Evaluation Module

Abstract

This user's guide describes the characteristics, operation, and use of the ADC364x evaluation module (EVM). This user's guide discusses how to set up and configure the software and hardware, and reviews various aspects of the program operation. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the ADC364xEVM. In the following sections of this document, the ADC364x evaluation board is referred to as the EVM and the ADC364x device is referred to as the ADC device.

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1 Introduction

The ADC364xEVM is an evaluation board used to evaluate the ADC364x analog-to-digital converter (ADC) from Texas Instruments. The ADC364xEVM is a dual-channel, 14-bit ADC that can operate up to 125 Mega-samples per second (MSPS). The ADC364x uses a parallel or serial CMOS interface to output the digital data. The serialized CMOS interface supports output rates to 250 Mbps which translates to ~ 30 MSPS (2-wire) to ~ 10 MSPS (0.5-wire) output rates after complex decimation. Hence the ADC3643 can be operated in 'oversampling + decimating' mode using the internal decimation filter in order to improve the dynamic range and relax external anti-aliasing filter.

The ADC364xEVM is equipped with the following features:

- Transformer and FDA coupled analog inputs
- CDCE6214 clocking solution for on-board clocking
- Transformer coupled or single-ended clock inputs
- INA226 current shunt monitors for evaluating power consumption
- Power over mini-USB
- FMC connector

2 Equipment

This hardware setup procedure is written with the intent to use the onboard CDC clocking option, and therefore only requires an analog input for evaluation. Using an external sampling clock(s) is an option, and instructions are provided toward the end of this document.

2.1 Evaluation Board Feature Identification Summary

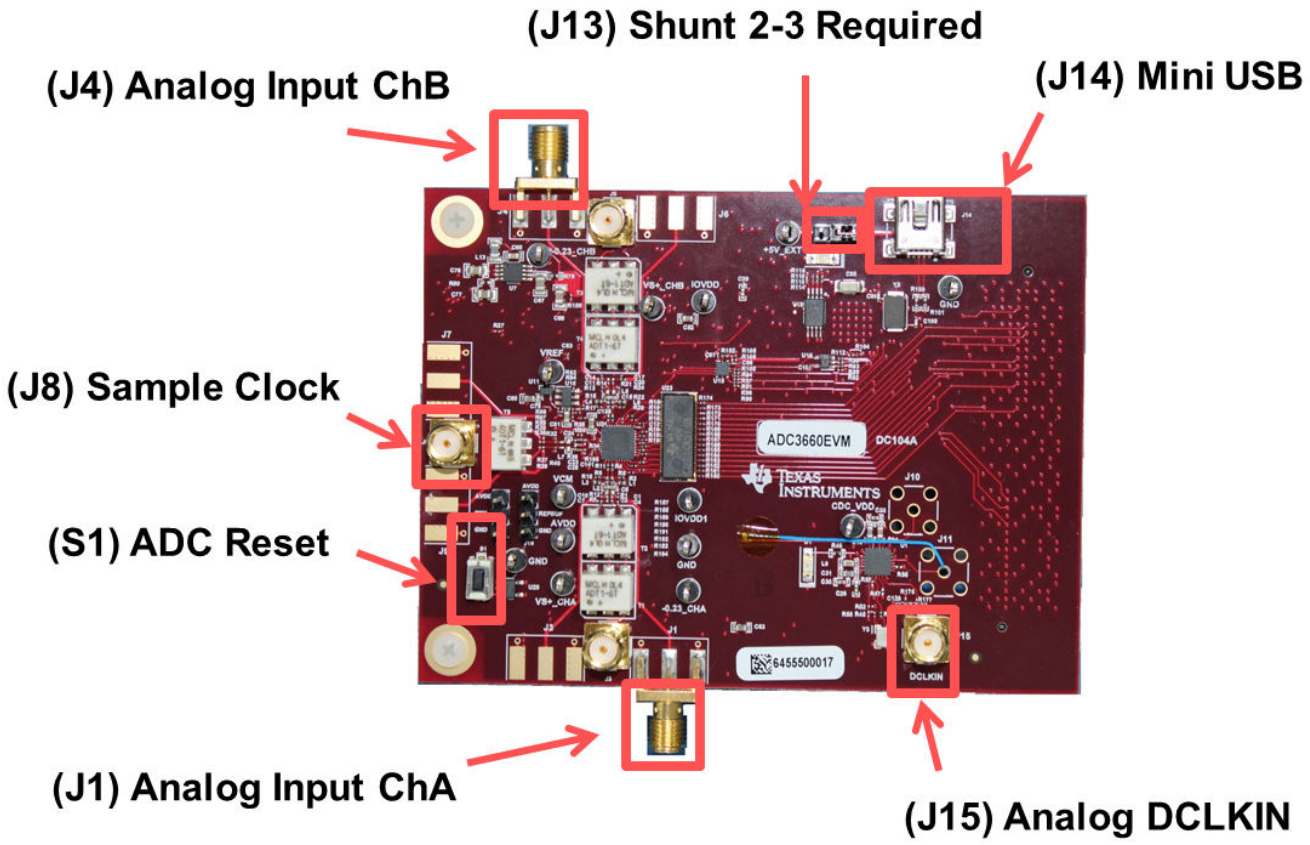

Figure 2-1. ADC364xEVM Feature Identification

Ensure that jumper J8 is shunted in the 2-3 position. This allows 5 V to be supplied to the ADC364xEVM through the mini-USB connector.

If an external 5-V supply is desired, J8 must be shunted in the 1-2 position, and the external 5 V can be connected to the test point labeled "+5 EXT".

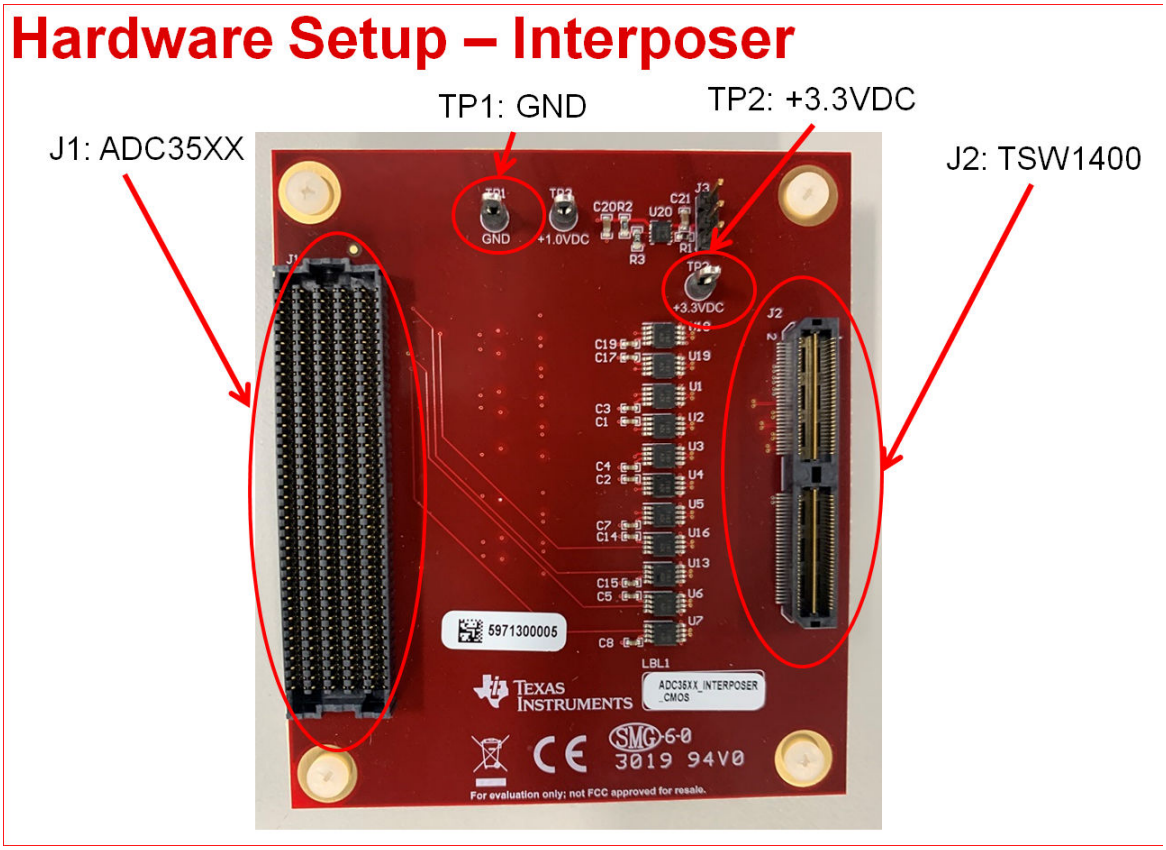

Figure 2-2. CMOS FPGA Interposer Card

2.2 Required Equipment

- The following equipment is included in the EVM evaluation kit:
  - ADC364x Evaluation board (EVM)
  - CMOS FPGA Interposer Card
  - Power supply clips for Interposer Card
  - Mini-USB cable

The following equipment is **not** included in the EVM evaluation kit, but is required for evaluation of this EVM:

- TSW1400EVM data capture board and related items
- HSDC Pro software
- PC running Microsoft® Windows® 7, or 10
- One low-noise signal generators for the analog input (If using external clock option, additional signal generator is required).

TI recommends the following generators:

- Rohde & Schwarz SMA100A
- Rohde & Schwarz SMA100B

Bandpass filter for the analog input signal. The following recommended bandpass filter will have:

- Bandpass filter, greater than or equal to 60-dB harmonic attenuation, less than or equal to 5% bandwidth, greater than 18-dBm power, less than 5-dB insertion loss
- Signal-path cables, SMA

3 Setup Procedure

This Setup Procedure will detail how to setup the software GUIs and EVM hardware required for evaluation using the onboard clock (CDCE6214).

3.1 Install High-Speed Data Converter (HSDC) Pro Software

Download the most recent version of the HSDC Pro software. Launch the executable, and accept the default installation options.

Download and install the HSDC Pro Patch. This patch copies all the INI files required to the HSDC pro directory.

3.2 Install ADC35XXEVM GUI 1.0 Software

Download the ADC35XXEVM GUI 1.0 software from the EVM tool folder at ADC3643EVM.

Extract and run the executable file, and accept the default installation options.

3.3 Connect the ADC EVM and TSW1400EVM

Connect the ADC364xEVM FMC connector to J1 of the FPGA Interposer Card.

Connect J2 of the FPGA Interposer Card to J1 of the TSW1400EVM.

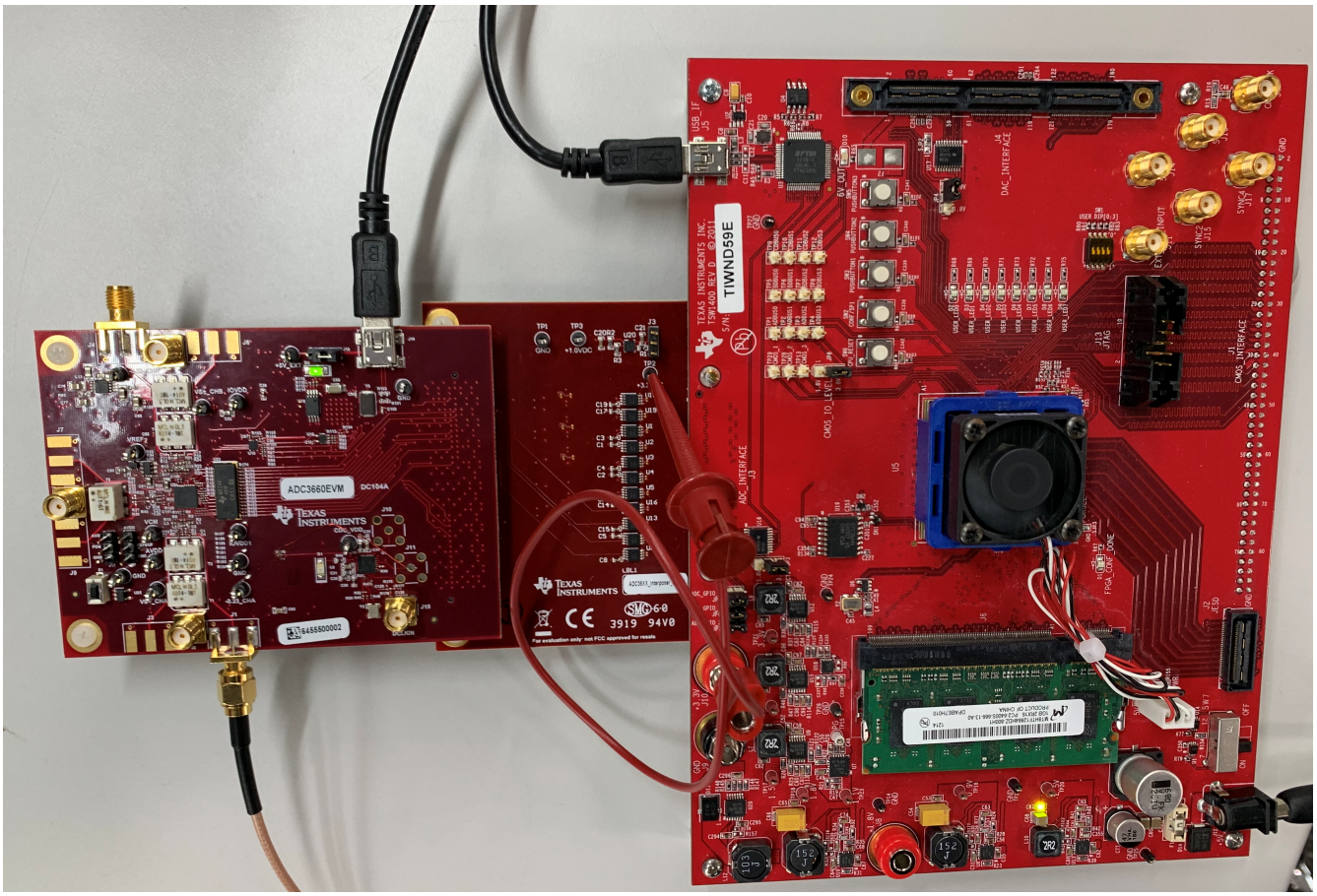

Figure 3-1. ADC3660EVM Full Setup

3.4 Connect the Power Supply and Mini-USB Connections

Use the following steps to connect the power supply and mini-USB connections:

1. Connect 3.3 VDC to TP2 of the FPGA Interposer card. Provide power supply ground to TP1, as required. J10 of the TSW1400EVM can be used to source this +3.3 VDC.
2. Connect the power cable to the TSW1400EVM at 5-V (minimum 3 A) power supply. Place the power switch (SW7) to the "On" position.
3. Connect the mini-USB cable to the TSW1400EVM (J2).
4. Connect the mini-USB cable to the ADC3643EVM (J14).

4 Device Configuration

A hardware reset should be performed before programming the ADC by toggling the push button switch S1.

A software reset may be performed at any time to reset the ADC registers to their default state.

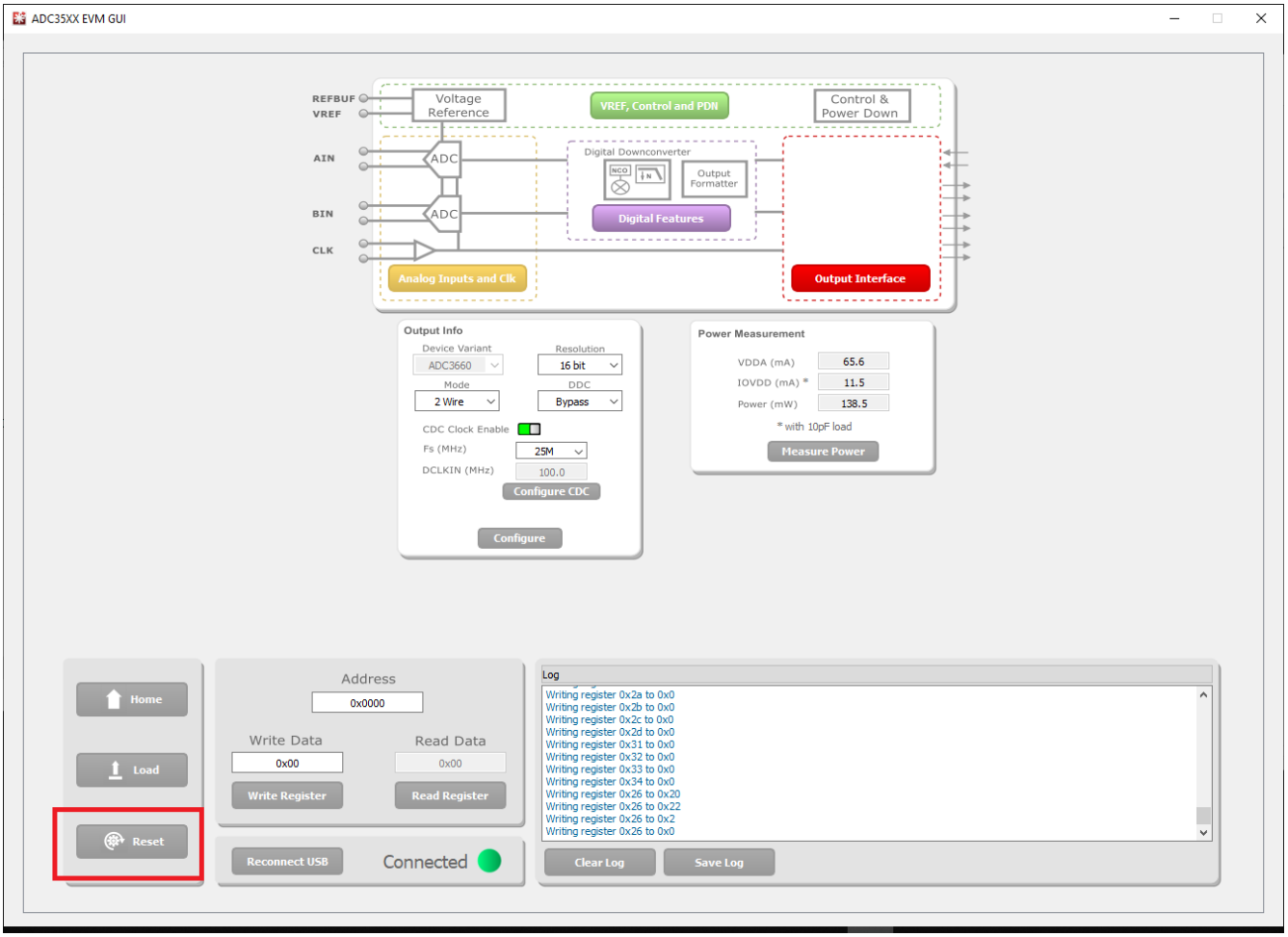

Figure 4-1. ADC35xx Software Reset

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4.1 Bypass Mode

The following steps show how to configure the ADC3643EVM in Bypass mode.

4.1.1 ADC35XX GUI: Bypass Mode (DDR) Configuration

By default, the ADC3643EVM is preconfigured for 14bit, DDR mode. When using this mode, the only required step in the ADC35XX GUI is to configure the onboard clock in order to select the desired sampling rate (10MHz, 25 MHz or 65 MHz).

Note: The following steps also apply to the ADC3642EVM and ADC3644EVM. However, the on board clocking device limits the ADC3642EVM to 25 MHz and 10 MHz clock frequencies, and the ADC3644EVM is limited to 125 MHz and 65 MHz. If different sampling frequencies are required, please connect an external clock source.

After launching the ADC35xx GUI perform the following steps:

- Under Resolution, select "14 bit".
- Select "65M" for Fs (sample clock).
- Ensure that "CDC Enable" is green (enabled).
- Click "Configure CDC" button.
- Click "Configure" button.

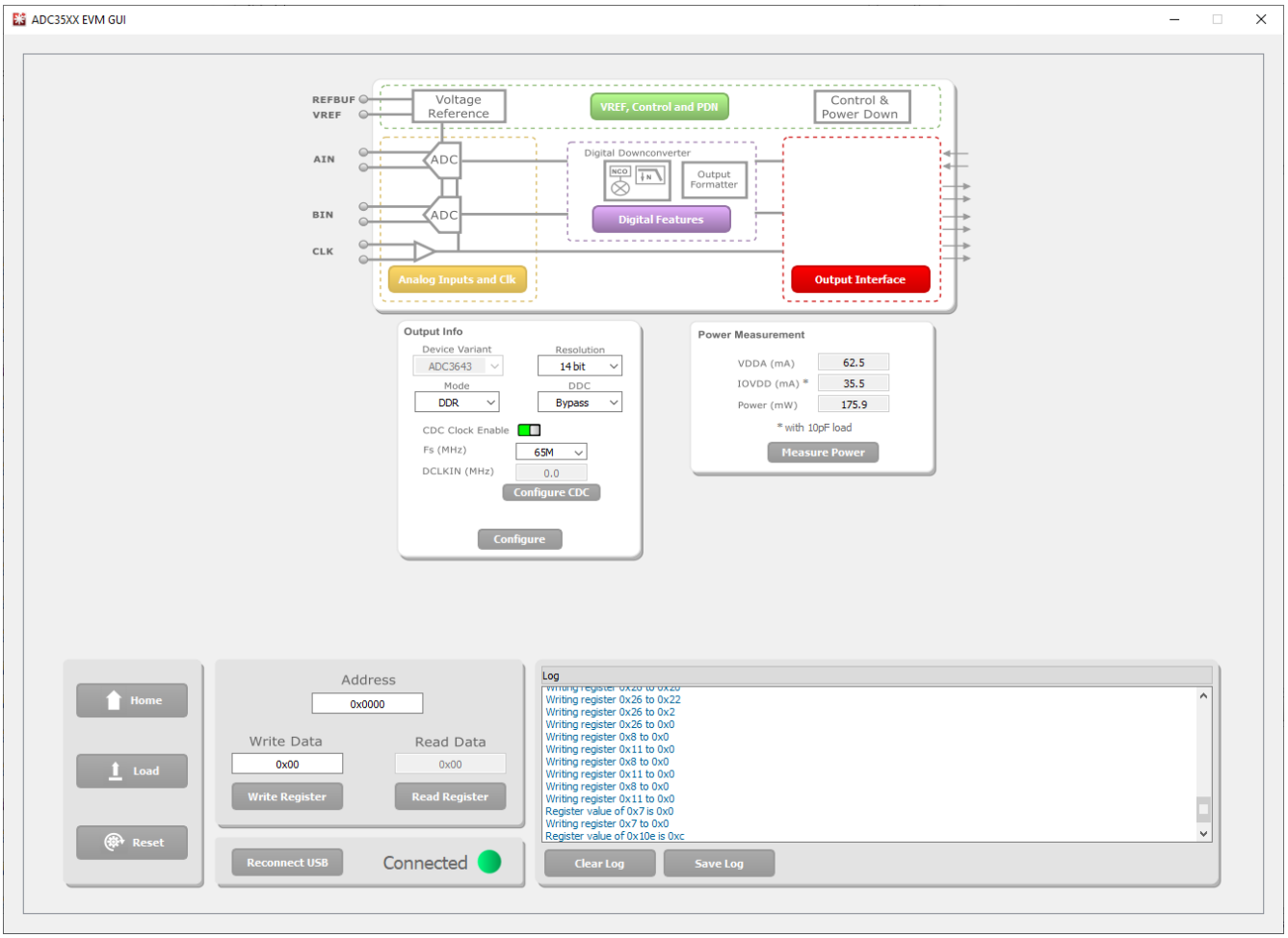

Figure 4-2. ADC35xx GUI settings for Bypass Mode

4.1.2 HSDC Pro: Bypass Mode

After pressing "Configure" within the ADC35xx GUI perform the following steps to setup HSDC pro:

- Launch HSDC Pro
- Select the TSW1400 and click OK

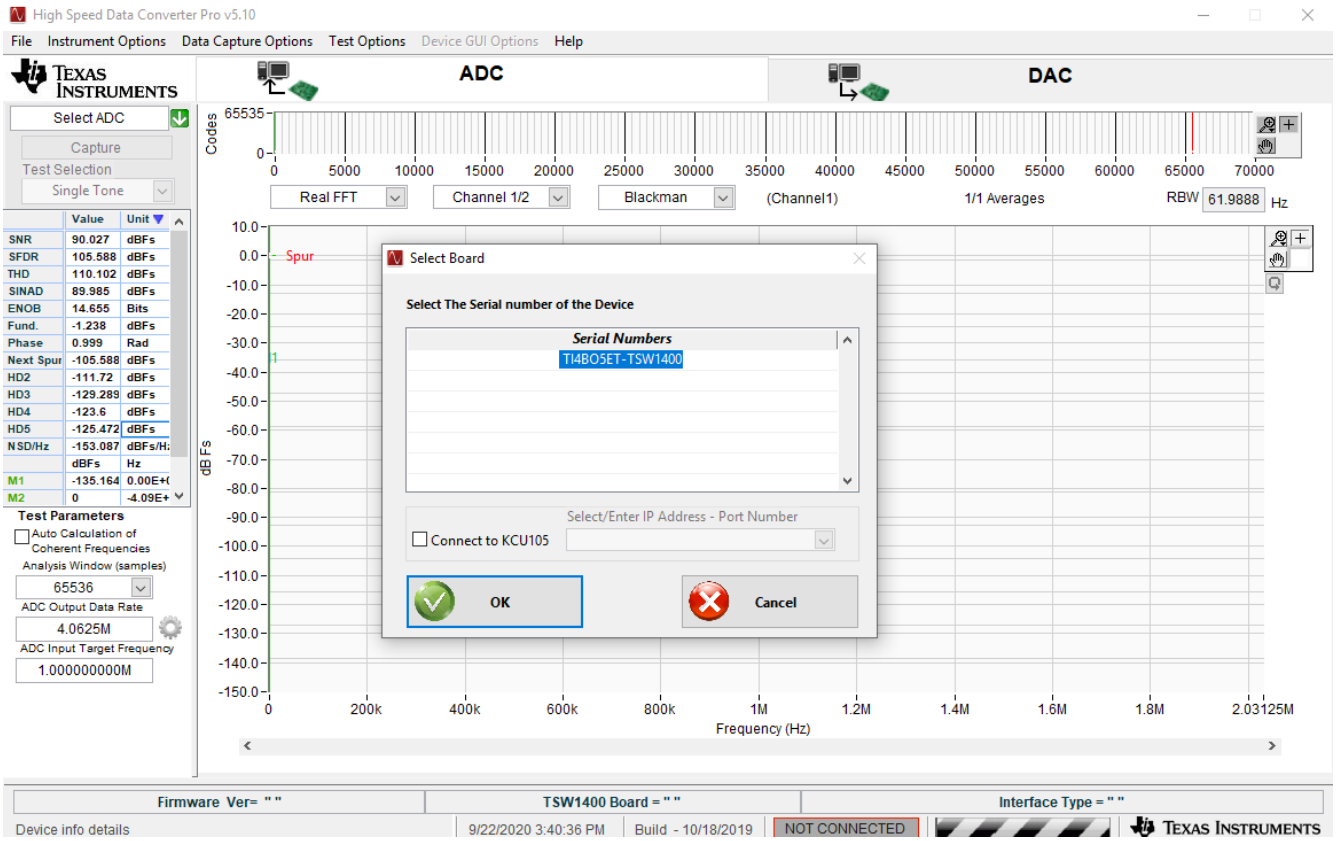

Figure 4-3. HSDC Pro: Connect to TSW1400

- Click OK for the no firmware loaded prompt.

- Select “ADC3643_7W_14bit_DDR" to load firmware, and click Yes.

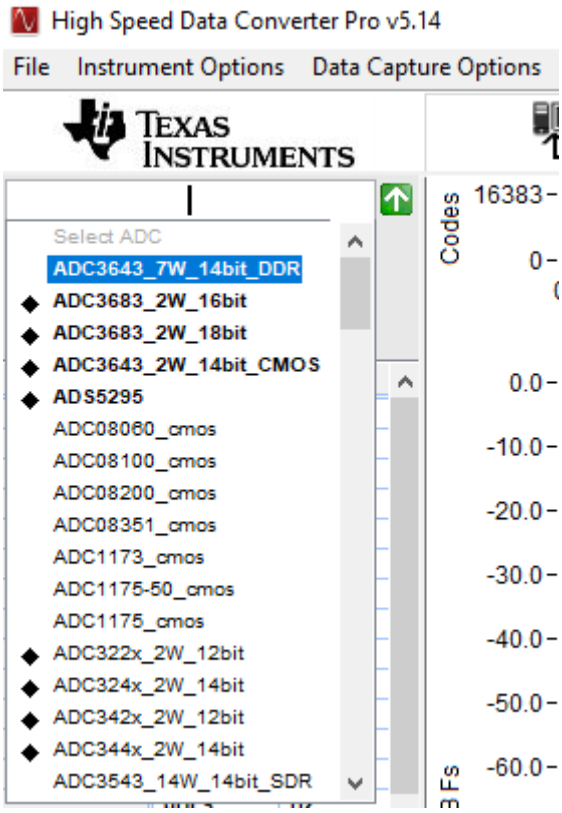

Figure 4-4. HSDC Pro ini file selection for Bypass Mode

- Enter 65M within the box that says “ADC Output Data Rate”
- Enter the input frequency of the input signal in the box that says "ADC Input Target Frequency" (5 MHz used in this example).

- Press Capture

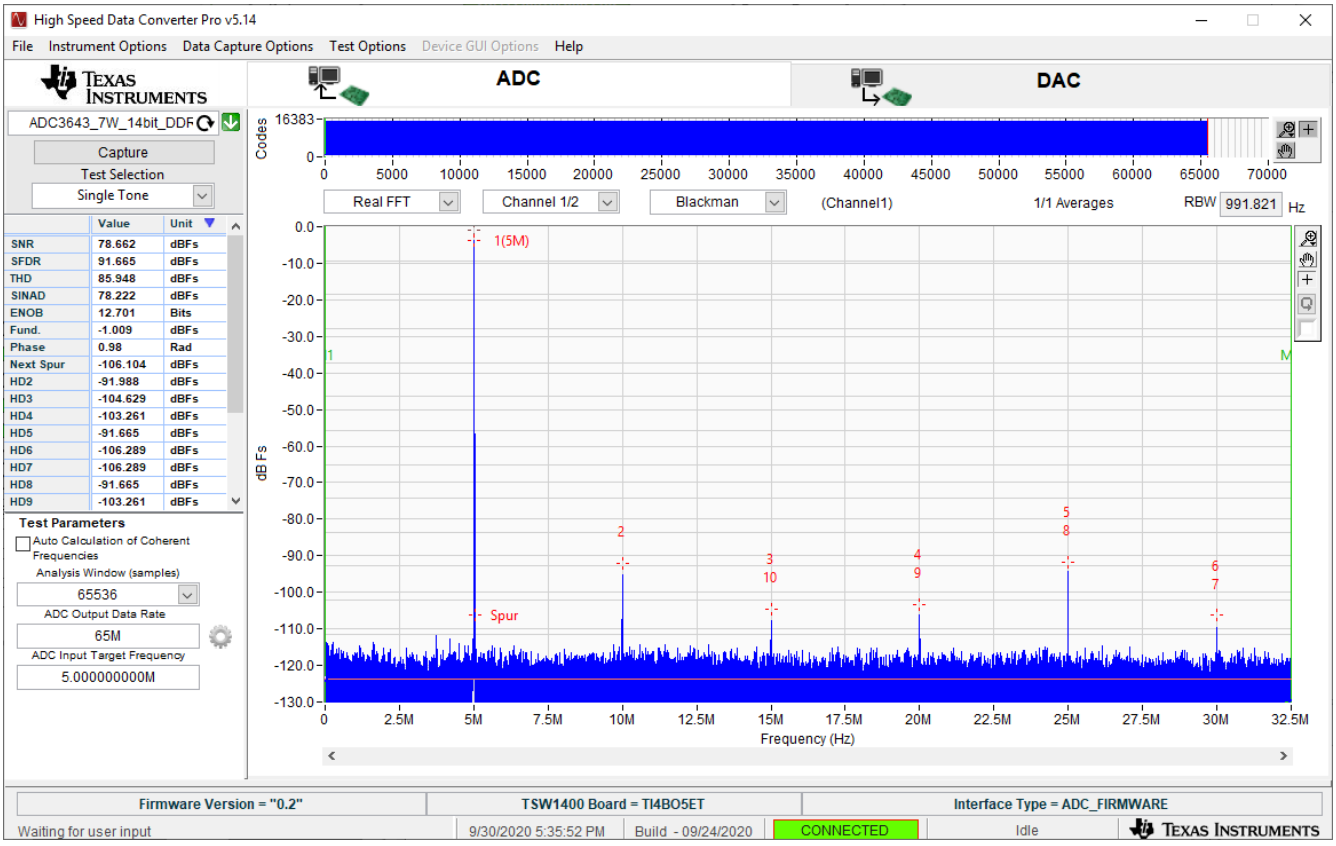

Figure 4-5. Bypass Mode Capture

- The analog input signal power may need to be adjusted to reach -1 dBFS.

4.2 Real Decimation Mode

The following software configuration steps will program the ADC364xEVM in Real Decimation mode.

4.2.1 ADC35XX GUI: Real Decimation Mode Configuration

After launching the ADC35xx GUI perform the following steps:

- Under Resolution, select 16 bit.
- Under DDC, Select Real.
- For Decimation Factor, select 16.
- For Fs(MHz), select 60M.
- Click Configure CDC
- Click Configure

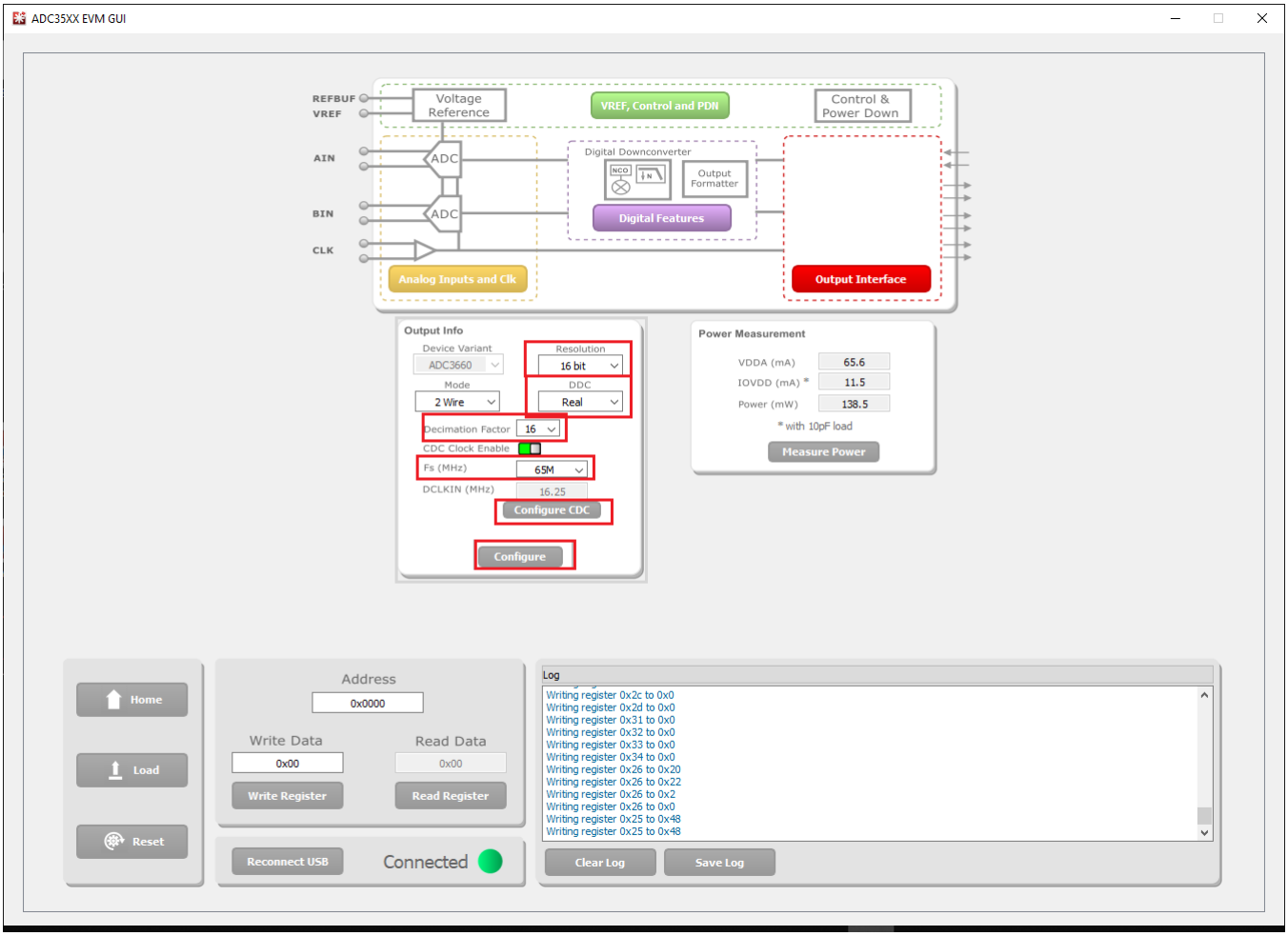

Figure 4-6. ADC35xx GUI settings for Real Decimation Mode

4.2.2 HSDC Pro: Real Decimation Mode

After pressing "Configure" within the ADC35xx GUI perform the following steps to setup HSDC pro:

- Launch HSDC Pro
- Select the TSW1400 and click OK
- Click OK for the no firmware loaded prompt.
- Select “ADC3643_2W_14bit_CMOS” to load firmware, and click Yes.

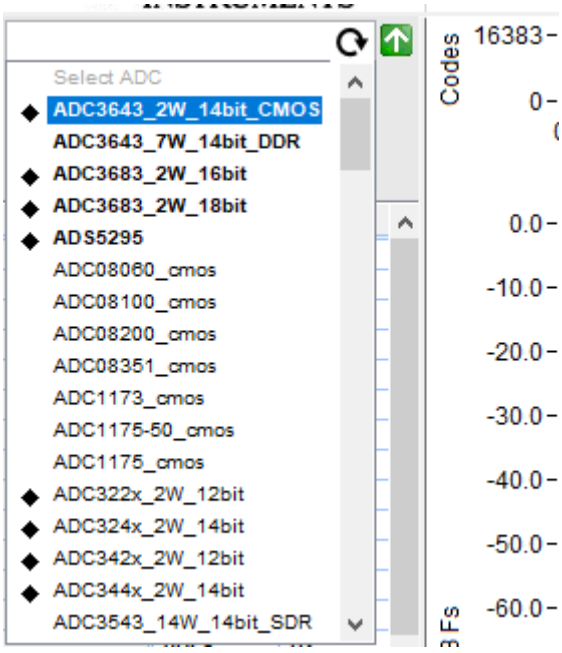

Figure 4-7. Real Decimation HSDC Pro INI File

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Click on the cog next to “ADC Output Data Rate”.

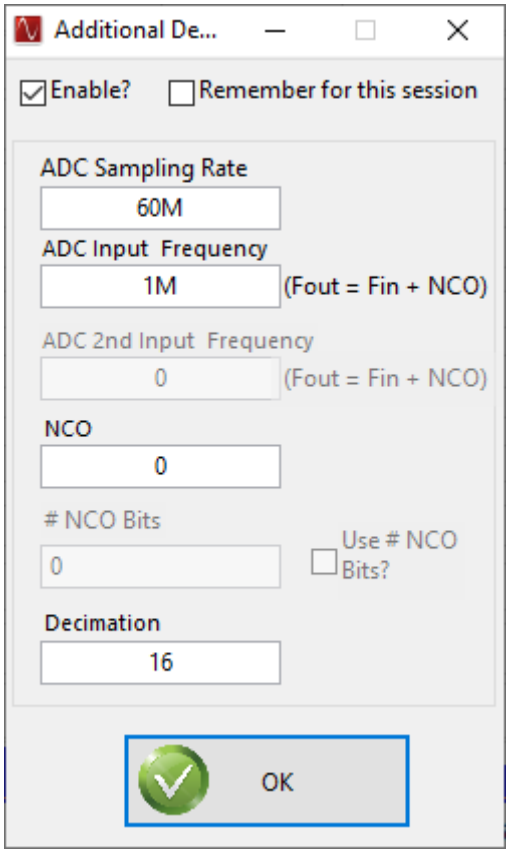

Figure 4-8. Real Decimation Mode HSDC Pro Parameters

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In the new dialogue box, enter 60M in “ADC Sampling Rate”

- Enter 1M in “ADC Input Frequency”
- Enter 16 in “Decimation”.
- Click Ok.
- Click the Capture button

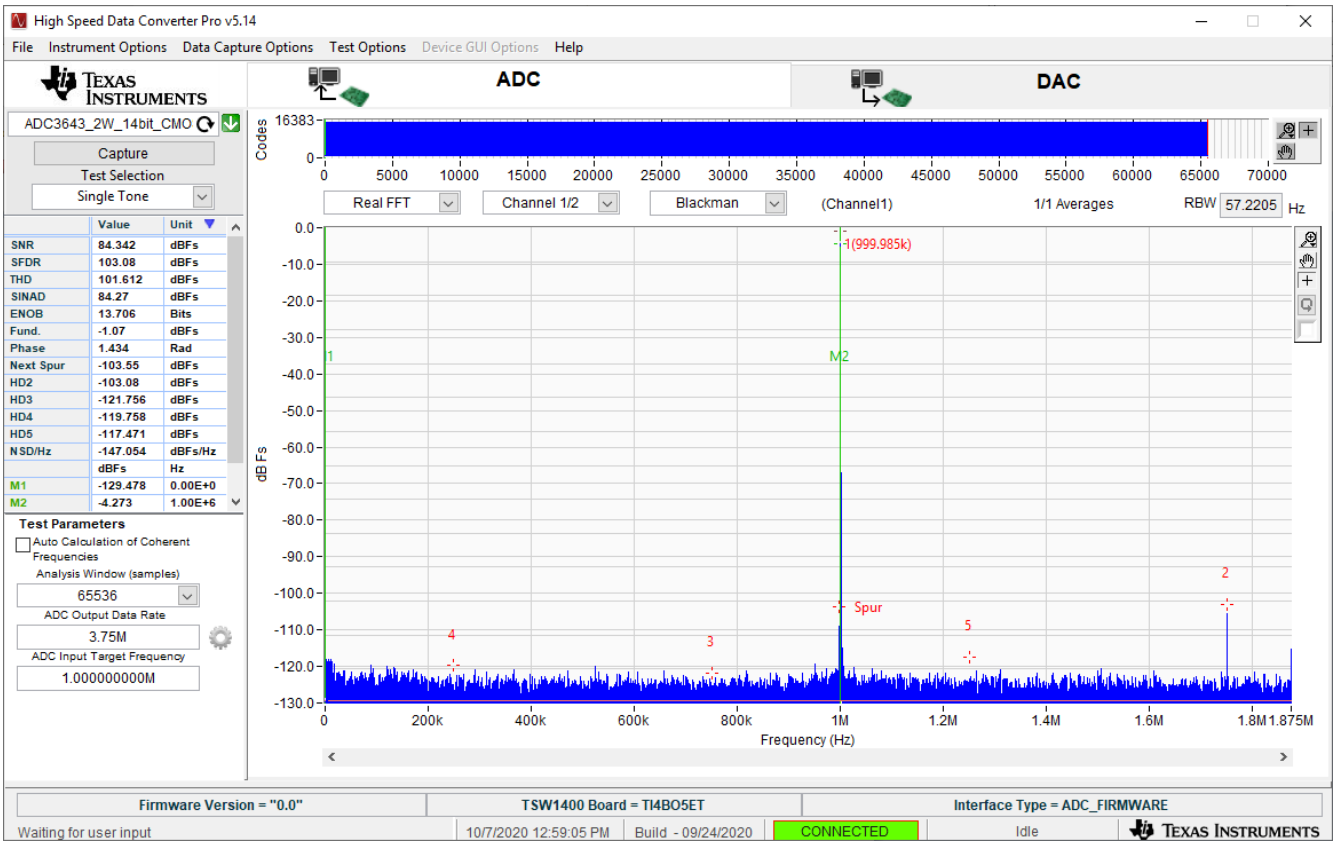

Figure 4-9. HSDC Pro Cog Wheel

4.3 Complex Decimation Mode

The following software configuration steps will program the ADC364xEVM in Complex Decimation mode (16x) with a 10 MHz analog input and 9.9 MHz NCO.

4.3.1 ADC35XX GUI: Complex Decimation Configuration

After launching the ADC35xxEVM GUI perform the following steps:

- Under Resolution, select 14 bit.
- Under DDC, Select Complex.
- For Decimation Factor, select 16.
- For Fs(MHz), select 60M.
- Under "FNCO A (MHz)", enter "9.9" in the field. This field will then calculate to the nearest valid NCO value, and will auto-calculate the correct register values in the field next to it.
- Click Configure CDC

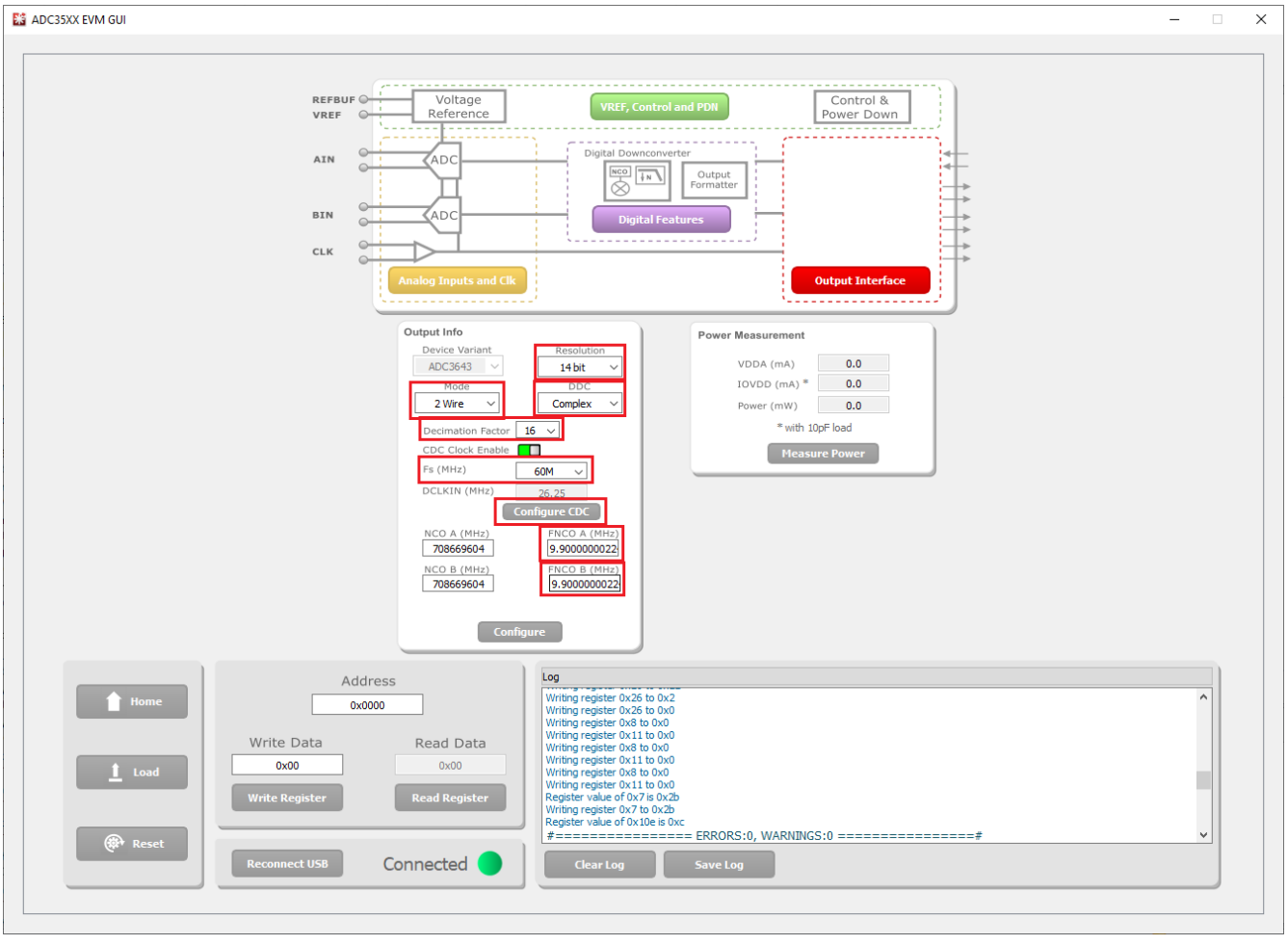

Figure 4-10. ADC35xx GUI settings for Complex Decimation Mode

4.3.2 HSDC PRO: Complex Decimation Mode

After pressing "Configure" within the ADC35xx GUI perform the following steps to setup HSDC pro:

- Launch HSDC Pro.
- Select the TSW1400 and click "OK".
- Click OK for the "no firmware loaded" prompt.
- Select “ADC3643_2W_14bit_CMOS_Complex” to load firmware, and click Yes.

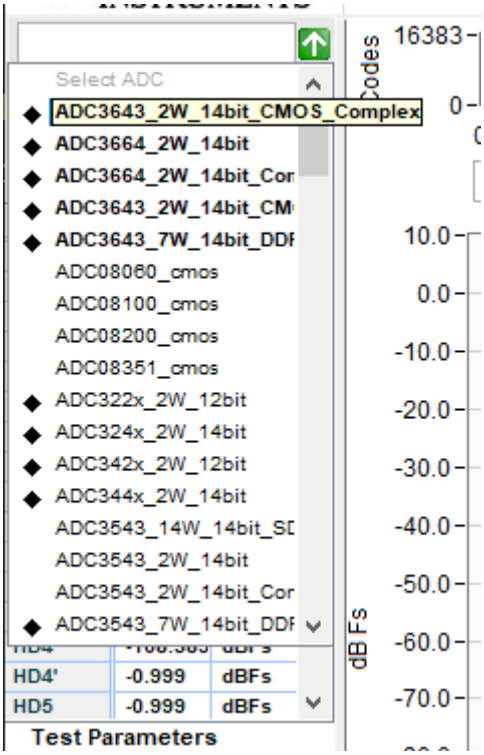

Figure 4-11. Complex Decimation HSDC Pro INI file

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Click on the cog next to “ADC Output Data Rate”.

- In the new dialogue box, check the "Enable?" box.
- Under “ADC Sampling Rate”, enter "60M"
- Under “ADC Input Frequency”, enter "10M"
- Under "NCO", enter "9.9M"
- Under “Decimation”, enter "16".
- Click "OK".

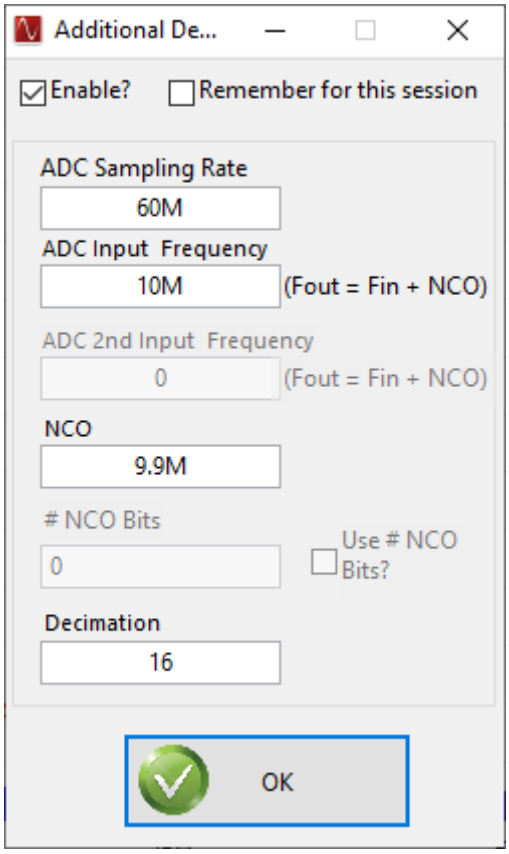

Figure 4-12. Complex Decimation Mode HSDC Pro Parameters

- Select "Complex FFT"

- Press "Capture"

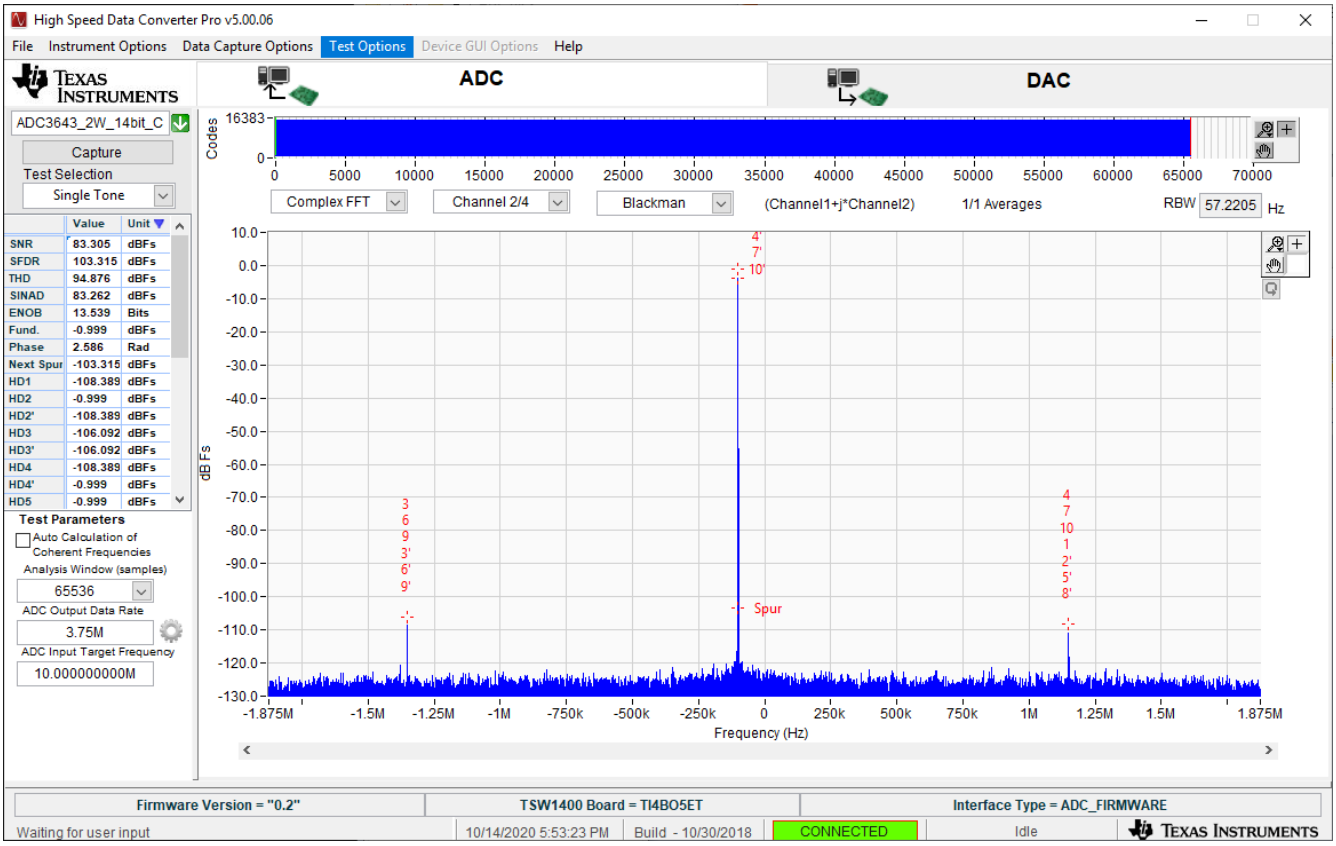

Figure 4-13. Complex Mode Capture

5 External Clocking Hardware Setup

The onboard CDC is useful for general evaluation and relieves the user requirment of needing additional signal generators. The following section shows how to configure and program the ADC364xEVM for external clock operation for Real Decimation Mode. This mode requires two external clock sources (must be frequency locked). If Bypass Mode or Complex Decimation Mode are to be used with an external clock source(s), use the steps outlined with the onboard clock for Bypass Mode and Complex Decimation mode for guidance on how the ADC35xx GUI should be configured (with the exception of using external clocks).

5.1 Hardware Modfications

The following hardware modifications must be made in order to operate the ADC364xEVM using an external sample and (if required) data clock .

External Sample Clock Modification:

- DNI R32, R40
- Install R36, R37 (0-Ω resistor)
- Connect sample clock to J8. Connect DCLKIN to J15.

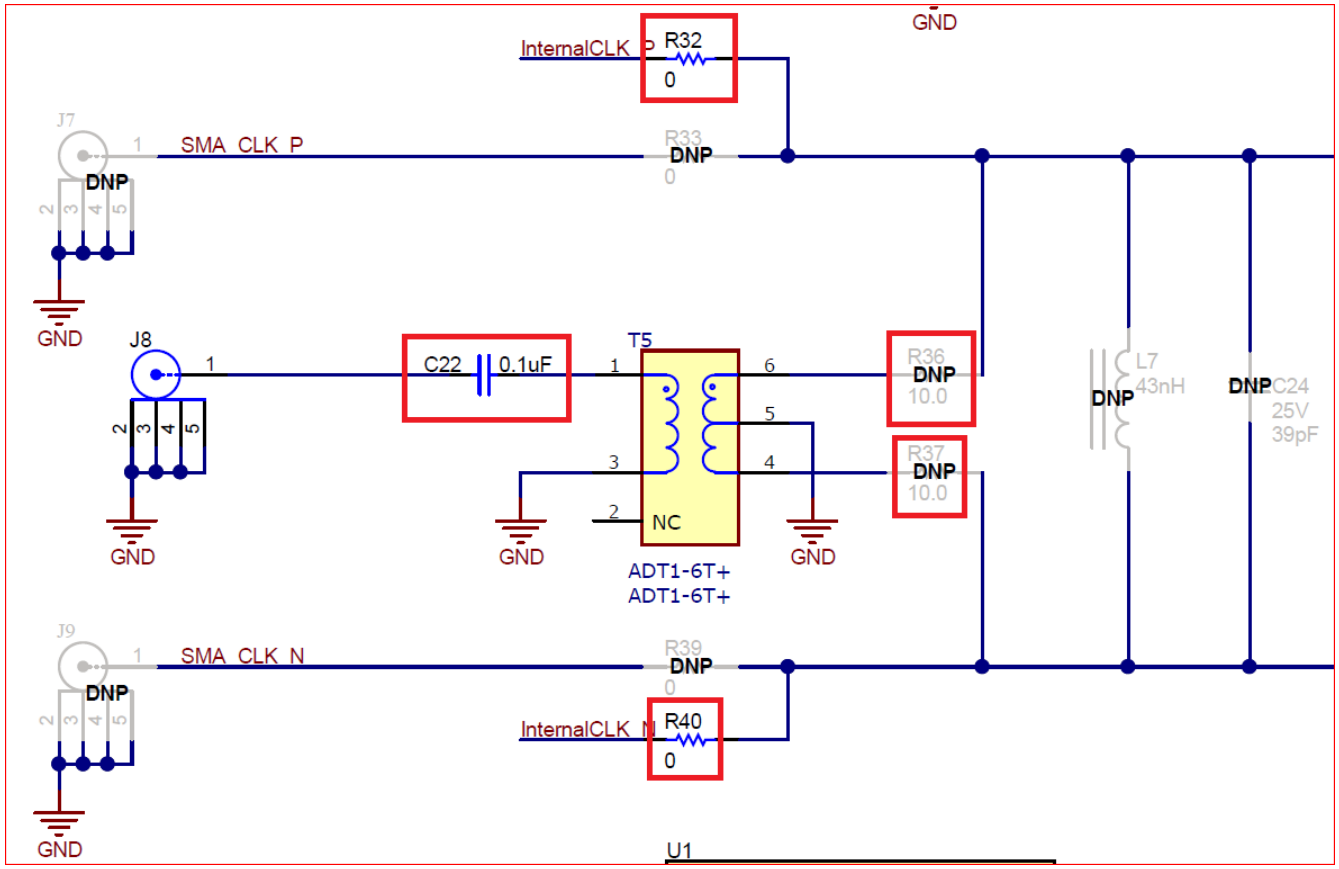

Figure 5-1. ADC364xEVM Schematic Snippet: Sample Clock

External DCLKIN Modification:

- DNI R176

- Replace C129 with 0-Ω resistor.

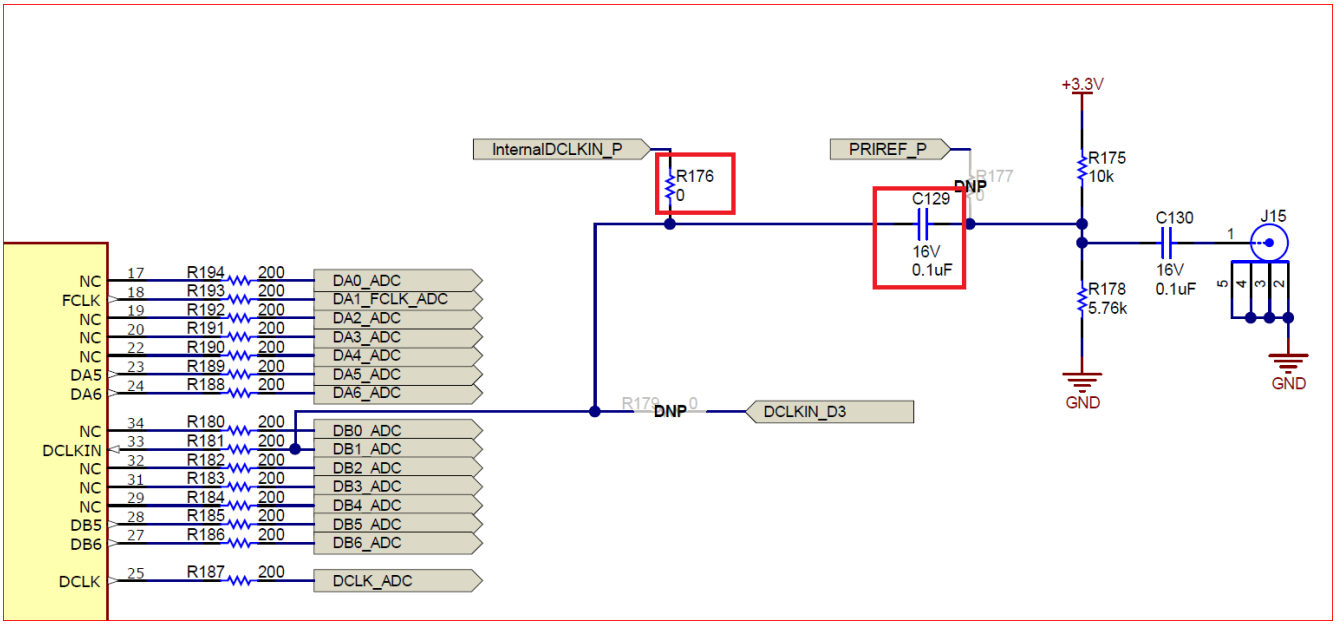

Figure 5-2. ADC364xEVM Schematic Snippet: DCKLIN

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5.2 Hardware Setup: Real Decimation 16x Mode

- Connect ADC sampling clock source (SMA100A used) to J8. Set signal power to +15 dBm. 65 MSPS used in this example.
- Connect DCLKIN clock source (SMA100A used) to J10. Set signal power to +13 dBm. 14.21875 MHz used in this example

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ADC sampling clock source and DCLKIN source must be frequency locked. If this is not performed, the captured data will appear scrambled.

- If not already done, complete the remaining steps outlined in the section Setup Procedure.

5.3 External Clock: ADC35XX GUI Real Decimation Mode

To program the ADC364xEVM follow the steps written in the previous section titled "ADC35xx GUI: Real Decimation Configuration". The only difference that must be observed in the GUI is "CDC Clock Enable" button must be disabled (red) before selecting "Configure" in the ADC35xx GUI.

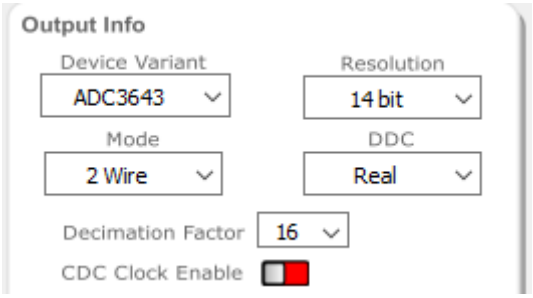

Figure 5-3. ADC35XX GUI: Disable CDC Clock Enable

6 ADC364xEVM Power Monitor

The ADC364xEVM is equipped with on-board current shunt monitors that are able to measure the current consumption on the +1.8VD C rails (AVDD and IOVDD). The user has the ability to read the ADC364xEVM's power consumption on the front page of the ADC35XX GUI. Click the "Measure Power" button to refresh the current values. This feature is useful for determining what mode/sampling speed offers the best power consumption for your application needs.

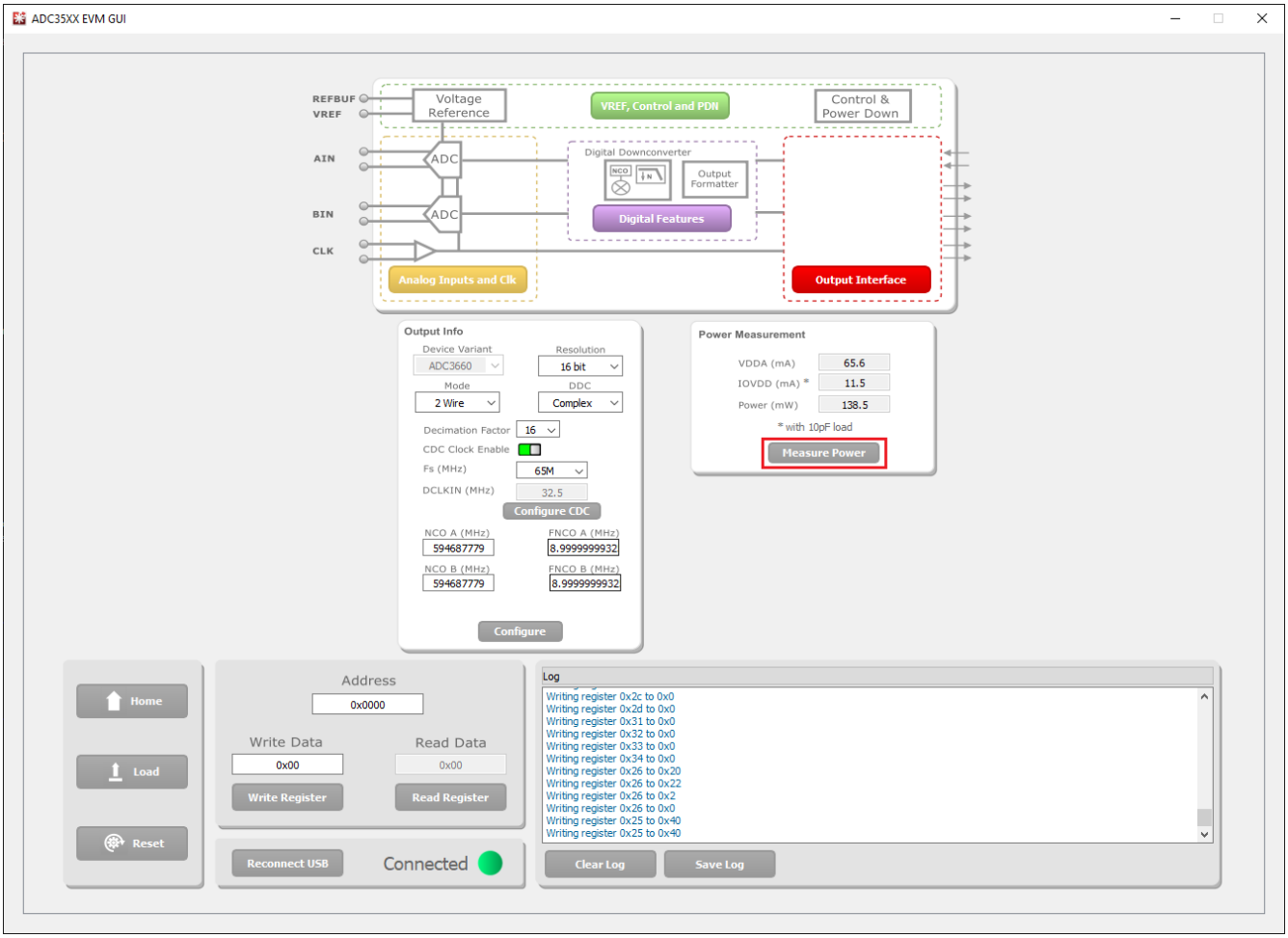

Figure 6-1. ADC364xEVM Power Meter

7 Test Pattern

It is often useful to utilize test patterns to help verify the correct reciept of digital data at the microcontroller or FPGA. A ramp pattern can be enabled by following these steps:

- Click the yellow button "Analog Inputs and Clk"
- Next to "Test Pattern CHA", click the drop down menu, and select "RAMP CUSTOM". This can be done for "Test Pattern CHB" as well.
- In the field next to "Custom Pattern", enter the number "16".
- The digital ramp pattern is now enabled on the ADC. The output of the ADC is now a 14 bit, incrementing ramp pattern.

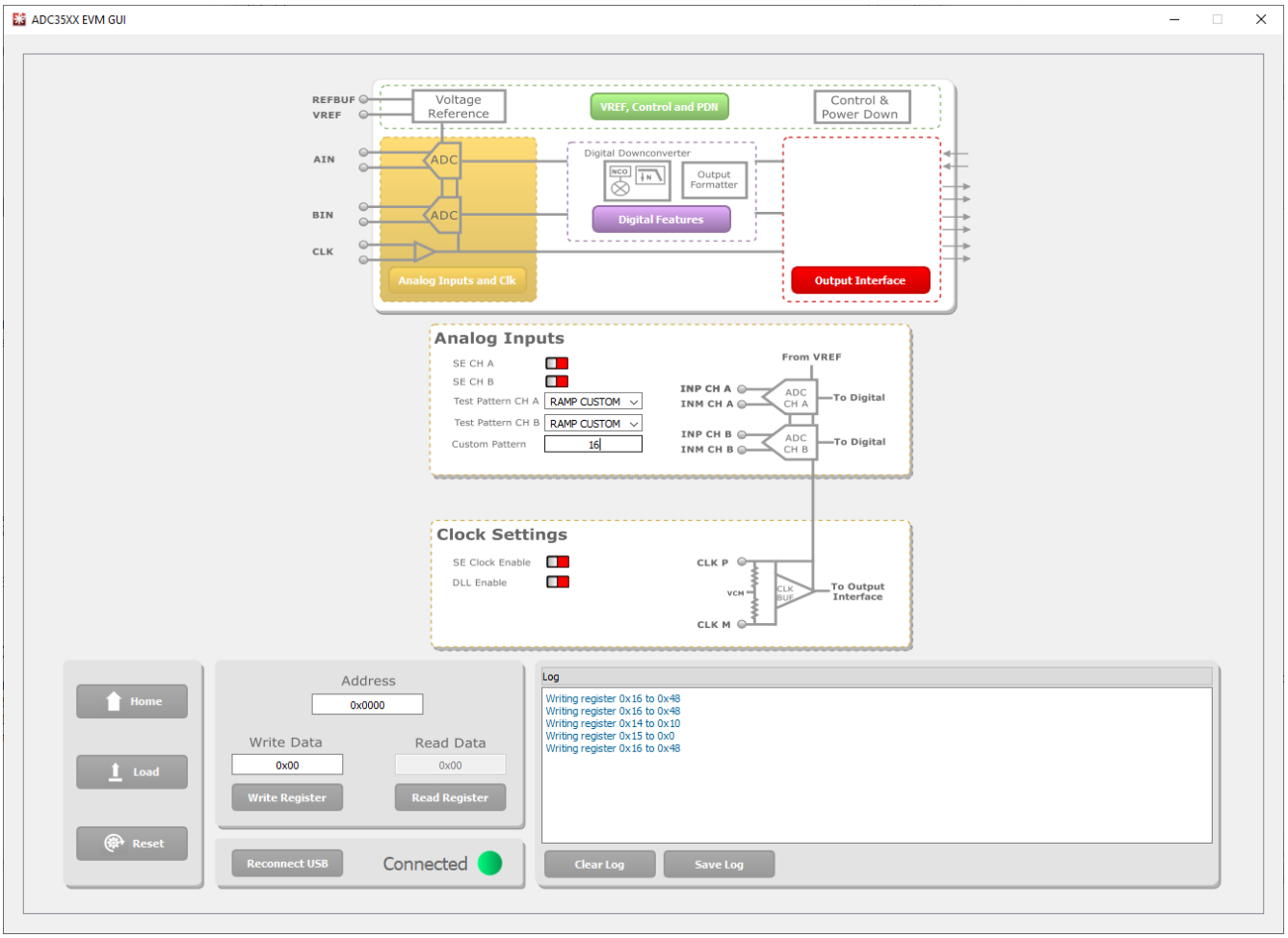

Figure 7-1. ADC35XXEVM GUI 1.0 Ramp Pattern

- In HSDC Pro, the ramp pattern can now be seen when data is captured. These same steps apply to any data output mode (Bypass, Real Decimation and Complex Decimation).

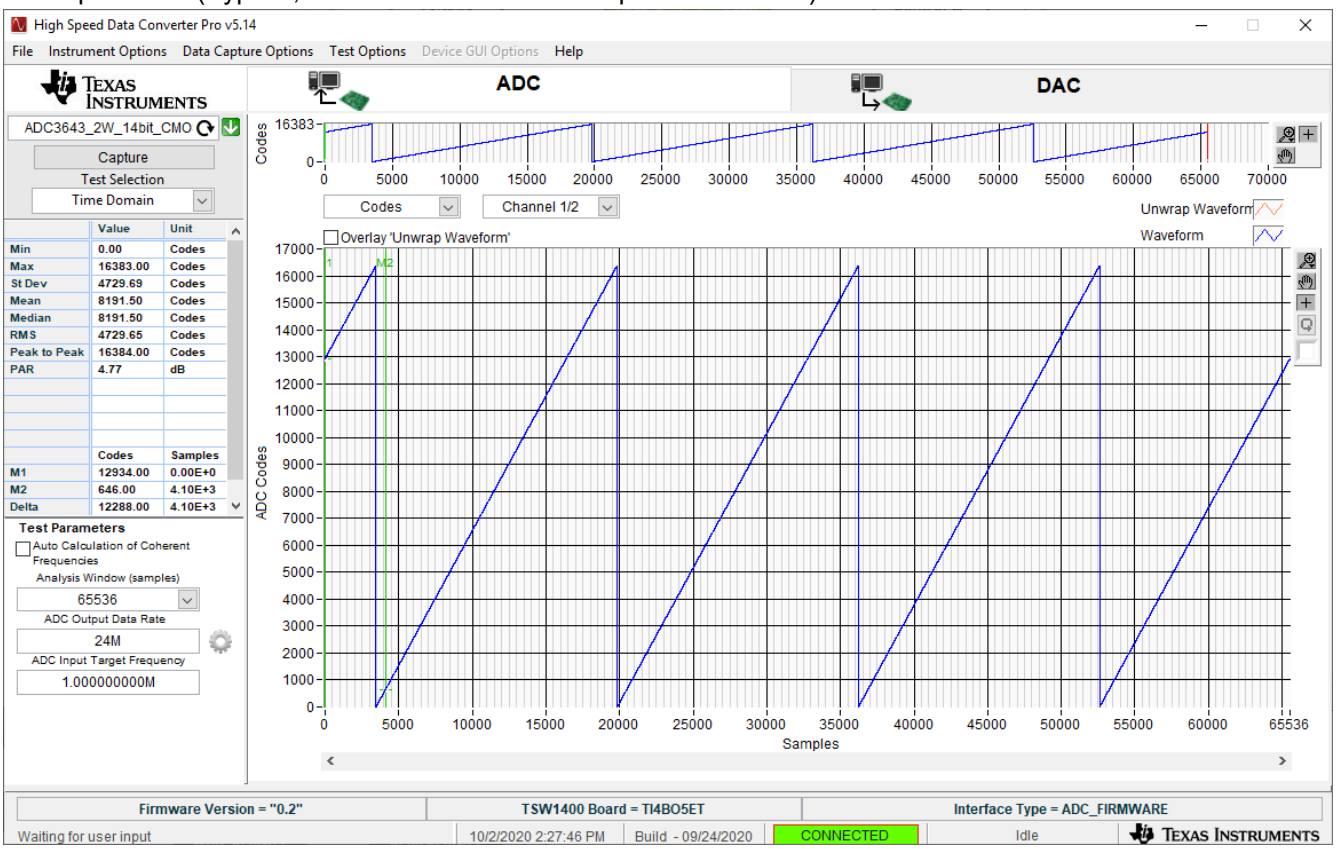

Figure 7-2. HSDC Pro Digital Ramp Pattern

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