NAND MCP Specification

4Gb (512M x 8) NAND flash + 2Gb(64M x 32) Low Power DDR2 SDRAM

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Revision History:

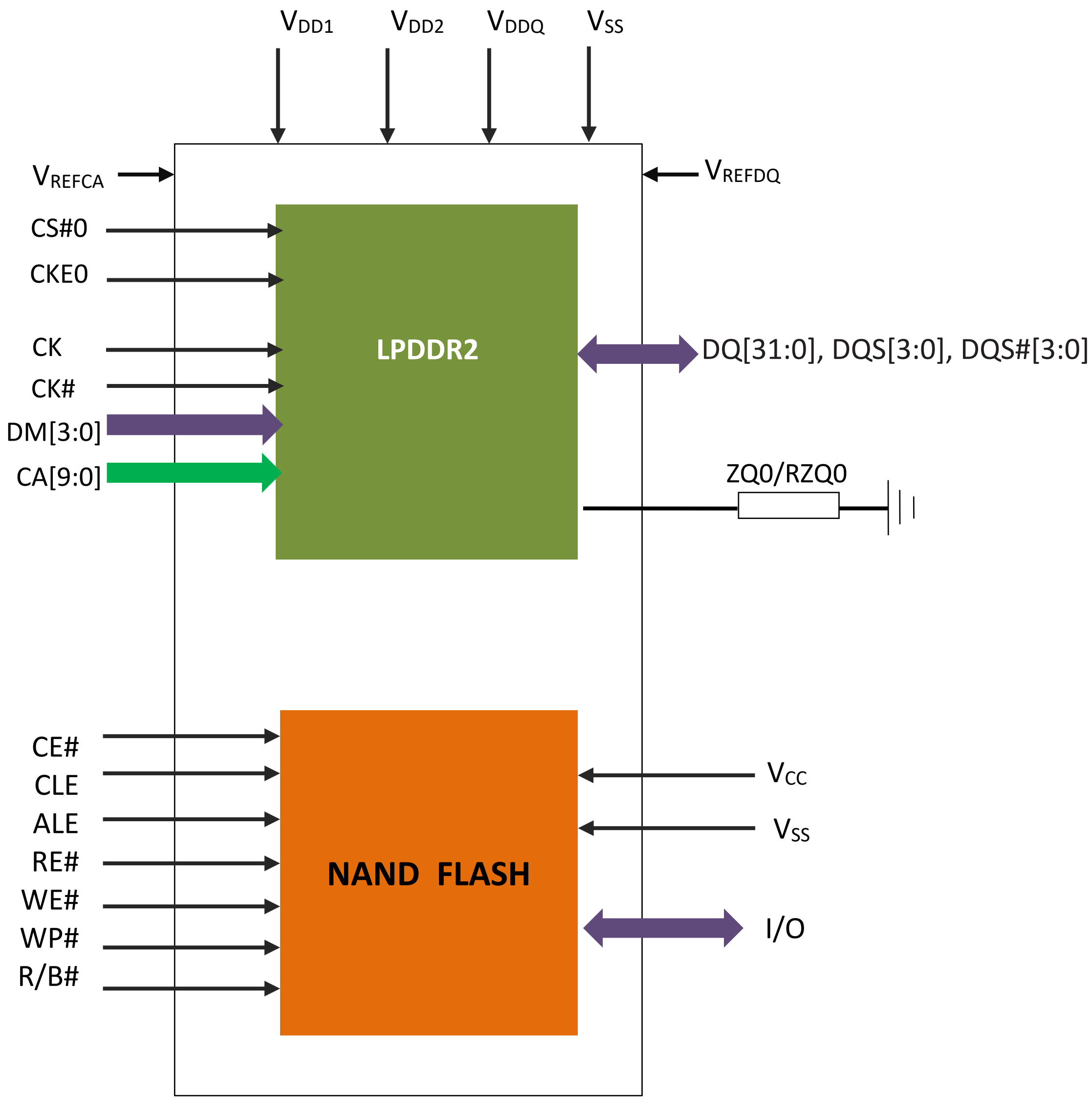
Rev.	Date	Changes	Remark
A1.0	2017/5/31	Initial release	Preliminary
A1.1	2017/6/5	Include MCP device block diagram	Preliminary
A1.2	2018/8/15	Revise to modify format	Revision
A1.3	2018/8/17	Correct CK_t of NAND block diagram to CE# in Page3	Revision
A1.4	2018/9/6	Delete company address	Revision
A1.5	2019/3/1	Adjust parameter description errors in AC CHARACTERISTICS for part 1, correct diagrams for Note regarding the WP# signal for part 1, correct mistakes in DC Characteristics 1, AC Characteristics and Advanced Data Retention Current for part 2.	Revision
A1.6	2019/12/4	Correct the unclear description	Revision
A1.7	2020/10/14	Updated Pin Description	Revision
A1.8	2022/11/15	Update logo font	Revision

Introduction

XTX nMCP is a Multi-Chip Packaged memory which combines NAND flash memory and LPDDR2 (Low Power Double Data Rate) SDRAM. The NAND flash memory provides the most cost-effective solution for the non-volatile solid state mass storage market, while the LPDDR2 is an excellent solution for large volatile but fast storage applications such as random/temporary data access.

XTX nMCP is suitable for use in data memory of portable electronic devices to reduce its square size and power consumption at the same time. The NAND flash memory and LPDDR2 SDRAM in it could be operated individually .

MCP Block Diagram



Features

< NAND flash >

- **Single Level per Cell (SLC) Technology**
- **ECC requirement: 8bits/544Bytes**
- **Power Supply Voltage**

  Voltage range: 1.7V ~ 1.95V
- **Organization**

  Page size: x8 (4096 + 256) bytes; 256- bytes spare area

  Block size: x8 (256k + 16k) bytes

  Plane size: 1024 Blocks per Plane
- **Modes**

  Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy, Multi Page Program, Multi Block Erase, Multi Page Copy, Multi Page Read
- **Page Read / Program**

  Random access: 25 µs (Max)

  Sequential access: 25ns(Min)(CL=30pF)

  Program time / Multiplane Program time: 300 µs (Typ.)
- **Block Erase**

  Block Erase time: 3.5 ms (Typ.)
- **Reliability**

  10 Year Data retention (Typ.)

  Blocks 0 is guaranteed to be a valid block at the time of shipment.

<LPDDR2>

Specifications

- Density: 2G bits
- Organization
  - × 32 bits: 8M words × 32 bits × 8 banks
- Power supply
  - VDD1 = 1.70V to 1.95V
  - VDD2, VDDCA, VDDQ = 1.14V to 1.30V
- Clock frequency: 533/466/400/333/266/200/166Mhz(max.)
- 2KB page size
  - Row address: R0 to R13
  - Column address:C0 to C8 (× 32 bits)
- Eight internal banks for concurrent operation
- Interface: HSUL_12
- Burst lengths (BL): 4, 8, 16
- Burst type (BT)
  - Sequential (4, 8, 16)
  - Interleave (4, 8)
- Read latency (RL): 3, 4, 5, 6, 7, 8
- Write latency (WL): 1, 2, 3, 4
- Pre-charge: auto pre-charge option for each burst access
- Programmable driver strength
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 16384 cycles/64ms
  - Average refresh period: 3.9us

Features

- DLL is not implemented
- Low power consumption
- JEDEC LPDDR2-S4B compliance
- Partial Array Self-Refresh (PASR)
- Auto Temperature Compensated Self- Refresh (ATCSR) by built-in temperature sensor
- Deep power-down mode
- Double-data-rate architecture; two data transfers per one clock cycle
- The high-speed data transfer is realized by the 4 bits pre-fetch pipelined architecture
- Differential clock inputs (CK and /CK)
- Commands entered on both rising and falling CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data

Ordering information

Product ID	NAND Flash		Mobile DDR2 SDRAM		Package	Operation Temperature Range
	Configuration	Speed	Configuration	Speed		
XT61M4G8D2TA-B8BEA	4Gb (512M X 8)	25ns	2Gb (8 Banks X 8M X 32 bits)	1066Mbps	162 ball BGA 8x10.5x0.9	Extended
XT61M4G8D2TA-B8BET	4Gb (512M X 8)	25ns	2Gb (8 Banks X 8M X 32 bits)	1066Mbps	162 ball BGA 8x10.5x0.9	Extended
XT61M4G8D2TA-B8BIA	4Gb (512M X 8)	25ns	2Gb (8 Banks X 8M X 32 bits)	1066Mbps	162 ball BGA 8x10.5x0.9	Industrial
XT61M4G8D2TA-B8BIT	4Gb (512M X 8)	25ns	2Gb (8 Banks X 8M X 32 bits)	1066Mbps	162 ball BGA 8x10.5x0.9	Industrial

Part number description

XT 61M 4G8 D2 TA – B 8 B x x

Vendor
XT : XTX

Product family
61M : 1.8v Nand + LPDDR2 MCP

Nand Density/Org
1G8 : 1Gb /x8
2G8 : 2Gb /x8
4G8 : 4Gb /x8

Dram Density/Org
C2 : 1Gb /x32
D2 : 2Gb /x32
E2 : 4Gb /x32

TA: Version
Internal version ref#

Packing type
A: Tray
T: Tape&Reel

Temperature range
E: Extended(-30℃ to 85℃)
I: Industrial(-40℃ to +85℃)

Nand ECC bit
0: 0 bit
B: 8 bit

DRAM speed
8: 1.875ns

Package type
B: 162 ball BGA 8x10.5x0.9

Pin Assignments

	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	WP#	CLE	VCC	IO4	IO7	VCC	DNU	DNU
B	DNU	VCC	NC	ALE	RE#	IO5	NC	NC	VSS	DNU
C	NC	IO1	IO3	WE#	R/B#	IO6				
D	NC	IO0	IO2	CE#	NC	NC				
E	VSS	NC	NC		VDD2	VDD1	DQ31	DQ29	DQ26	DNU
F	VDD1	VSS	RFU		VSS	VSSQ	VDDQ	DQ25	VSSQ	VDDQ
G	VSS	VDD2	ZQ0		VDDQ	DQ30	DQ27	DQS3	DQS3#	VSSQ
H	VSSCA	CA9	CA8		DQ28	DQ24	DM3	DQ15	VDDQ	VSSQ
J	NC/ VDDCA	CA6	CA7		VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ
K	VDD2	CA5	VREFCA		DQS1#	DQS1	DQ10	DQ9	DQ8	VSSQ
L	NC/ VDDCA	VSS	CK#		DM1	VDDQ				
M	VSSCA	NC	CK		VSSQ	VDDQ	VDD2	VSS	VREFDQ	
N	CKE0	RFU	RFU		DM0	VDDQ				
P	CS0#	RFU	RFU		DQS0#	DQS0	DQ5	DQ6	DQ7	VSSQ
R	CA4	CA3	CA2		VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ
T	VSSCA	NC/ VDDCA	CA1		DQ19	DQ23	DM2	DQ0	VDDQ	VSSQ
U	VSS	VDD2	CA0		VDDQ	DQ17	DQ20	DQS2	DQS2#	VSSQ
V	VDD1	VSS	NC		VSS	VSSQ	VDDQ	DQ22	VSSQ	VDDQ
W	DNU	NC	NC		VDD2	VDD1	DQ16	DQ18	DQ21	DNU
Y	DNU	DNU							DNU	DNU

NAND LPDDR2 SUPPLY GROUND

162 balls - Ball Array (Top View)

Pin description

Pin Name	Type	Function
NAND		
VCC	Supply	Supply Voltage: The VCC supplies the power for all the operations (Read, Program, Erase). An internal lock circuit ,prevents the insertion of Commands when VCC is less than VLKO.
VSS	Supply	Ground
I/O0-I/O7	Input/output	Data input/outputs: address inputs, or command inputs
ALE	Input	Address Latch Enable: This input activates the latching of the I/O inputs inside the Address Register on the
CLE	Input	Command Latch Enable: This input activates the latching of the I/O inputs inside the Command Register on
CE#	Input	Chip Enable: This input controls the selection of the device. When the device is not busy CE# low selects
RE#	Input	Read Enable: The RE# input is the serial data-out control, and when active drives the data onto the I/O bus.
WE#	Input	Write Enable: This input latches Command, Address and Data. The I/O inputs are latched on the rising edge
WP#	Input	Write Protect: The WP# pin, when low, provides hardware protection against undesired data modification
R / B#	Output	Ready Busy: The Ready/Busy output is an Open Drain pin that signals the state of the memory.
LP DDR2 SDRAM		
CK, CK#	Input	Clock: CK and are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK. Single Data Rate (SDR) inputs, CK# and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK and CK#. The positive Clock edge . Clock Enable: CKE high activates, and CKE low deactivates internal clock signals, and device Input buffers and output drivers. Power saving modes are entered and exited through CKE transitions.
CA0 – CA9	Input	Command/Address Inputs: Unidirectional command/address bus inputs. Provide the command and address inputs according to the command truth table. CA is considered part of the command code.
DQ0-DQ31	Input / Output	Data Bus: Bi-directional Input / Output data bus.
DM0-DM3	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matched the DQ and DQS. DM0 corresponds to the data on DQ0-DQ7, DM1 corresponds to the data on DQ8-DQ15, DM2, corresponds to the data on DQ16-DQ23, and DM3 corresponds to the data on DQ24-DQ31.
DQS0~3 DQS#0~3	Input / Output	Data Strobe (Bi-directional, Differential): The data strobe is bi-directional (used for read and write data) and Differential DQS ,t is output with read data and input with write data. DQS is edge-aligned to read data, and centered with write data.
ZQ0	Input	Reference Pin for Output Drive Strength Calibration. External impedance (240-ohm): this signal is used to calibrate the device output impedance.

CKE0	**Input**	Clock Enable: CKE high activates, and CKE low deactivates internal clock signals, and device input buffers and output drivers. Power saving modes are entered and exited through CKE transitions. CKE is considered part of the command code. CKE is sampled at the positive Clock edge.
CS0#	**Input**	CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
VDD1	**Supply**	VDD1: LPDDR2 power supply 1.
VDD2	**Supply**	VDD2: LPDDR2 power supply 2.
VDDCA	**Supply**	VDDCA: LPDDR2 CA power supply.
VDDQ	**Supply**	VDDQ: LPDDR2 I/O power supply.
VREFCA	**Supply**	VREFCA: LPDDR2 reference for CA pins.
VREFDQ	**Supply**	VREFDQ: LPDDR2 reference for DQ pins.
VSSCA	**Supply**	VSSCA: LPDDR2 I/O ground.
VSSQ	**Supply**	VSSQ: LPDDR2 I/O ground.

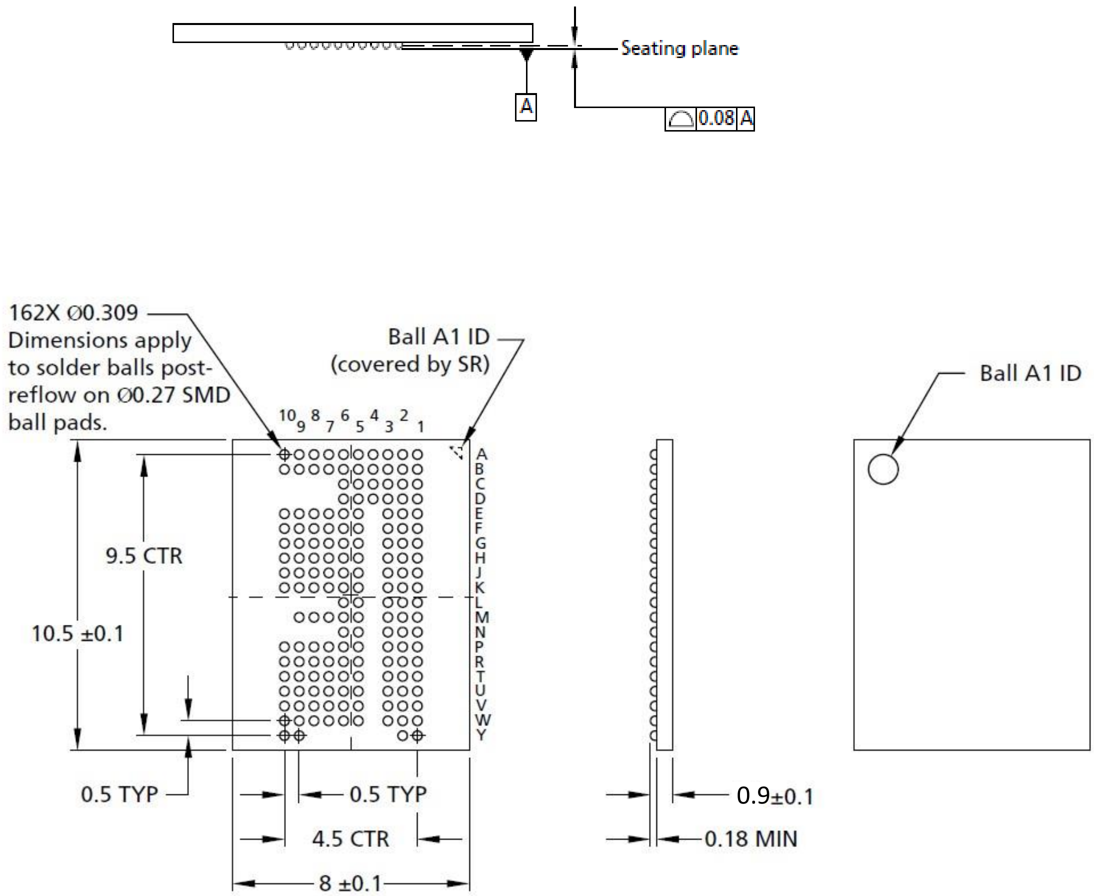
NOTES:

DNU – Do not use: Must be grounded or left floating.

NC – No connect: Not internally connected.

RFU – Reserved for future use.

Package Dimension 8x10.5 package



Notes: 1. All dimensions are in millimeters.

Content

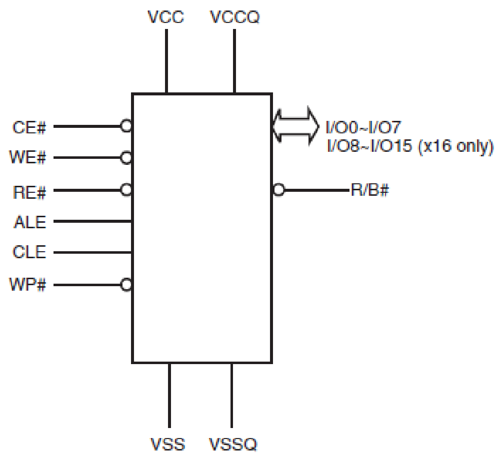
1. NAND Flash Memory Part

1.1. General Description

The NAND is a single 1.8V 4 Gbit (4,563,402,752 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E2PROM) organized as (4096 + 256) bytes × 64 pages × 2048blocks. The device has two 4352-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 4352-byte increments. The Erase operation is implemented in a single block unit (256 Kbytes + 16 Kbytes: 4352 bytes × 64 pages).

The NAND is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

1.2. Logic Diagram



1.3. Pin Description

Pin Name	Description
I/O0 - I/O7 (x8)	**Inputs/Outputs**. The I/O pins are used for command input, address input, data input, and data output. The I/O pins float to High-Z when the device is deselected or the outputs are disabled.
CLE	**Command Latch Enable.** This input activates the latching of the I/O inputs inside the Command Register on the rising edge of Write Enable (WE#).
ALE	**Address Latch Enable.** This input activates the latching of the I/O inputs inside the Address Register on the rising edge of Write Enable (WE#).
CE#	**Chip Enable.** This input controls the selection of the device. When the device is not busy CE# low selects the memory.
WE#	**Write Enable.** This input latches Command, Address and Data. The I/O inputs are latched on the rising edge of WE#.
RE#	**Read Enable.** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WP#	**Write Protect.** The WP# pin, when low, provides hardware protection against undesired data modification (program / erase).
R/B#	**Ready Busy**. The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VCC	**Supply Voltage**. The VCC supplies the power for all the operations (Read, Program, Erase). An internal lock circuit prevents the insertion of Commands when VCC is less than VLKO.
VSS	**Ground.**
NC	**Not Connected.**

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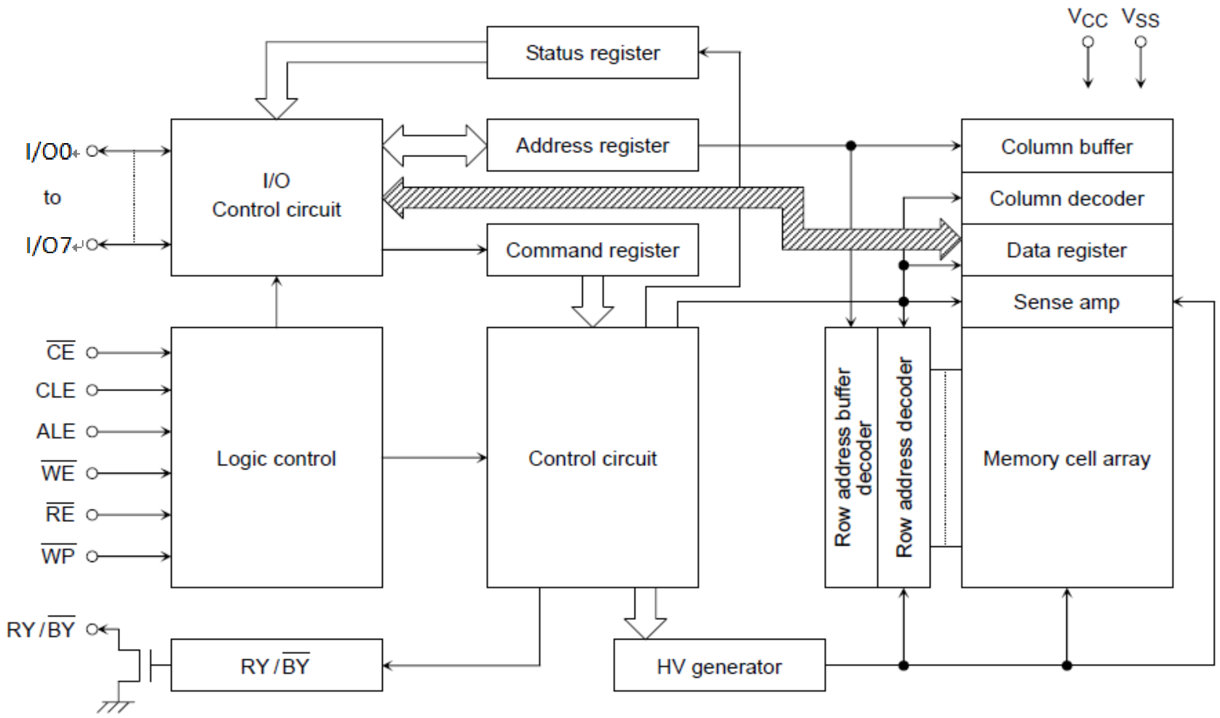
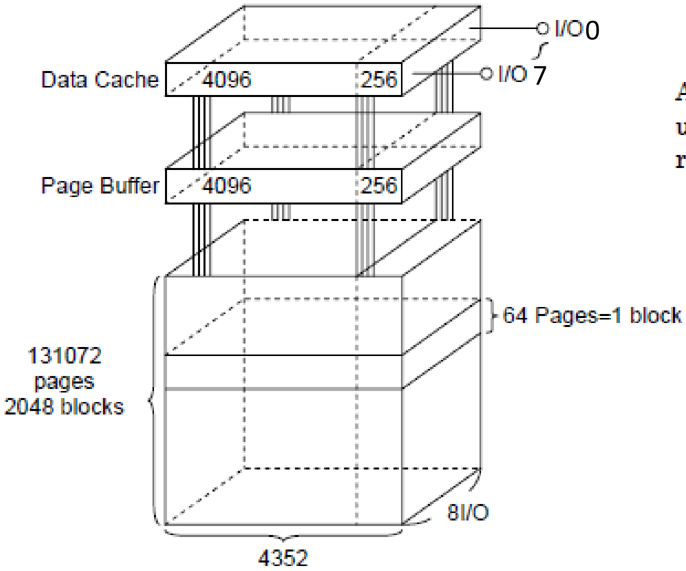
1.4. Block Diagram



1.5. Array Organization

The Program operation works on page units while the Erase operation works on block units.



A page consists of 4352 bytes in which 4096 bytes are used for main memory storage and 256 bytes are for redundancy or for other uses.

1 page = 4352 bytes

1 block = 4352 bytes × 64 pages = (256K + 16K) bytes

Capacity = 4352 bytes × 64pages × 2048 blocks

An address is read in via the I/O port over five consecutive clock cycles, as shown in Table 1.

1.6. Addressing

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	L	CA12	CA11	CA10	CA9	CA8
Third cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8
Fifth cycle	L	L	L	L	L	L	L	PA16

CA0 to CA12: Column adress

PA0 to PA16: Page address

PA6 to PA16: Block address

PA0 to PA5: NAND address in block

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
VCC	Power Supply Voltage	−0.6 to 2.5	V
VIN	Input Voltage	−0.6 to 2.5	V
VI/O	Input /Output Voltage	−0.6 to VCC + 0.3 (≤ 2.5 V)	V
PD	Power Dissipation	0.3	W
TSOLDER	Soldering Temperature (10 s)	260	°C
TSTG	Storage Temperature	−55° C to 125° C	°C
TOPR	Operating Temperature	-40° C to 85° C	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
CIN	Input	VIN = 0 V	–	10	pF
COUT	Output	VOUT = 0 V	–	10	pF

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
NVB	Number of Valid Blocks	2008	–	2048	Blocks

NOTE:

The device occasionally contains unusable blocks. The first block (Block 0) is guaranteed to be a valid block at the time of shipment. The specification for the minimum number of valid blocks is applicable over lifetime The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
VCC	Power Supply Voltage	1.7	–	1.95	V
VIH	High Level input Voltage	Vcc x 0.8	–	VCC + 0.3	V
VIL	Low Level Input Voltage	−0.3*	–	Vcc x 0.2	V

* −2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta = -40 to 85℃, VCC = 1.7 to 1.95V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
IIL	Input Leakage Current	VIN = 0 V to VCC	–	–	±10	µA
ILO	Output Leakage Current	VOUT = 0 V to VCC	–	–	±10	µA
ICCO1	Serial Read Current	CE# = VIL, IOUT = 0 mA, tcycle = 25ns	–	–	30	mA
ICCO2	Programming Current	–	–	–	30	mA
ICCO3	Erasing Current	–	–	–	30	mA
ICCS	Standby Current	CE# = VCC−0.2 V, WP# = 0 V/VCC	–	–	50	µA
VOH	High Level Output Voltage	IOH = −0.1 mA	Vcc – 0.2	–	–	V
VOL	Low Level Output Voltage	IOL = 0.1 mA	–	–	0.2	V
IOL (RY / BY#)	Output current of RY / BY# pin	VOL = 0.2 V	–	4	–	mA

AC CHARACTERISTICS AND RECOMMENDED OPERATING (Ta = -40 to 85℃, VCC = 1.7 to 1.95V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
tCLS	CLE Setup Time	12	–	ns
tCLH	CLE Hold Time	5	–	ns
tCS	CE# Setup Time	20	–	ns
tCH	CE# Hold Time	5	–	ns
tWP	Write Pulse Width	12	–	ns
tALS	ALE Setup Time	12	–	ns
tALH	ALE Hold Time	5	–	ns
tDS	Data Setup Time	12	–	ns
tDH	Data Hold Time	5	–	ns
tWC	Write Cycle Time	25	–	ns
tWH	WE# High Hold Time	10	–	ns
tWW	WP# High to WE# Low	100	–	ns
tRR	Ready to RE# Falling Edge	20	–	ns
tRW	Ready to WE# Falling Edge	20	–	ns
tRP	Read Pulse Width	12	–	ns
tRC	Read Cycle Time	25	–	ns
tREA	RE# Access Time	–	20	ns
tCEA	CE# Access Time	–	25	ns
tCLR	CLE Low to RE# Low	10	–	ns
tAR	ALE Low to RE# Low	10	–	ns
tRHOH	RE# High to Output Hold Time	25	–	ns
tRLOH	RE# Low to Output Hold Time	5	–	ns
tRHZ	RE# High to Output High Impedance	–	60	ns
tCHZ	CE# High to Output High Impedance	–	20	ns
tCSD	CE# High to ALE or CLE Don't Care	0	–	ns
tREH	RE# High Hold Time	10	–	ns
tIR	Output-High-impedance-to-RE# Falling Edge	0	–	ns
tRHW	RE# High to WE# Low	30	–	ns
tWHC	WE# High to CE# Low	30	–	ns
tWHR	WE# High to RE# Low	60	–	ns
tR	Memory Cell Array to Starting Address	–	25	µs
tDCBSYR1	Data Cache Busy in Read Cache (following 31h and 3Fh)	–	25	µs
tDCBSYR2	Data Cache Busy in Page Copy (following 3Ah)	–	30	µs
tWB	WE# High to Busy	–	100	ns
tRST	Device Reset Time (Ready/Read/Program/Erase)	–	5/5/10/500	µs

*1: tCLS and tALS can not be shorter than tWP

*2: tCS should be longer than tWP +8ns.

AC TEST CONDITIONS

PARAMETER	CONDITION
	VCC: 1.7 to 1.95V
Input level	VCC − 0.2 V, 0.2 V
Input pulse rise and fall time	3 ns
Input comparison level	Vcc / 2
Output data comparison level	Vcc / 2
Output load	CL (30 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the RY/BY

PROGRAMMING AND ERASING CHARACTERISTICS (Ta = -40 to 85℃, VCC = 1.7 to 1.95V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
tPROG	Average Programming Time	–	300	700	µs	
tDCBSYW1	Data Cache Busy Time in Write Cache (following 11h)	–	–	10	µs	
tDCBSYW2	Data Cache Busy Time in Write Cache (following 15h)	–	–	700	µs	(2)
N	Number of Partial Program Cycles in the Same Page	–	–	4		(1)
tBERASE	Block Erasing Time	–	3.5	10	ms	

(1) Refer to Application Note (12) toward the end of this document.

(2) tDCBSYW2 depends on the timing between internal programming time and data in time.

Data Output

When tREH is long, output buffers are disabled by /RE=High, and the hold time of data output depend on tRHOH (25ns MIN). On this condition, waveforms look like normal serial read mode.

When tREH is short, output buffers are not disabled by /RE=High, and the hold time of data output depend on tRLOH (5ns MIN). On this condition, output buffers are disabled by the rising edge of CLE,ALE,/CE or falling edge of /WE, and waveforms look like Extended Data Output Mode.

Mode Selection

The operation modes such as Program, Erase, Read and Reset are controlled by command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, CE# , WE# , RE# and WP# signals as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L	↑	H	*
Data Input	L	L	L	↑	H	H
Address input	L	H	L	↑	H	*
Serial Data Output	L	L	L	H	↓	*
During Program (Busy)	*	*	*	*	*	H
During Erase (Busy)	*	*	*	*	*	H
During Read (Busy)	*	*	H	*	*	*
	*	*	L	H (*2)	H (*2)	*
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/V_{CC}

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

1. **1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit*
2. **2: If CE is low during read busy, $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to the device or read to device. Reset or Status Read command can be input during Read Busy.*

Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	–	
Read	00	30	
Column Address Change in Serial Data Output	05	E0	
Read with Data Cache	31	–	
Read Start for Last Page in Read Cycle with	3F	–	
Auto Page Program	80	10	
Column Address Change in Serial Data Input	85	–	
Auto Program with Data Cache	80	15	
Multi Page Program	80 81 81	11 15 10	
Read for Page Copy (2) with Data Out	00	3A	
Auto Program with Data Cache during Page Copy (2)	8C	15	
Auto Program for last page during Page Copy (2)	8C	10	
Auto Block Erase	60	D0	
ID Read	90	–	
Status Read	70	–	○
Status Read for Multi-Page Program or Multi Block Erase	71	–	○
Reset	FF	–	○

HEX data bit assignment

(Example) Serial Data Input: 80h

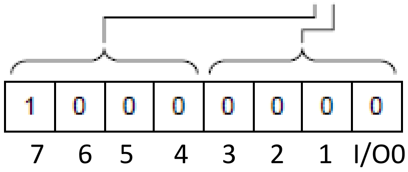


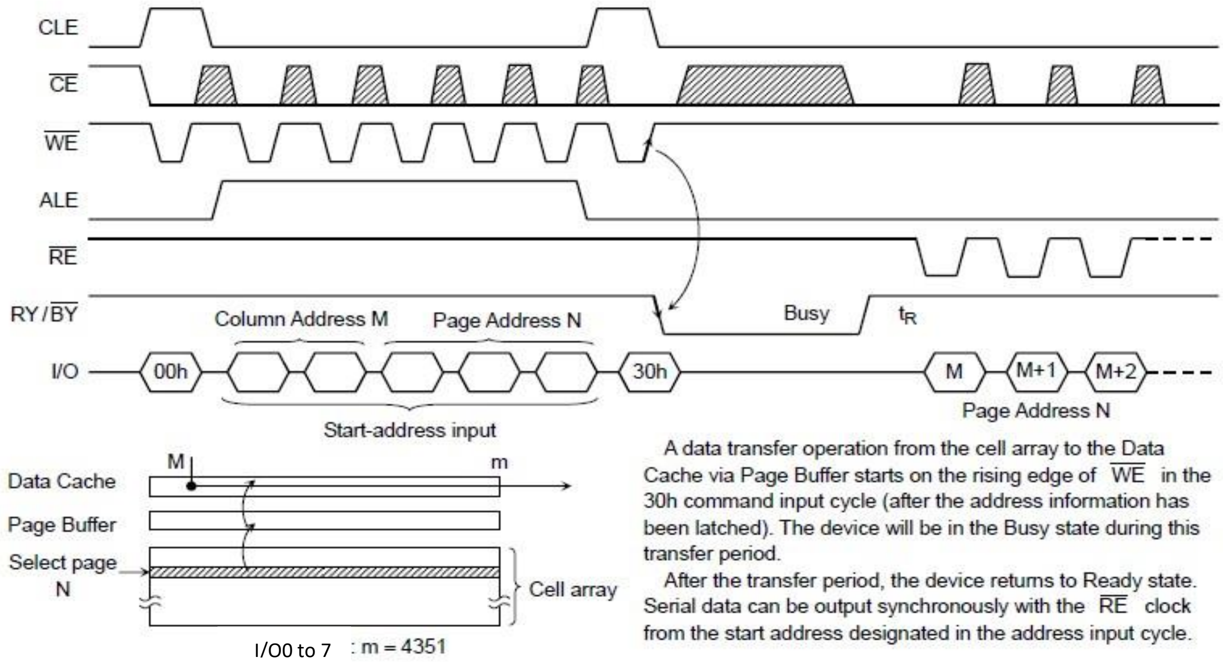
Table 4. Read mode operation states

	CLE	ALE	CE	WE	RE	I/O0 to I/O7	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

H: VIH, L: VIL

1.7. Read Mode

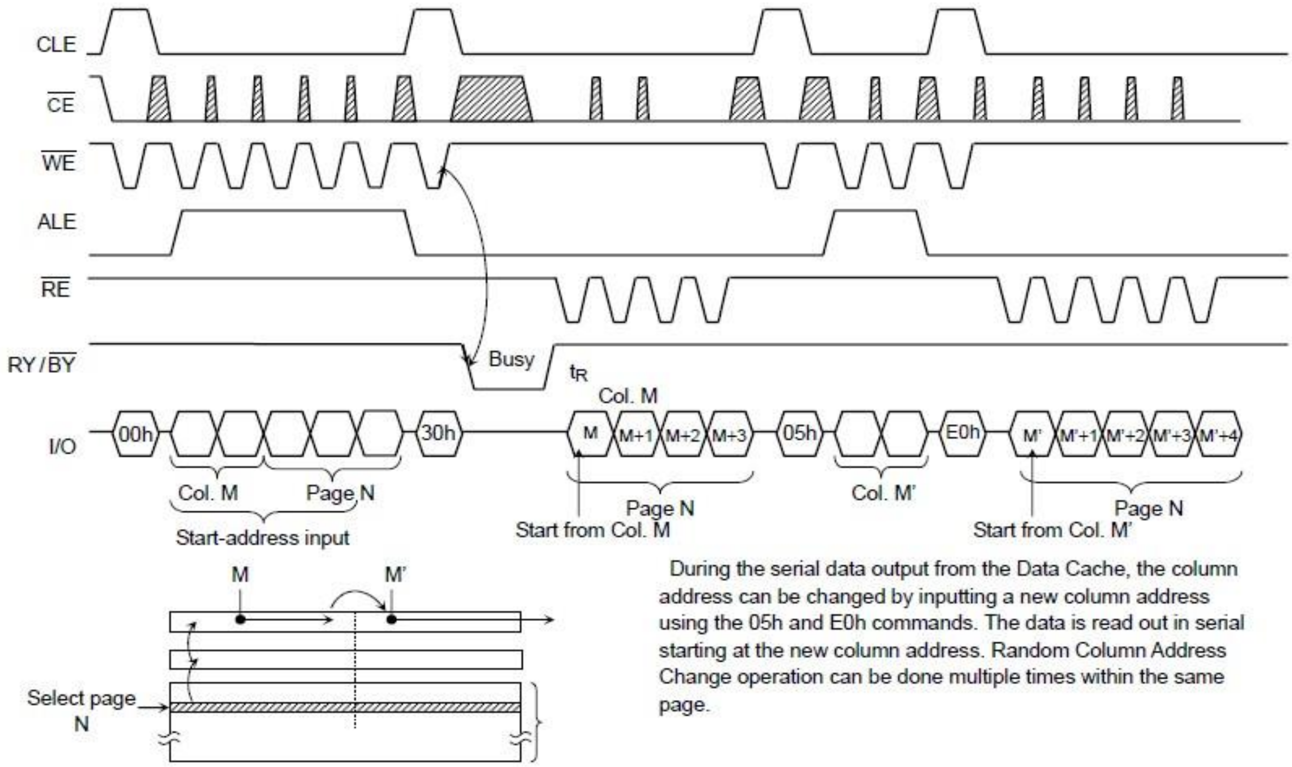
Read mode is set when the "00h" and “30h” commands are issued to the Command register. Between the two commands, a start address for the Read mode needs to be issued. After initial power on sequence, “00h” command is latched into the internal command register. Therefore read operation after power on sequence is executed by the setting of only five address cycles and “30h” command. Refer to the figures below for the sequence and the block diagram (Refer to the detailed timing chart.).



A data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of WE in the 30h command input cycle (after the address information has been latched). The device will be in the Busy state during this transfer period.

After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the RE clock from the start address designated in the address input cycle.

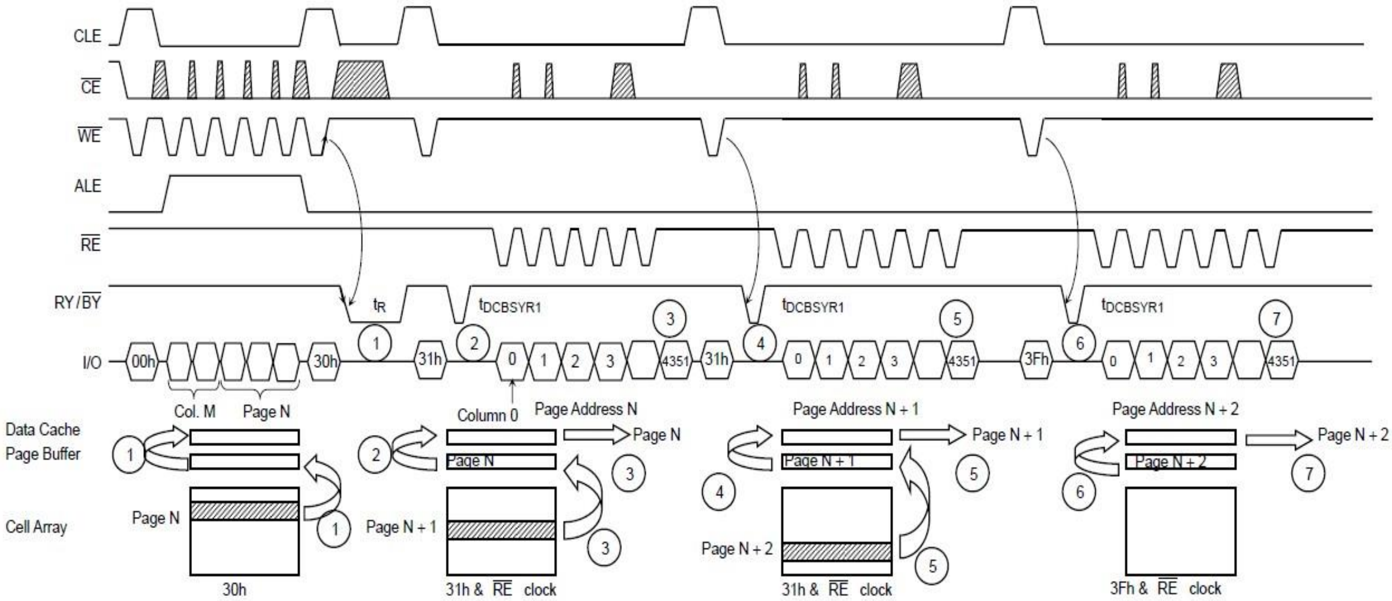
1.7.1. Random Column Address Change in Read Cycle



During the serial data output from the Data Cache, the column address can be changed by inputting a new column address using the 05h and E0h commands. The data is read out in serial starting at the new column address. Random Column Address Change operation can be done multiple times within the same page.

1.7.2. Read Operation with Read Cache

The device has a Read operation with Data Cache that enables the high speed read operation shown below. When the block address changes, this sequence has to be started from the beginning.



If the 31h command is issued to the device, the data content of the next page is transferred to the Page Buffer during serial data out from the Data Cache, and therefore the tR (Data transfer from memory cell to data register) will be reduced.

1. Normal read. Data is transferred from Page N to Data Cache through Page Buffer. During this time period, the device outputs Busy state for tR max.
2. After the Ready/Busy returns to Ready, 31h command is issued and data is transferred to Data Cache from Page Buffer again. This data transfer takes tDCBSYR1 max and the completion of this time period can be detected by Ready/Busy signal.
3. Data of Page N + 1 is transferred to Page Buffer from cell while the data of Page N in Data cache can be read out by /RE clock simultaneously.
4. The 31h command makes data of Page N + 1 transfer to Data Cache from Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max.. This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.
5. Data of Page N + 2 is transferred to Page Buffer from cell while the data of Page N + 1 in Data cache can be read out by /RE clock simultaneously
6. The 3Fh command makes the data of Page N + 2 transfer to the Data Cache from the Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max.. This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.
7. Data of Page N + 2 in Data Cache can be read out, but since the 3Fh command does not transfer the data from the memory cell to Page Buffer, the device can accept new command input immediately after t he completion of serial data out.

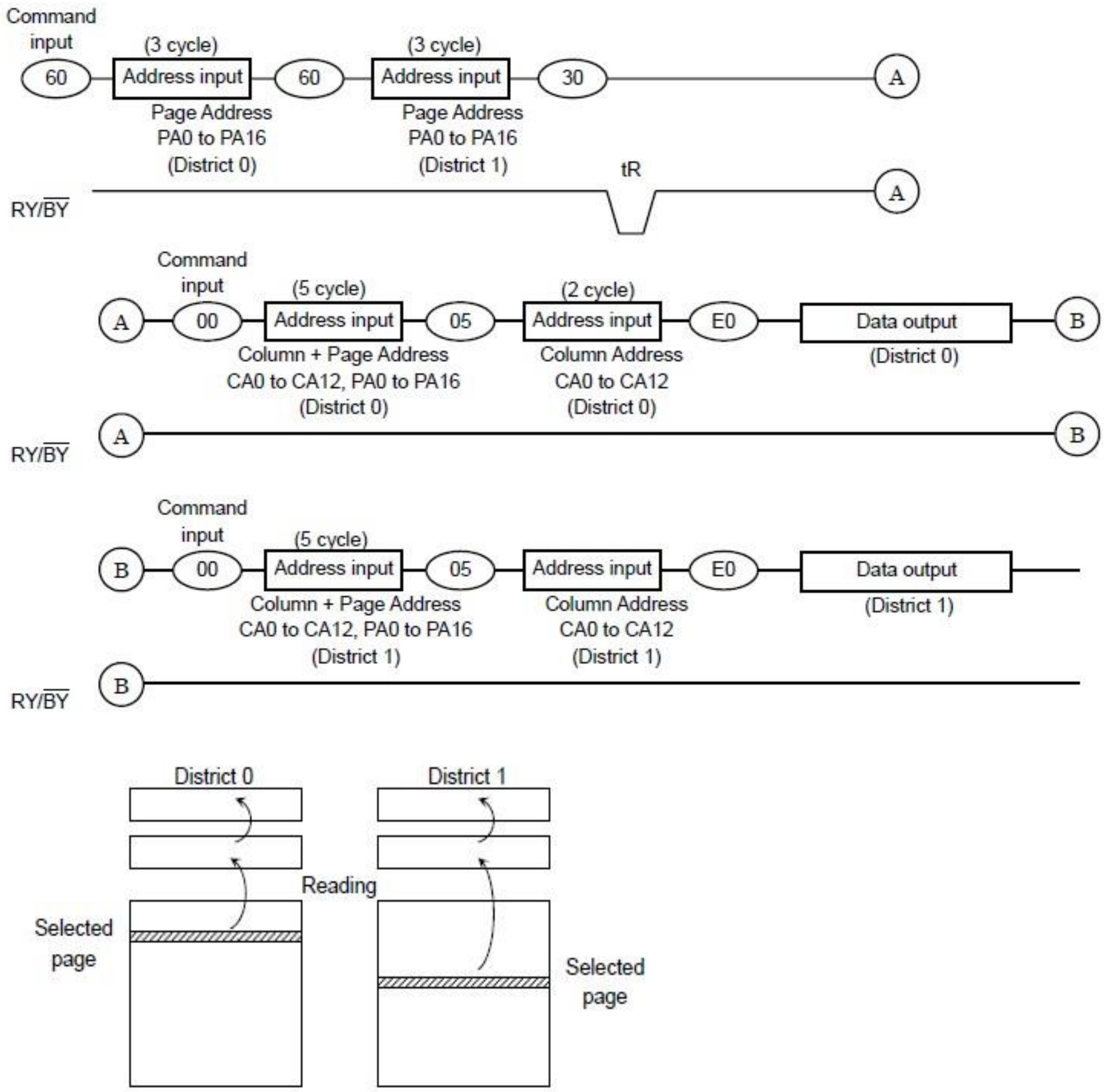
1.7.3. Multi Page Read Operation

The device has a Multi Page Read operation and Multi Page Read with Data Cache operation.

1) Multi Page Read without Data Cache

The sequence of command and address input is shown below.

Same page address (PA0 to PA5) within each district has to be selected.



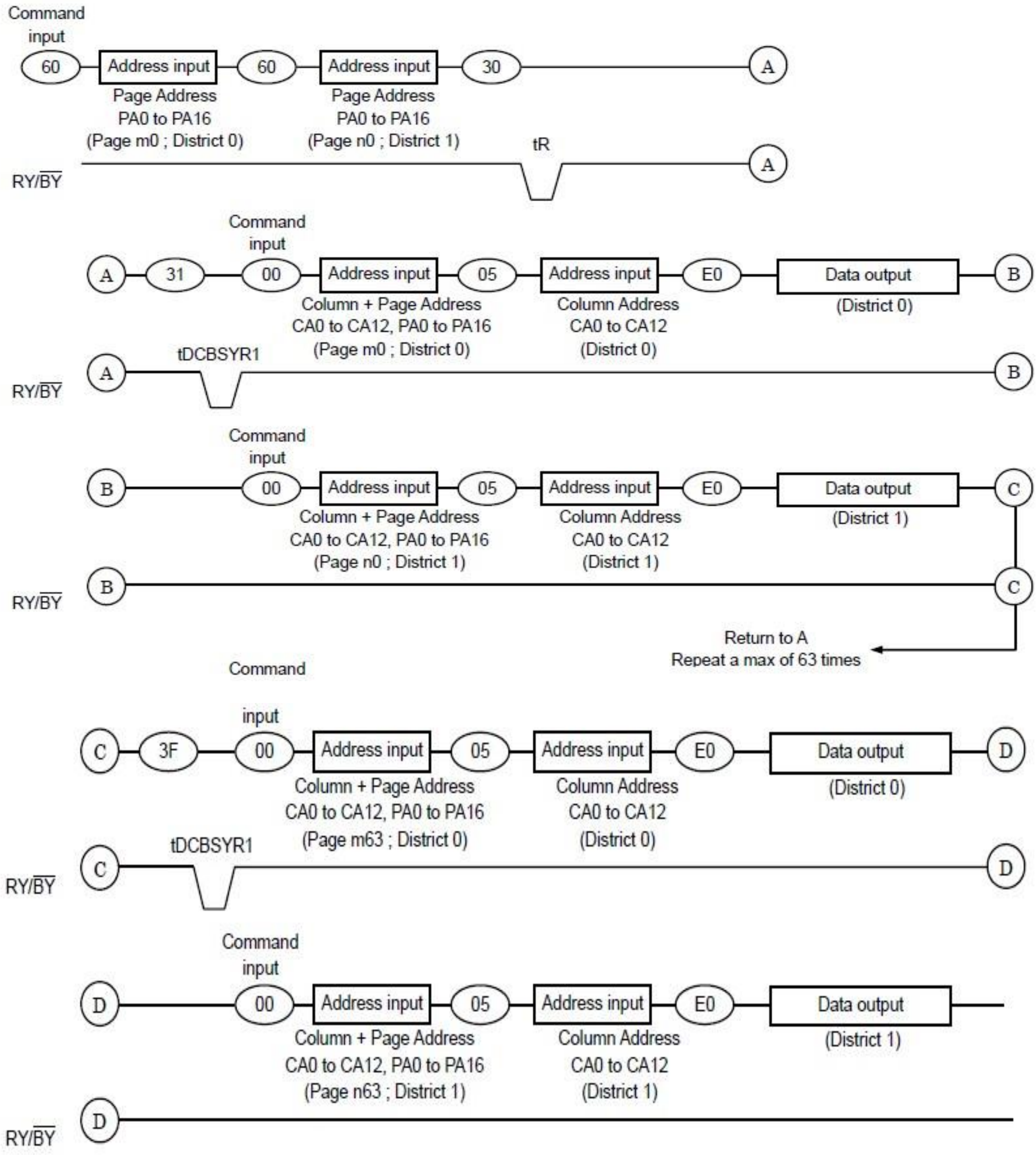
The data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of $\overline{WE}$ in the 30h command input cycle (after the 2 Districts address information has been latched). The device will be in the Busy state during this transfer period.

After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start address designated in the address input cycle.

2) Multi Page Read with Data Cache

When the block address changes (increments) this sequenced has to be started from the beginning. The sequence of command and address input is shown below.

Same page address (PA0 to PA5) within each district has to be selected.



Notes:

(a) Internal addressing in relation with the Districts

To use Multi Page Read operation, the internal addressing should be considered in relation with the District.

- The device consists from 2 Districts.
- Each District consists from 1024 erase blocks.
- The allocation rule is follows.

District 0: Block 0, Block 2, Block 4, Block 6,···, Block 2046

District 1: Block 1, Block 3, Block 5, Block 7,···, Block 2047

(b) Address input restriction for the Multi Page Read operation There are following restrictions in using Multi Page Read; (Restriction) Maximum one block should be selected from each District.

Same page address (PA0 to PA5) within two districts has to be selected.

For example;

(60) [District 0, Page Address 0x00000] (60) [District 1, Page Address 0x00040] (30)

(60) [District 0, Page Address 0x00001] (60) [District 1, Page Address 0x00041] (30)

(Acceptance)

There is no order limitation of the District for the address input.

For example, following operation is accepted;

(60) [District 0] (60) [District 1] (30)

(60) [District 1] (60) [District 0] (30)

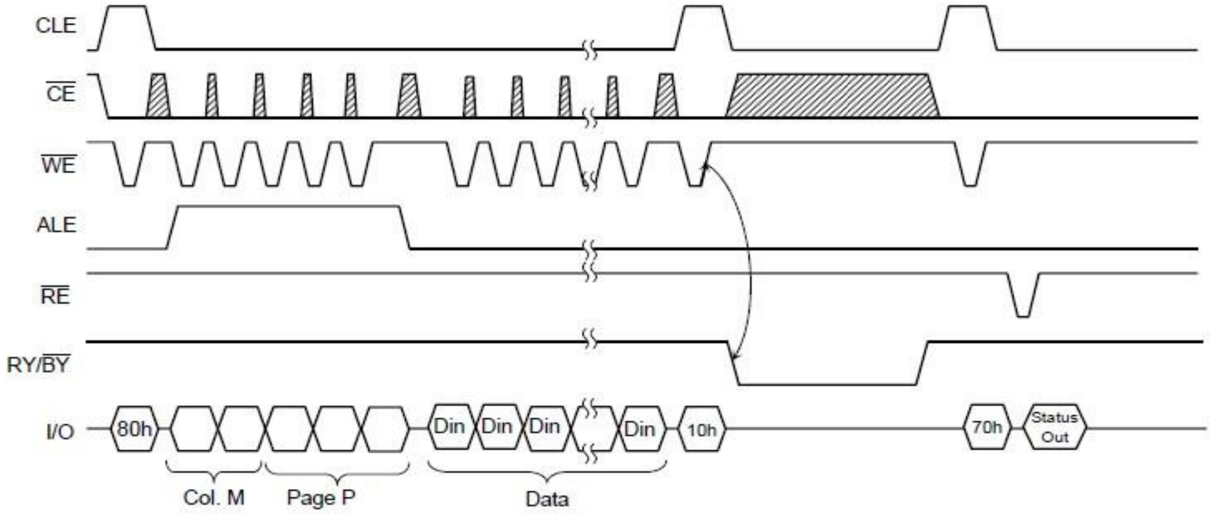
It requires no mutual address relation between the selected blocks from each District.

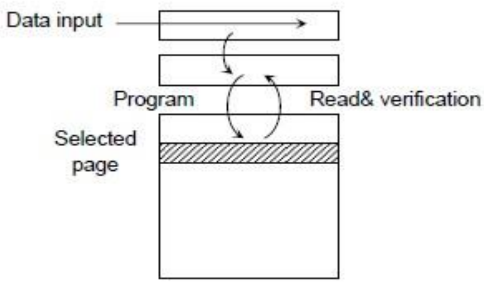
(c) $\overline{\text{WP}}$ signal

Make sure $\overline{\text{WP}}$ is held to High level when Multi Page Read operation is performed.

1.8. Auto Page Program Operation

The device carries out an Automatic Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)



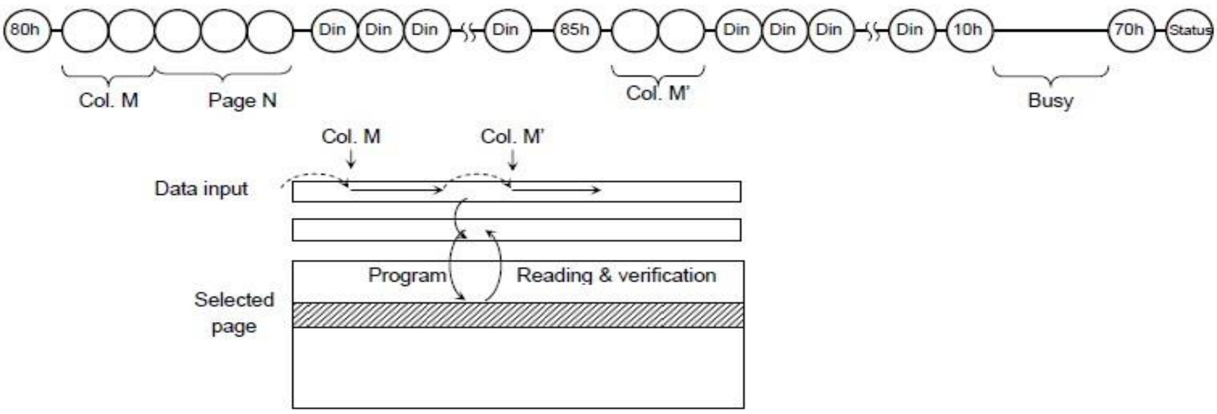


The data is transferred (programmed) from the Data Cache via the Page Buffer to the selected page on the rising edge of WE following input of the "10h" command. After programming, the programmed data is transferred back to the Page Buffer to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

1.8.1. Random Column Address Change in Auto Page Program Operation

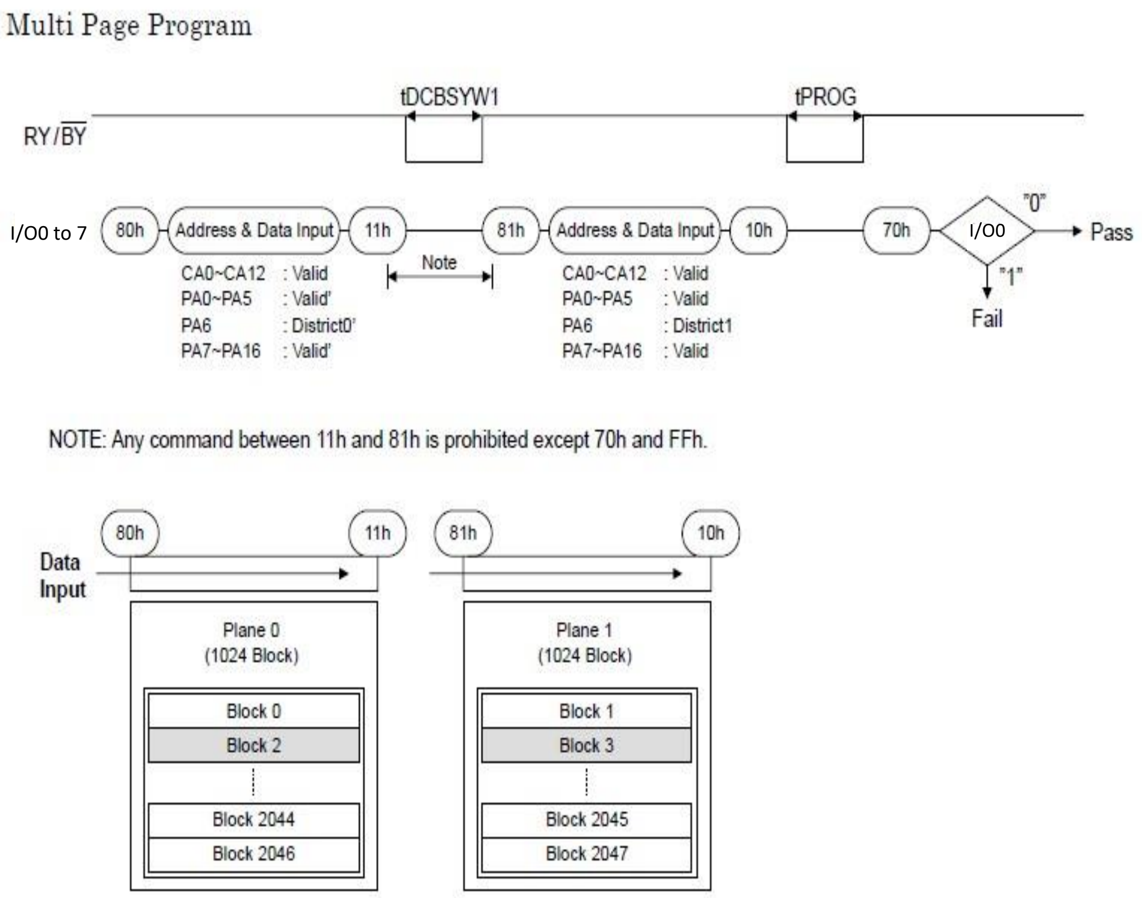
The column address can be changed by the 85h command during the data input sequence of the Auto Page Program operation.

Two address input cycles after the 85h command are recognized as a new column address for the data input. After the new data is input to the new column address, the 10h command initiates the actual data program into the selected page automatically. The Random Column Address Change operation can be repeated multiple times within the same page.



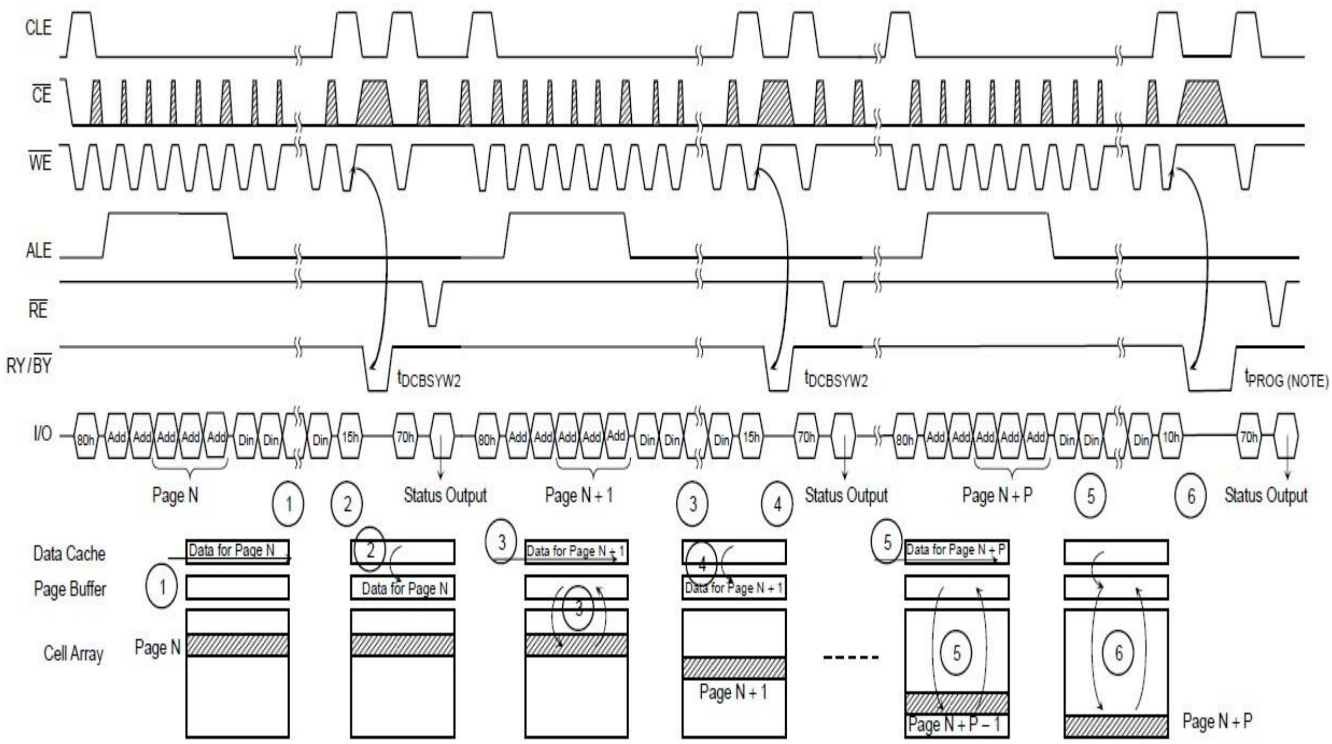
1.8.2. Multi Page Program

The device has a Multi Page Program, which enables even higher speed program operation compared to Auto Page Program. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.) Although two planes are programmed simultaneously, pass/fail is not available for each page by "70h" command when the program operation completes. Status bit of I/O 1 is set to “1” when any of the pages fails. Limitation in addressing with Multi Page Program is shown below.



1.8.3. Auto Page Program Operation with Data Cache

The device has an Auto Page Program with Data Cache operation enabling the high speed program operation shown below. When the block address changes this sequenced has to be started from the beginning.



Issuing the 15h command to the device after serial data input initiates the program operation with Data Cache.

1. Data for Page N is input to Data Cache.
2. Data is transferred to the Page Buffer by the 15h command. During the transfer the Ready/Busy outputs Busy State (tDCBSYW2).
3. Data is programmed to the selected page while the data for page N + 1 is input to the Data Cache.
4. By the 15h command, the data in the Data Cache is transferred to the Page Buffer after the programming of page N is completed. The device output busy state from the 15h command until the Data Cache becomes empty. The duration of this period depends on timing between the internal programming of page N and serial data input for Page N + 1 (tDCBSYW2).
5. Data for Page N + P is input to the Data Cache while the data of the Page N + P − 1 is being programmed.
6. The programming with Data Cache is terminated by the 10h command. When the device becomes Ready, it shows that the internal programming of the Page N + P is completed.

NOTE: Since the last page programming by the 10h command is initiated after the previous cache program, the tPROG during cache programming is given by the following; tPROG = tPROG for the last page + tPROG of the previous page − (command input cycle + address input cycle + data input cycle time of the last page)

Pass/fail status for each page programmed by the Auto Page Programming with Data Cache operation can be detected by the Status Read operation.

- I/O0 : Pass/fail of the current page program operation.
- I/O1 : Pass/fail of the previous page program operation.

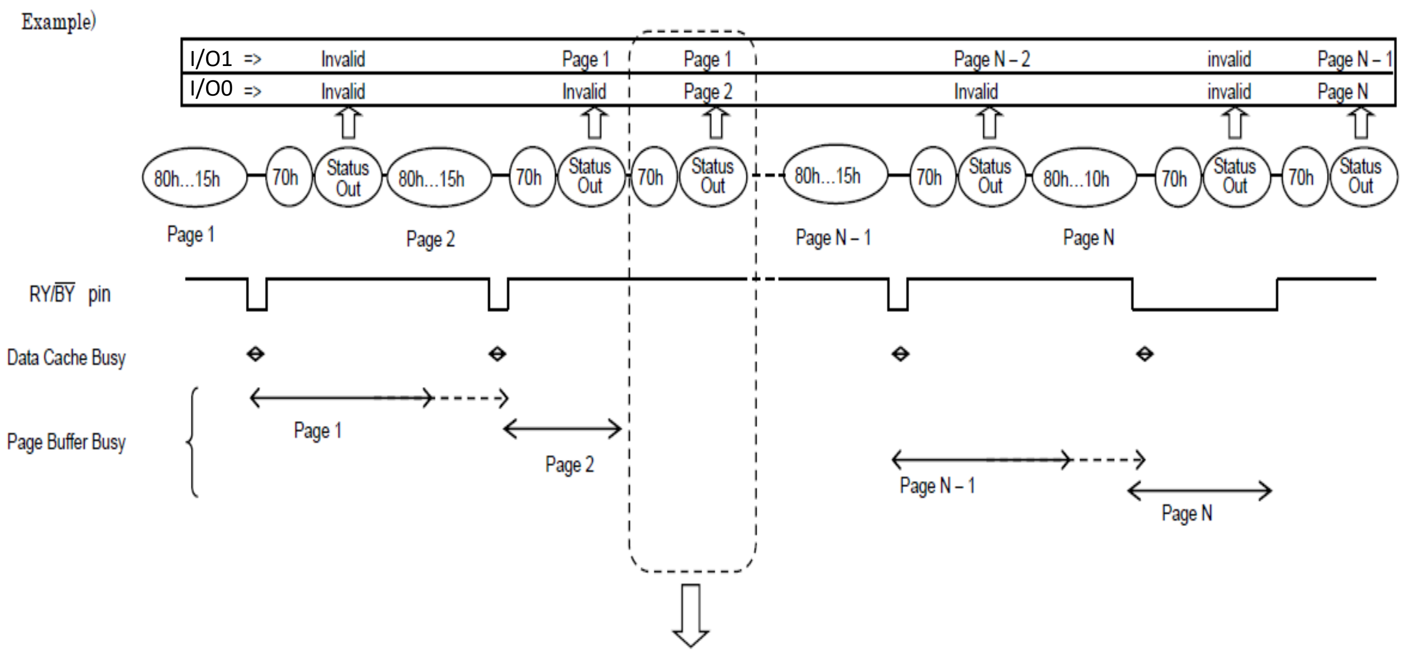
The Pass/Fail status on I/O0 and I/O1 are valid under the following conditions.

- Status on I/O0: Page Buffer Ready/Busy is Ready State.

  The Page Buffer Ready/Busy is output on I/O5 by Status Read operation or RY / $\overline{BY}$ pin after the 10h command.

- Status on I/O1: Data Cache Read/Busy is Ready State.

  The Data Cache Ready/Busy is output on I/O6 by Status Read operation or RY / $\overline{BY}$ pin after the 15h command.

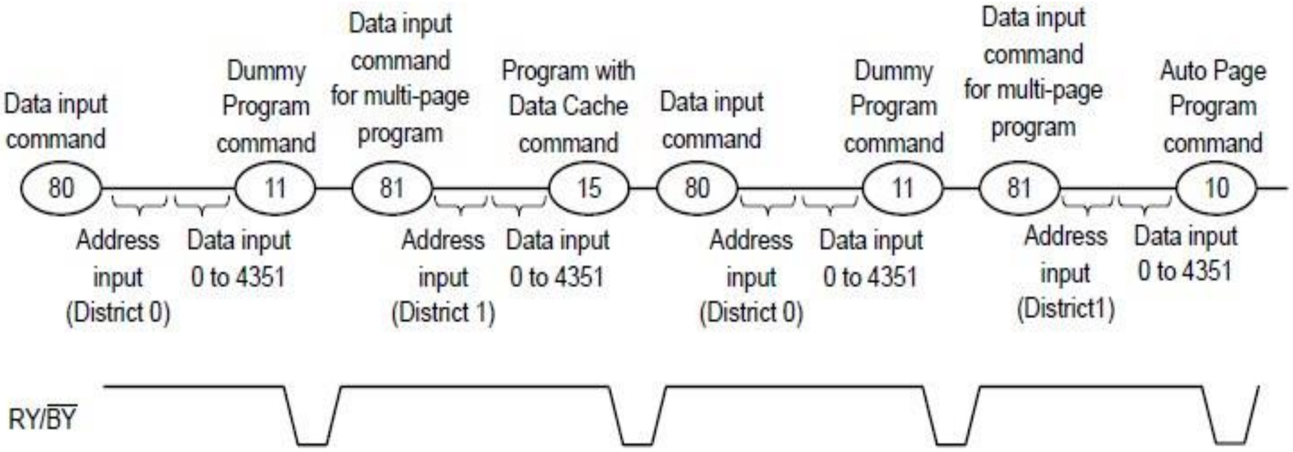


If the Page Buffer Busy returns to Ready before the next 80h command input, and if Status Read is done during this Ready period, the Status Read provides pass/fail for Page 2 on I/O0 and pass/fail result for Page1 on I/O1

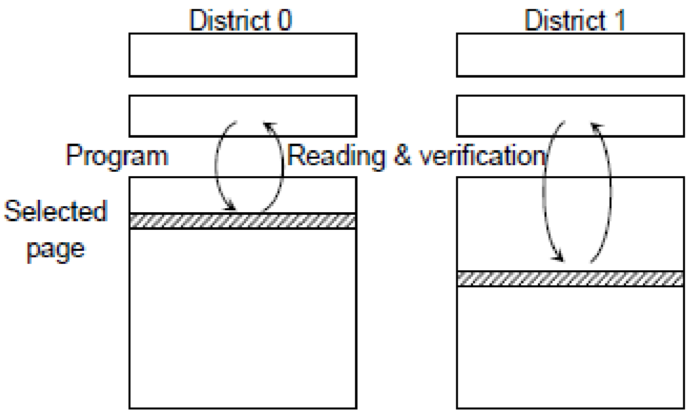
1.8.4. Multi Page Program with Data Cache

The device has a Multi-Page Program with Data Cache operation, which enables even higher speed program operation compared to Auto Page Program with Data Cache as shown below. When the block address changes (increments) this sequenced has to be started from the beginning.

The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)



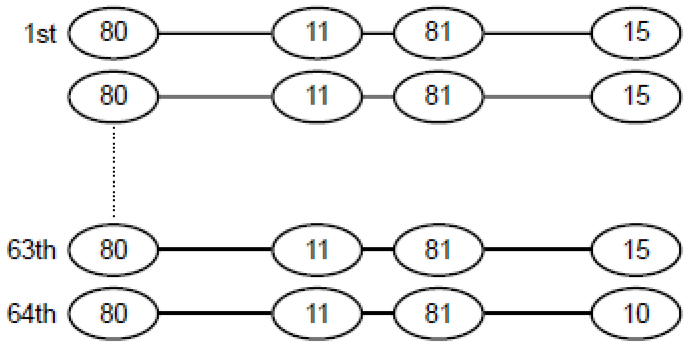
After "15h" or "10h" Program command is input to device, physical programming starts as follows. For details of Auto Program with Data Cache, refer to "Auto Page Program with Data Cache".



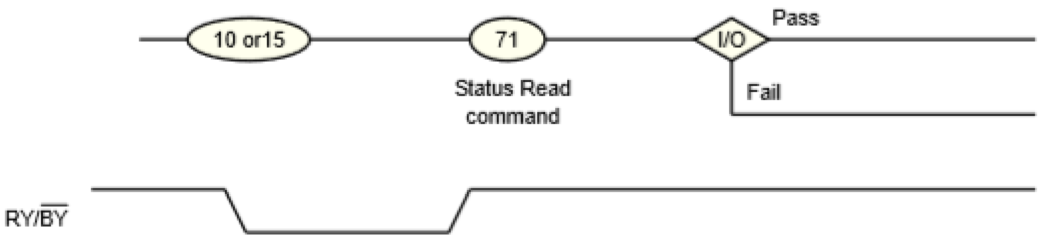
The data is transferred (programmed) from the page buffer to the selected page on the rising edge of /WE following input of the "15h" or "10h" command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Starting the above operation from 1st page of the selected erase blocks, and then repeating the operation total 64 times with incrementing the page address in the blocks, and then input the last page data of the blocks, "10h" command executes final programming. Make sure to terminate with 81h-10h- command sequence.

In this full sequence, the command sequence is following.



After the “15h” or “10h” command, the results of the above operation is shown through the “71h”Status Read command.



The 71h command Status description is as below.

	STATUS	OUTPUT	
I/O0	Chip Status1 : Pass/Fail	Pass: 0	Fail: 1
I/O1	District 0 Chip Status1 : Pass/Fail	Pass: 0	Fail: 1
I/O2	District 1 Chip Status1 : Pass/Fail	Pass: 0	Fail: 1
I/O3	District 0 Chip Status2 : Pass/Fail	Pass: 0	Fail: 1
I/O4	District 1 Chip Status2 : Pass/Fail	Pass: 0	Fail: 1
I/O5	Ready/Busy	Ready: 1	Busy: 0
I/O6	Data Cache Ready/Busy	Ready: 1	Busy: 0
I/O7	Write Protect	Protect: 0	Not Protect: 1

I/O1 describes Pass/Fail condition of district 0 and 1(OR data of I/O1 and I/O2). If one of the districts fails during multi page program operation, it shows “Fail”.

I/O1 to 4 shows the Pass/Fail condition of each district. For details on “Chip Status1” and “Chip Status2”, refer to section “Status Read”.

Internal addressing in relation with the Districts

To use Multi Page Program operation, the internal addressing should be considered in relation with the District.

- The device consists from 2 Districts.
- Each District consists from 1024 erase blocks.
- The allocation rule is follows.

District 0: Block 0, Block 2, Block 4, Block 6,···, Block 2046

District 1: Block 1, Block 3, Block 5, Block 7,···, Block 2047

Address input restriction for the Multi Page Program with Data Cache operation

There are following restrictions in using Multi Page Program with Data Cache;

(Restriction)

Maximum one block should be selected from each District.

Same page address (PA0 to PA5) within two districts has to be selected.

For example;

(80) [District 0, Page Address 0x00000] (11) (81) [District 1, Page Address 0x00040] (15 or 10)

(80) [District 0, Page Address 0x00001] (11) (81) [District 1, Page Address 0x00041] (15 or 10) (Acceptance)

There is no order limitation of the District for the address input.

For example, following operation is accepted;

(80) [District 0] (11) (81) [District 1] (15 or 10)

(80) [District 1] (11) (81) [District 0] (15 or 10)

It requires no mutual address relation between the selected blocks from each District.

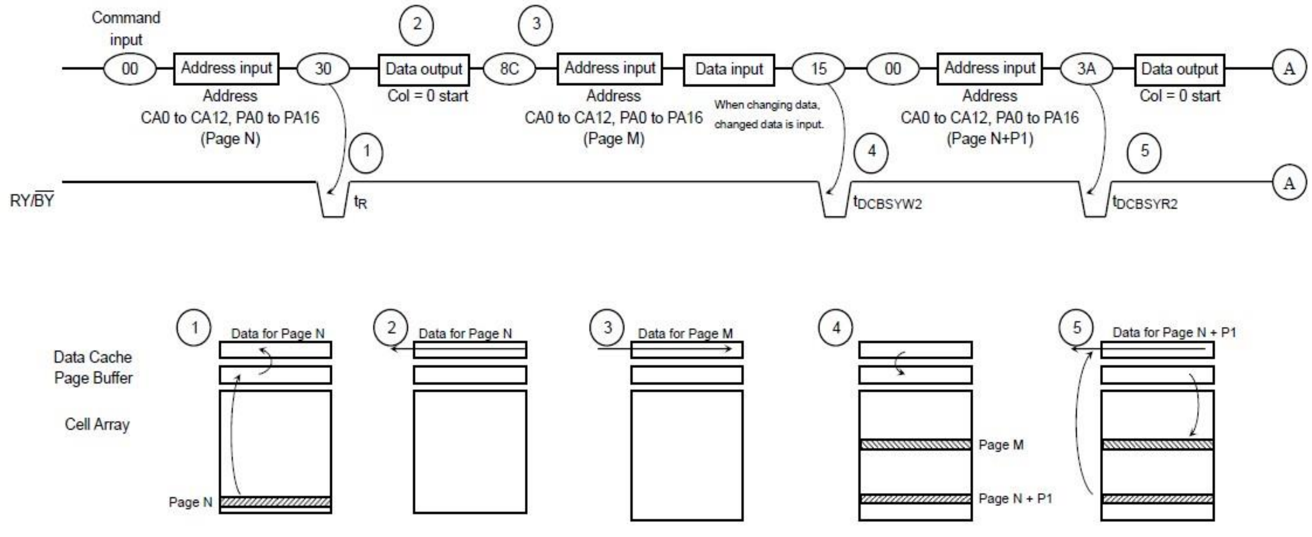
Operating restriction during the Multi Page Program with Data Cache operation (Restriction)

The operation has to be terminated with “10h” command.

Once the operation is started, no commands other than the commands shown in the timing diagram is allowed to be input except for Status Read command and reset command.

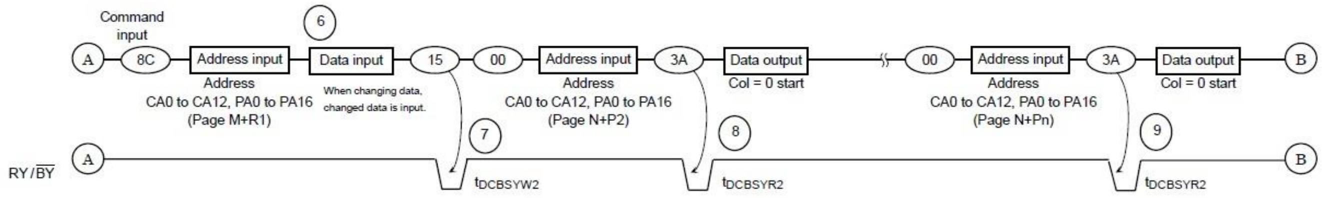
Page Copy (2)

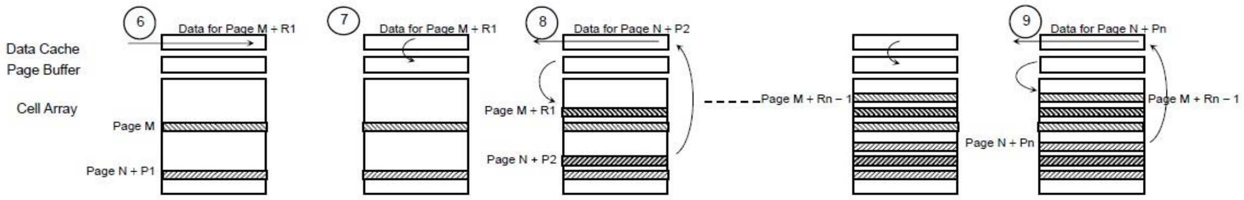
By using Page Copy (2), data in a page can be copied to another page after the data has been read out. When the block address changes (increments) this sequenced has to be started from the beginning.



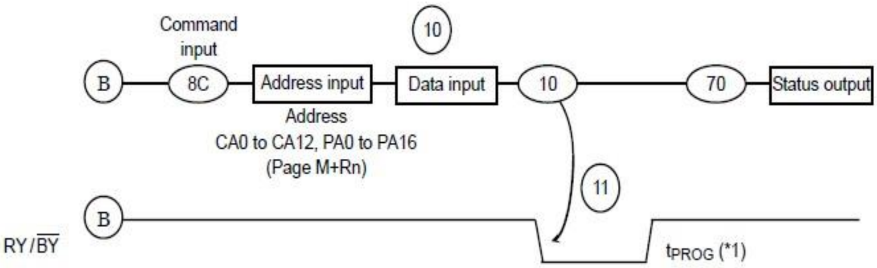
Page Copy (2) operation is as following.

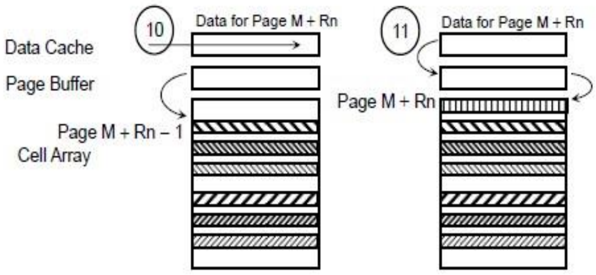
1. Data for Page N is transferred to the Data Cache.
2. Data for Page N is read out.
3. Copy Page address M is input and if the data needs to be changed, changed data is input.
4. Data Cache for Page M is transferred to the Page Buffer.
5. After the Ready state, Data for Page N + P1 is output from the Data Cache while the data of Page M is being programmed.





6. Copy Page address (M + R1) is input and if the data needs to be changed, changed data is input.
7. After programming of page M is completed, Data Cache for Page M + R1 is transferred to the Page Buffer.
8. By the 15h command, the data in the Page Buffer is programmed to Page M + R1. Data for Page N + P2 is transferred to the Data cache.
9. The data in the Page Buffer is programmed to Page M + Rn − 1. Data for Page N + Pn is transferred to the Data Cache.





10. Copy Page address (M + Rn) is input and if the data needs to be changed, changed data is input.
11. By issuing the 10h command, the data in the Page Buffer is programmed to Page M + Rn.

(*1) Since the last page programming by the 10h command is initiated after the previous cache program, the t_{PROG} here will be expected as the following,
t_{PROG} = t_{PROG} of the last page + t_{PROG} of the previous page − (command input cycle + address input cycle + data output/input cycle time of the last page)

NOTE) This operation needs to be executed within District-0 or District-1.

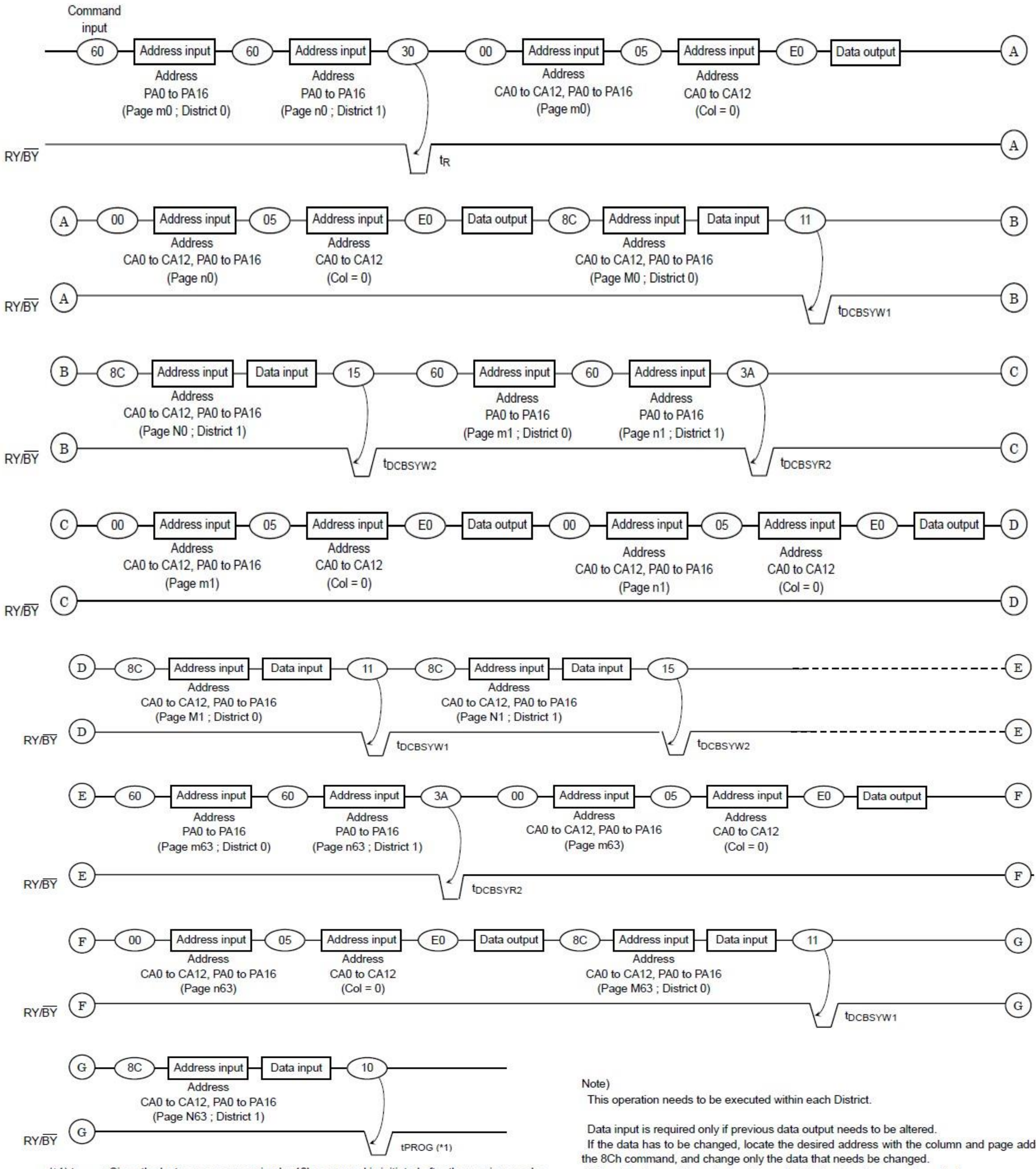
Data input is required only if previous data output needs to be altered.
If the data has to be changed, locate the desired address with the column and page address input after the 8Ch command, and change only the data that needs be changed. If the data does not have to be changed, data input cycles are not required.

Make sure WP# is held to High level when Page Copy (2) operation is performed.

Also make sure the Page Copy operation is terminated with 8Ch-10h command sequence

Multi Page Copy (2)

By using Multi Page Copy (2), data in two pages can be copied to other pages after the data has been read out. When each block address changes (increments) this sequence has to be started from the beginning. Same page address (PA0 to PA5) within two districts has to be selected.



(*1) t_{PROG}: Since the last page programming by 10h command is initiated after the previous cache program, the t_{PROG*} during cache programming is given by the following equation.

t_{PROG} = t_{PROG} of the last page + t_{PROG} of the previous page-A

Note)
This operation needs to be executed within each District.

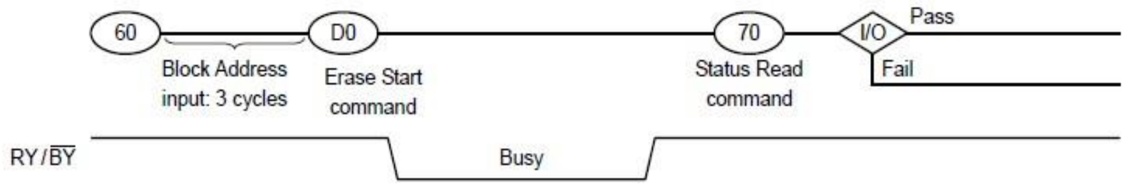
Data input is required only if previous data output needs to be altered.
If the data has to be changed, locate the desired address with the column and page address input the 8Ch command, and change only the data that needs be changed.
If the data does not have to be changed, data input cycles are not required.

Make sure $\overline{WP}$ is held to High level when Multi Page Copy (2) operation is performed.
Also make sure the Multi Page Copy operation is terminated with 8Ch-10h command sequence

1.9. Erase Mode

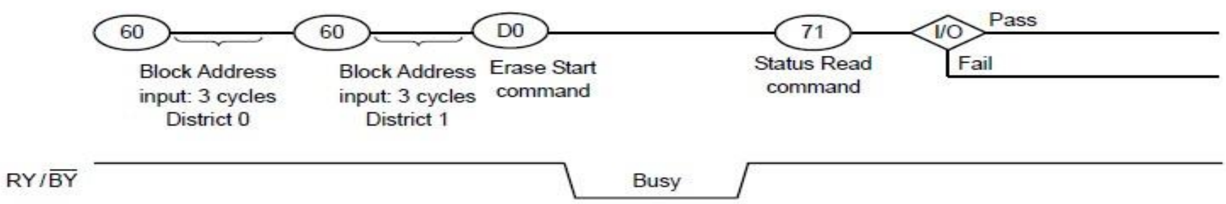
1.9.1. Auto Block Erase

The Auto Block Erase operation starts on the rising edge of WE after the Erase Start command “D0h” which follows the Erase Setup command “60h”. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



1.9.2. Multi Block Erase

The Multi Block Erase operation starts by selecting two block addresses before D0h command as in below diagram. The device automatically executes the Erase and Verify operations and the result can be monitored by checking the status by 71h status read command. For details on 71h status read command, refer to section “Multi Page Program with Data Cache”.



Internal addressing in relation with the Districts

To use Multi Block Erase operation, the internal addressing should be considered in relation with the District.

- The device consists from 2 Districts.
- Each District consists from 1024 erase blocks.
- The allocation rule is follows.

District 0: Block 0, Block 2, Block 4, Block 6,···, Block 2046

District 1: Block 1, Block 3, Block 5, Block 7,···, Block 2047

Address input restriction for the Multi Block Erase

There are following restrictions in using Multi Block Erase (Restriction)

Maximum one block should be selected from each District.

For example;

(60) [District 0] (60) [District 1] (D0) (Acceptance)

There is no order limitation of the District for the address input.

For example, following operation is accepted;

(60) [District 1] (60) [District 0] (D0)

It requires no mutual address relation between the selected blocks from each District.

Make sure to terminate the operation with D0h command. If the operation needs to be terminated before D0h command input, input the FFh reset command to terminate the operation.

1.10. ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:

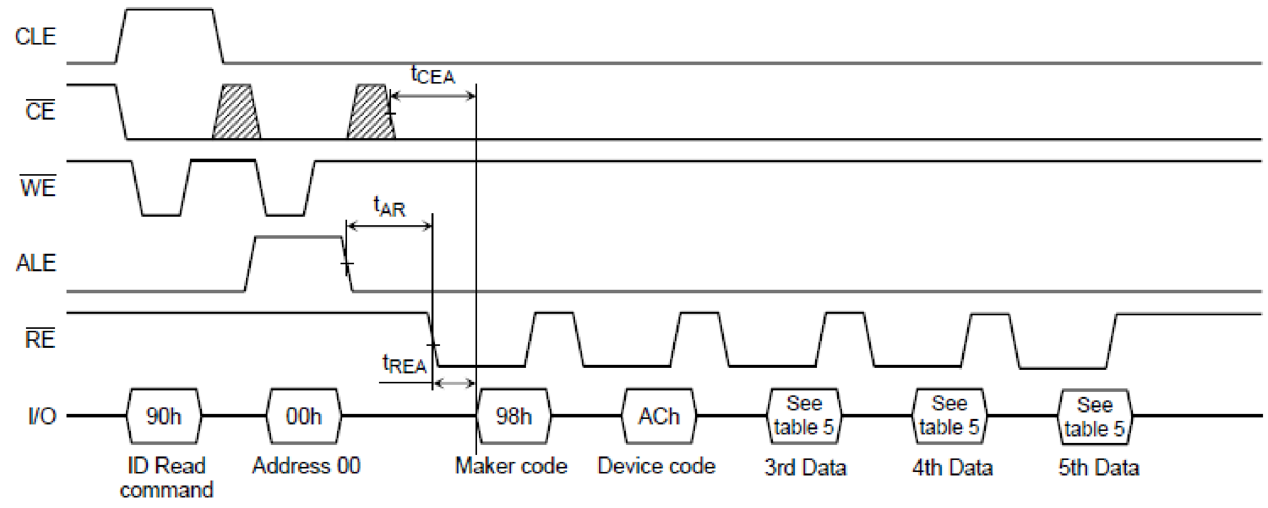


Table 5. Code table

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98h
2nd Data	Device Code	1	0	1	0	1	1	0	0	ACh
3rd Data	Chip Number, Cell Type	1	0	0	1	0	0	0	0	90h
4th Data	Page Size, Block Size,I/O Width	0	0	1	0	0	1	1	0	26h
5th Data	Plane Number	0	1	1	1	0	1	1	0	76h

3rd Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 level cell					0	0		
	4 level cell					0	1		
	8 level cell					1	0		
	16 level cell					1	1		
Reserved		1	0	0	1				

4th Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size	1 KB							0	0
	2 KB							0	1
(without redundant area)	4 KB							1	0
	8 KB							1	1
Block Size	64 KB			0	0				
	128 KB			0	1				
(without redundant area)	256 KB			1	0				
	512 KB			1	1				
I/O Width	x8		0						
	x16		1						
Reserved		0				0	1		

5th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Plane Number	1 Plane					0	0		
	2 Plane					0	1		
	4 Plane					1	0		
	8 Plane					1	1		
Reserved		0	1	1	1			1	0

1.11. Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass /fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using $\overline{RE}$ after a “70h” command input. The Status Read can also be used during a Read operation to find out the Ready/Busy status. The resulting information is outlined in Table 6.

Table 6. Status output table

	Definition	Page program Block Erase	Cache Program	Read Cache read
I/O0	Chip status1 Pass:0 Fail:1	Pass/Fail	Pass/Fail	Invalid
I/O1	Chip status2 Pass:0 Fail:1	Invalid	Pass/Fail	Invalid
I/O2	Not used	0	0	0
I/O3	Not used	0	0	0
I/O4	Not used	0	0	0
I/O5	Page buffer Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O6	Data cache Ready/busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O7	Write protect Not protected : 1 Protected: 0	Write Protect	Write Protect	Write Protect

The Pass/Fail status on I/O0 and I/O1 is only valid during a Program/Erase operation when the device is in the Ready state.

Chip Status 1:

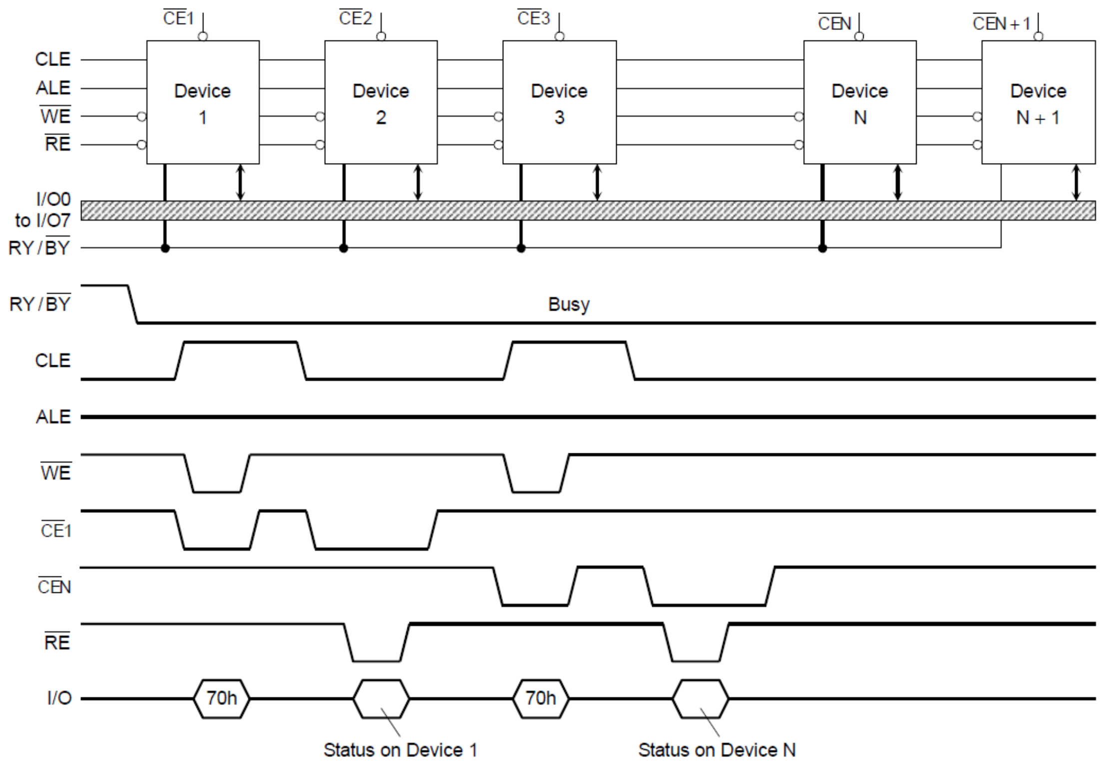
During a Auto Page Program or Auto Block Erase operation this bit indicates the pass/fail result. During a Auto Page Programming with Data Cache operation, this bit shows the pass/fail results of the current page program operation, and therefore this bit is only valid when I/O5 shows the Ready state.

Chip Status 2:

This bit shows the pass/fail result of the previous page program operation during Auto Page Programming with Data Cache. This status is valid when I/O6 shows the Ready State.

The status output on the I/O5 is the same as that of I/O6 if the command input just before the 70h is not 15h or 31h.

An application example with multiple devices is shown in the figure below.



System Design Note: If the RY / BY pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

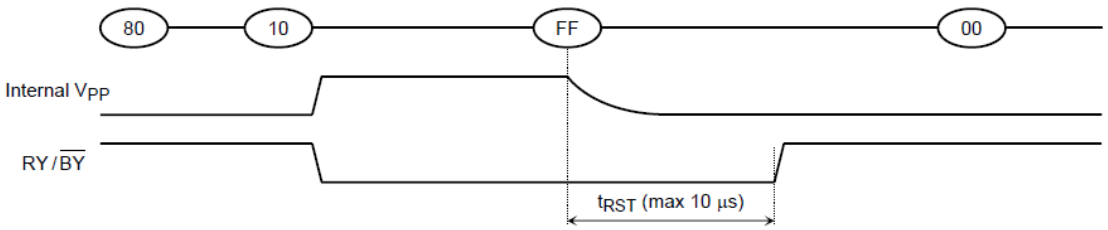
1.12. Reset

The Reset mode stops all operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged to 0 volt and the device enters the Wait state.

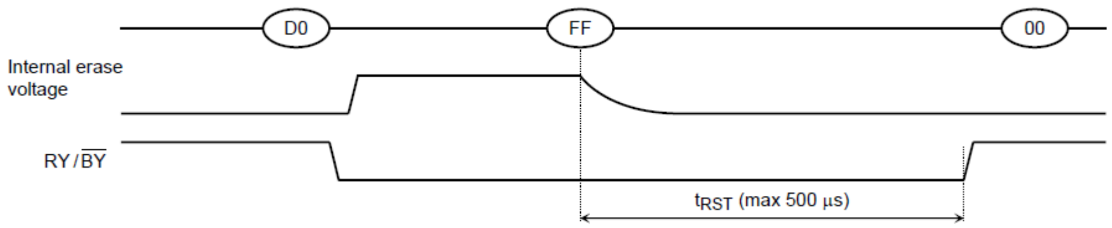
Reset during a Cache Program/Page Copy may not just stop the most recent page program but it may also stop the previous program to a page depending on when the FF reset is input.

The response to a “FFh” Reset command input during the various device operations is as follows:

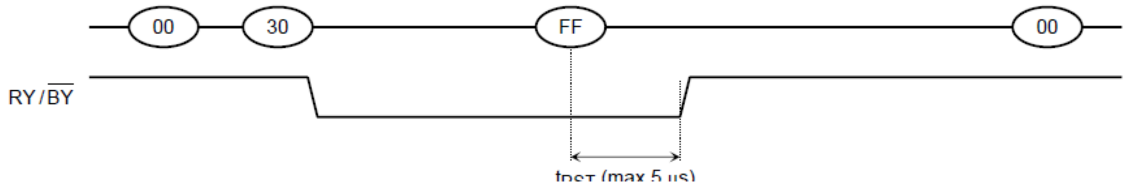
When a Reset (FFh) command is input during programming



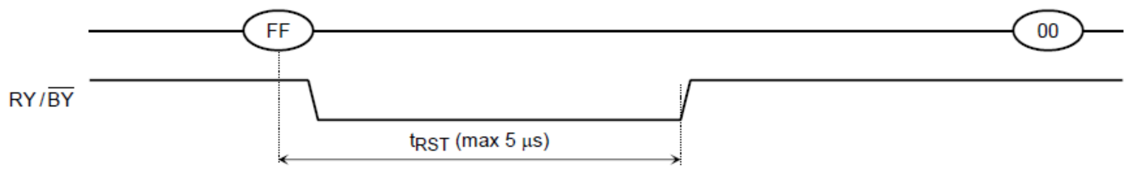
When a Reset (FFh) command is input during erasing



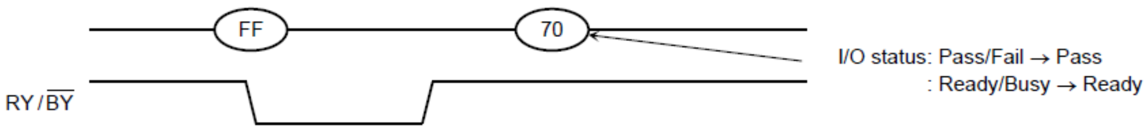
When a Reset (FFh) command is input during Read operation



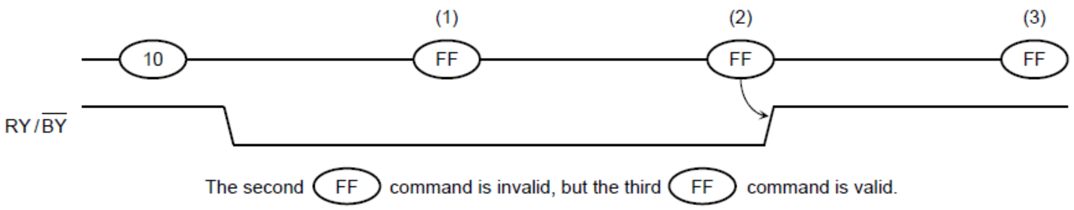
When a Reset (FFh) command is input during Ready



When a Status Read command (70h) is input after a Reset



When two or more Reset commands are input in succession



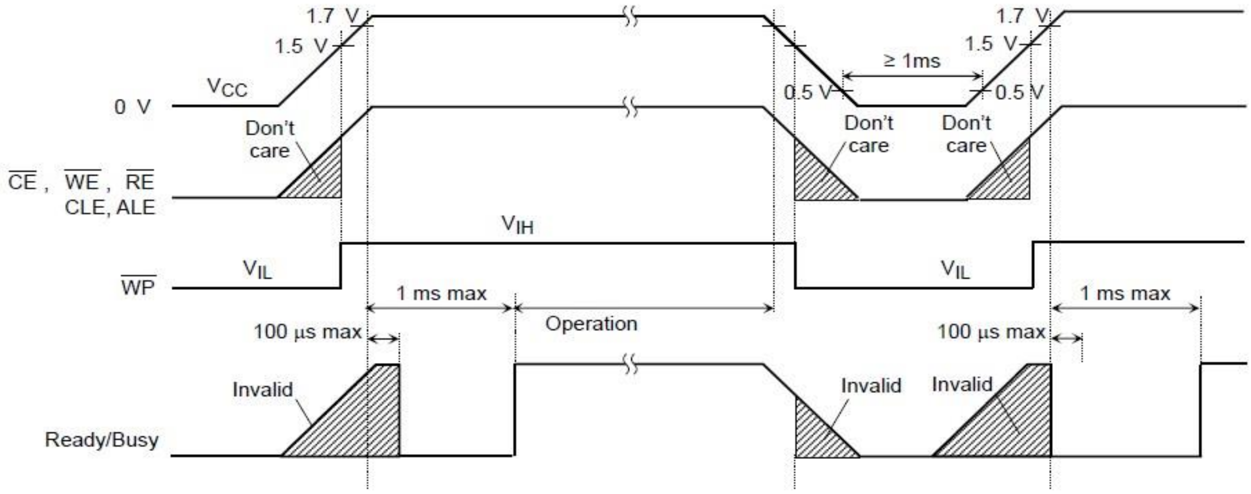
1.13. APPLICATION NOTES AND COMMENTS

(1) Power-on/off sequence:

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

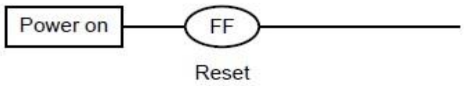
The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are FFh or 70h.

The $\overline{\text{WP}}$ signal is useful for protecting against data corruption at power-on/off.



(2) Power on Reset

The following sequence is necessary because some input signals may not be stable at power on.



(3) Prohibition of unspecified commands

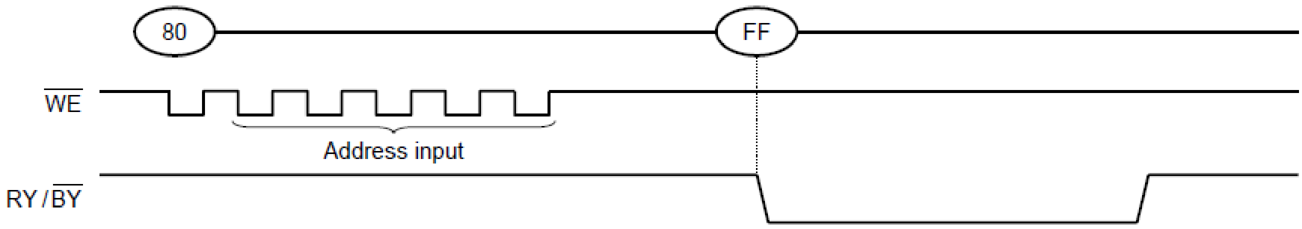
The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(4) Restriction of commands while in the Busy state

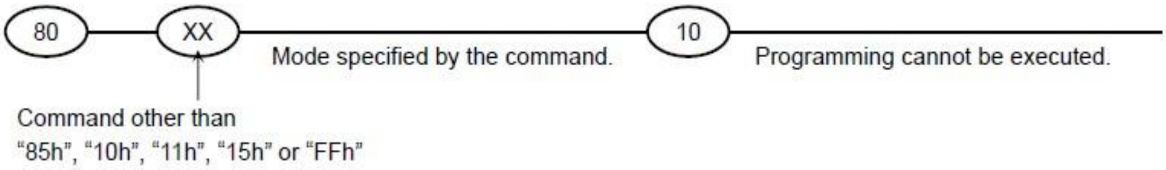
During the Busy state, do not input any command except 70h(71h) and FFh.

(5) Acceptable commands after Serial Input command “80h”

Once the Serial Input command “80h” has been input, do not input any command other than the Column Address Change in Serial Data Input command “85h”, Auto Program command “10h”, Multi Page Program command “11h”, Auto Program with Data Cache Command “15h”, or the Reset command “FFh”.

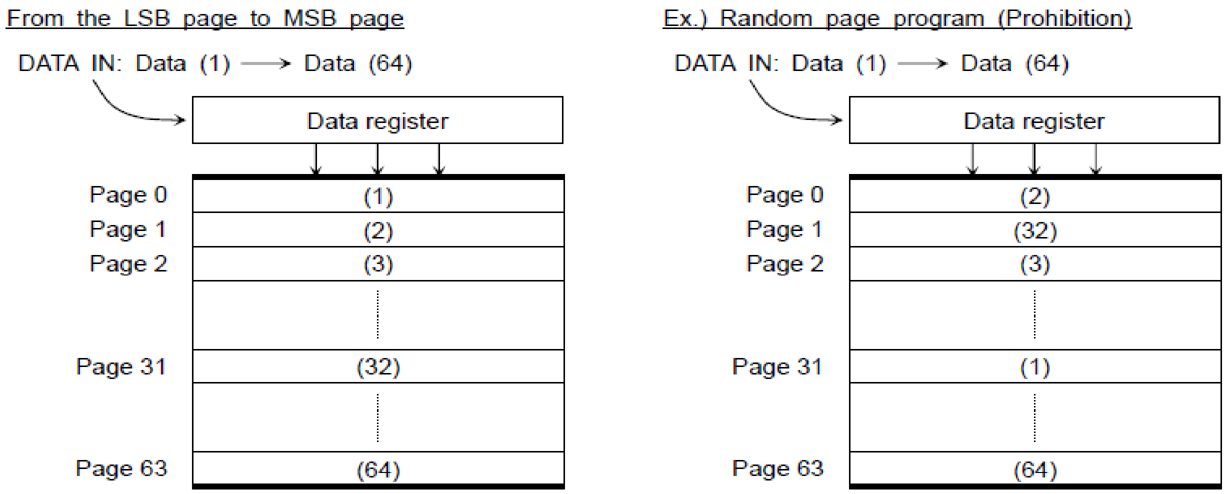


If a command other than “85h” , “10h” , “11h” , “15h” or “FFh” is input, the Program operation is not performed and the device operation is set to the mode which the input command specifies.

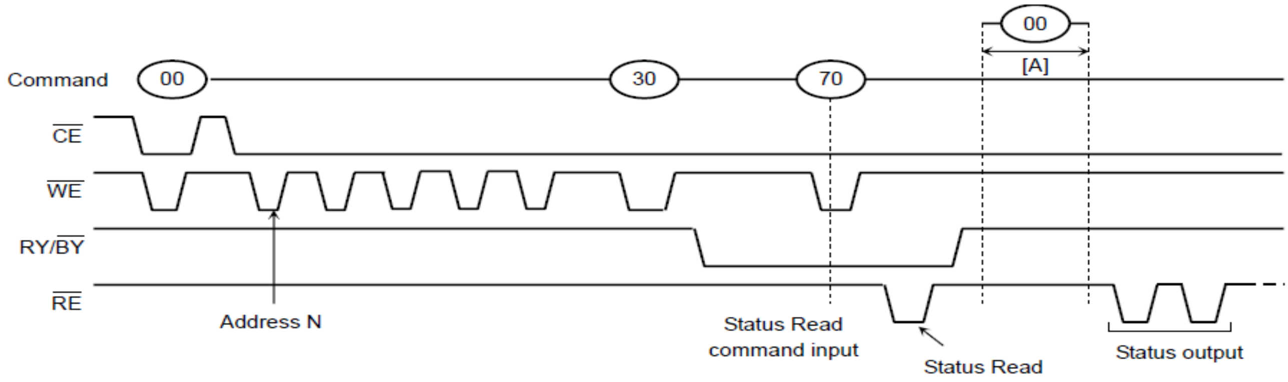


(6) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

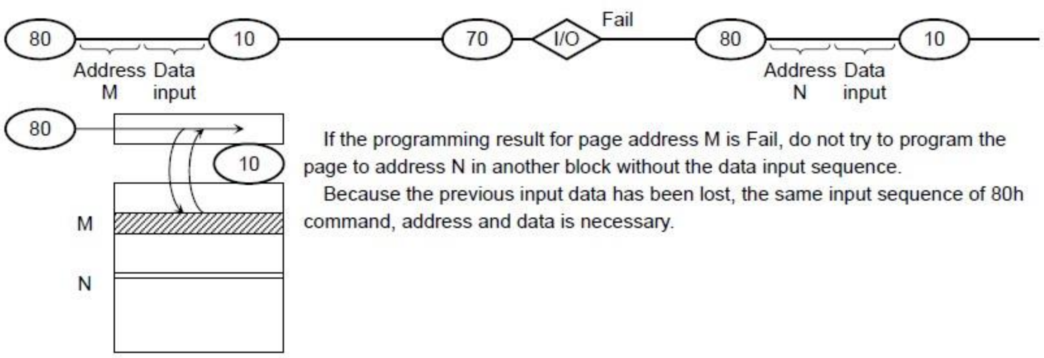


(7) Status Read during a Read operation



The device status can be read out by inputting the Status Read command "70h" in Read mode. Once the device has been set to Status Read mode by a "70h" command, the device will not return to Read mode unless the Read command "00h" is inputted during [A]. If the Read command "00h" is inputted during [A], Status Read mode is reset, and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary.

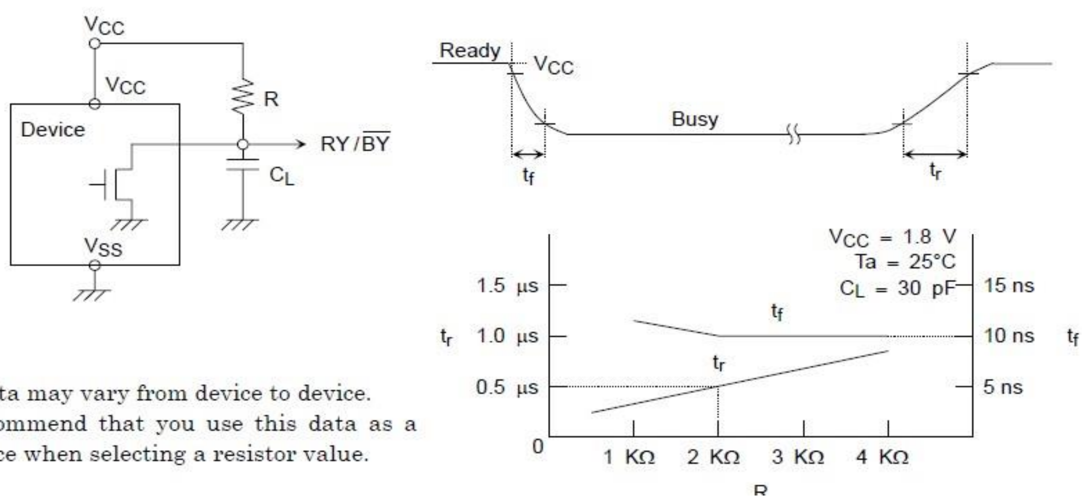
(8) Auto programming failure



If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence.
Because the previous input data has been lost, the same input sequence of 80h command, address and data is necessary.

(9) RY / $\overline{\text{BY}}$: termination for the Ready/Busy pin (RY / $\overline{\text{BY}}$)

A pull-up resistor needs to be used for termination because the RY / $\overline{\text{BY}}$ buffer consists of an open drain circuit.

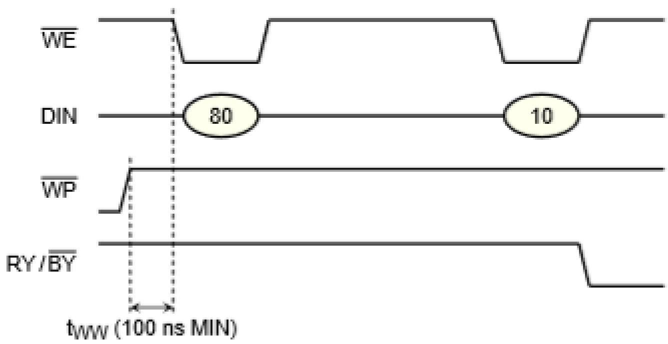


This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.

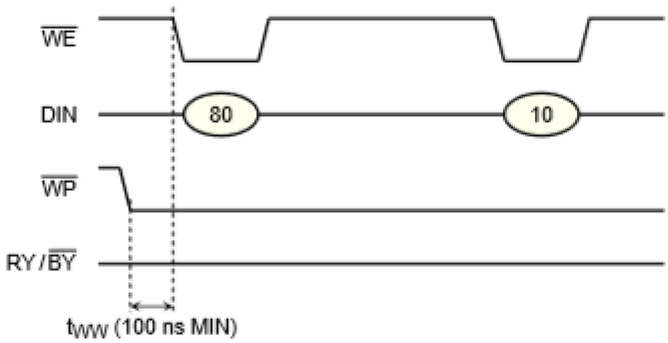
(10) Note regarding the WP# signal

The Erase and Program operations are automatically reset when WP# goes Low. The operations are enabled and disabled as follows:

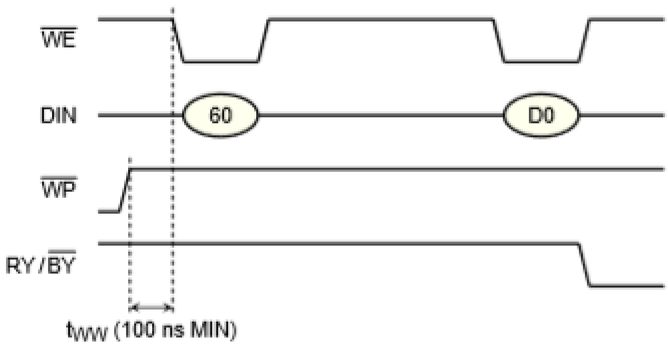
Enable Programming



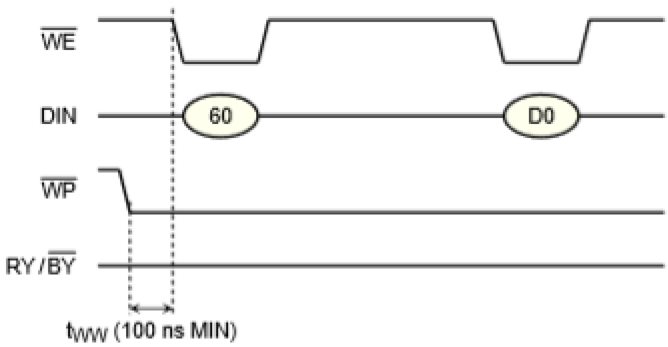
Disable Programming



Enable Erasing

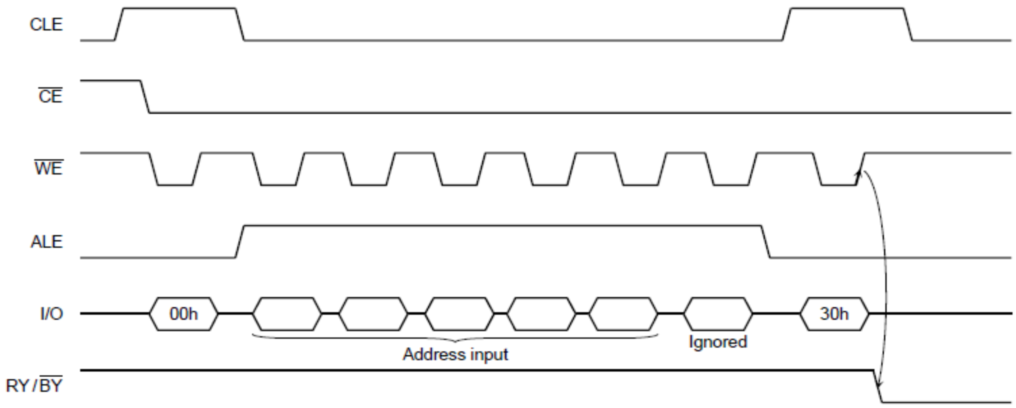


Disable Erasing

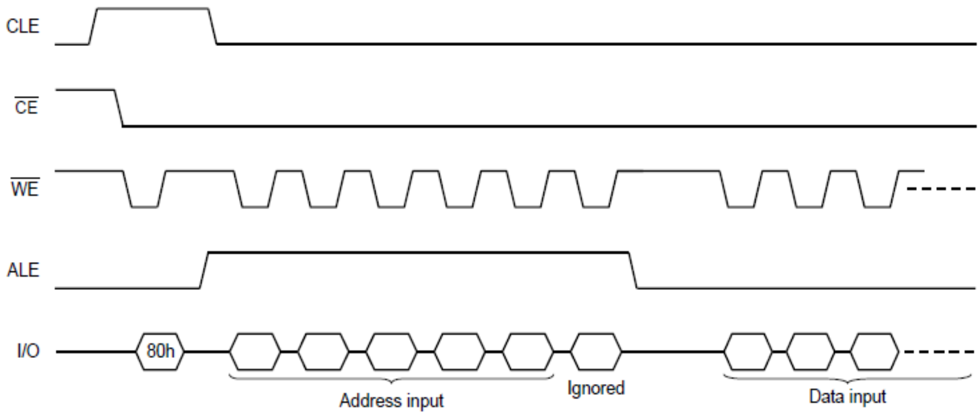


(11) When six address cycles are input

Although the device may read in a sixth address, it is ignored inside the chip. Read operation

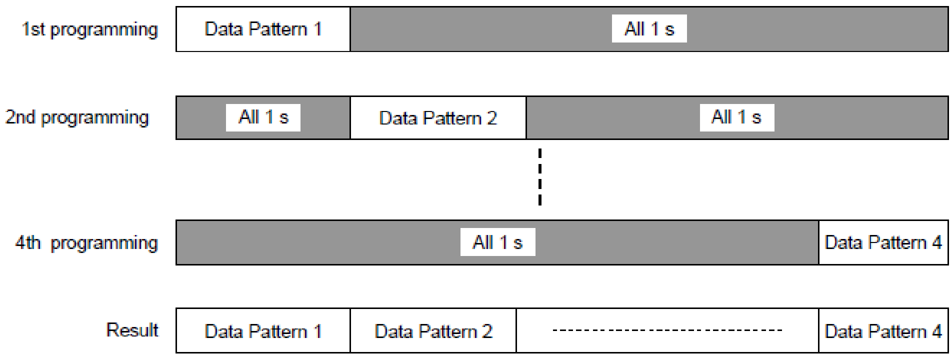


Program operation



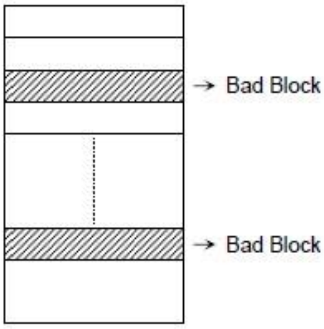
(12) Several programming cycles on the same page (Partial Page Program)

Each segment can be programmed individually as follows:



(13) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information if the information is erased.

Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

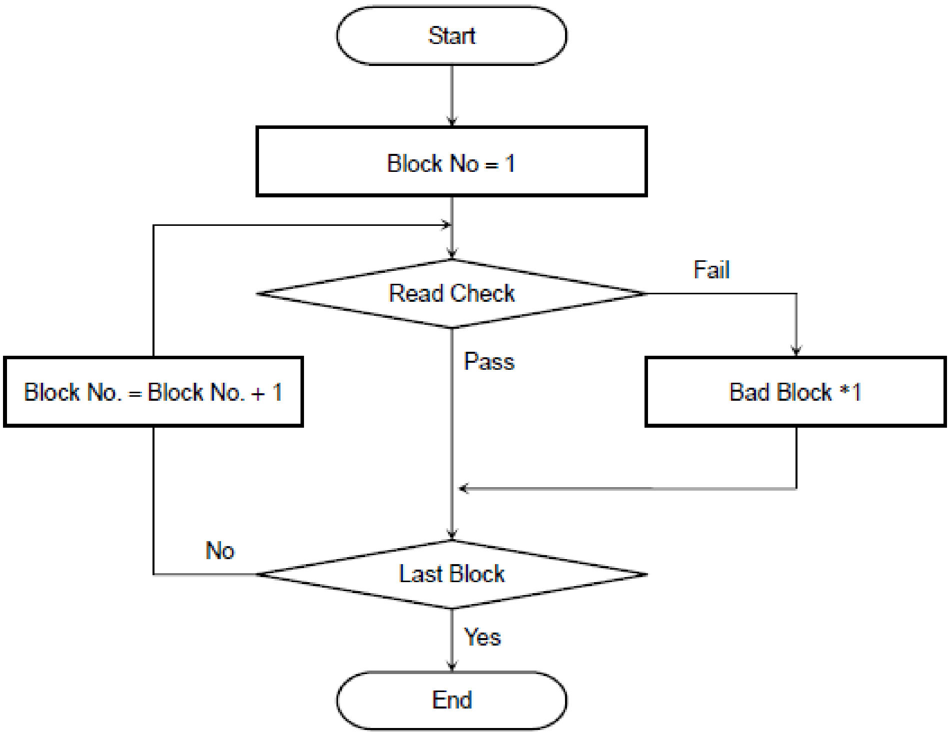
The number of valid blocks over the device lifetime is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	2008	—	2048	Block

1.14. Bad Block Test Flow

Regarding invalid blocks, bad block mark is in whole pages.

Please read one column of any page in each block. If the data of the column is 00(Hex), define the block as a bad block.



*1: No erase operation is allowed to detected bad blocks

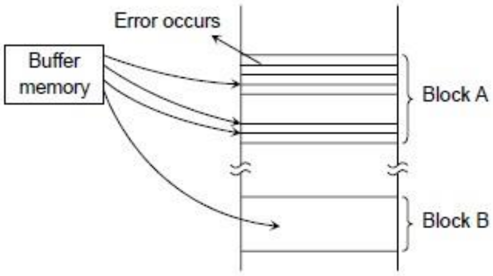
(14) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Read	Bit Error	ECC Correction / Block Refresh

- ECC: Error Correction Code. 8 bit correction per 544 Bytes is necessary.
- Block Replacement

Program



When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(15) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

(16) The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

(17) Reliability Guidance

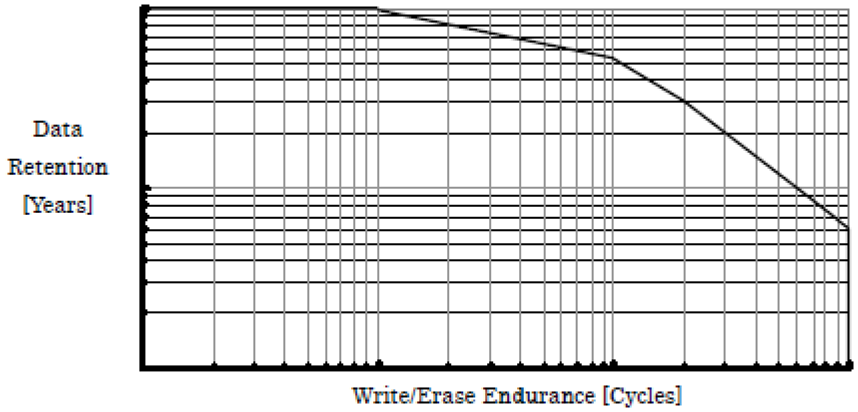
This reliability guidance is intended to notify some guidance related to using NAND flash with 8 bit ECC for each 544 bytes. For detailed reliability data, please refer to NAND’s reliability note. Although random bit errors may occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes may be recovered by a block erase.

ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

- **Write/Erase Endurance**

  Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.
- **Data Retention**

  The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again. Here is the combined characteristics image of Write/Erase Endurance and Data Retention.

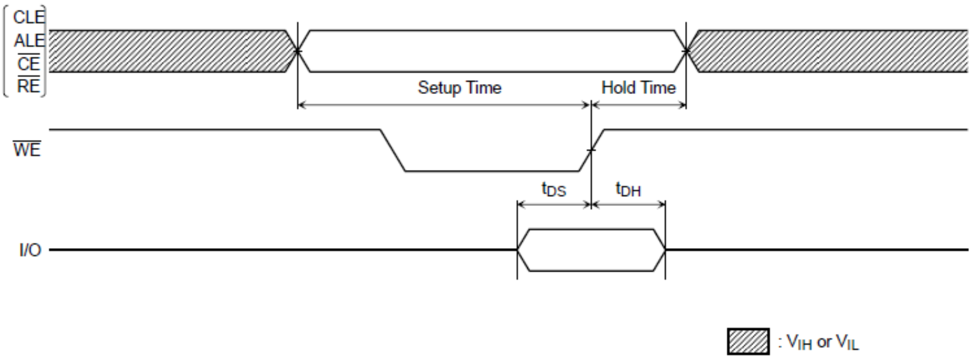


- **Read Disturb**

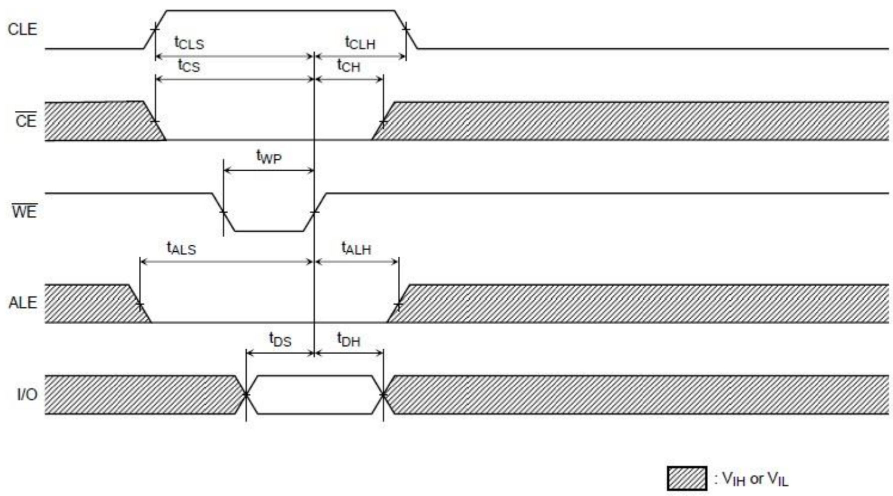
A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

1.15. Timing Diagrams

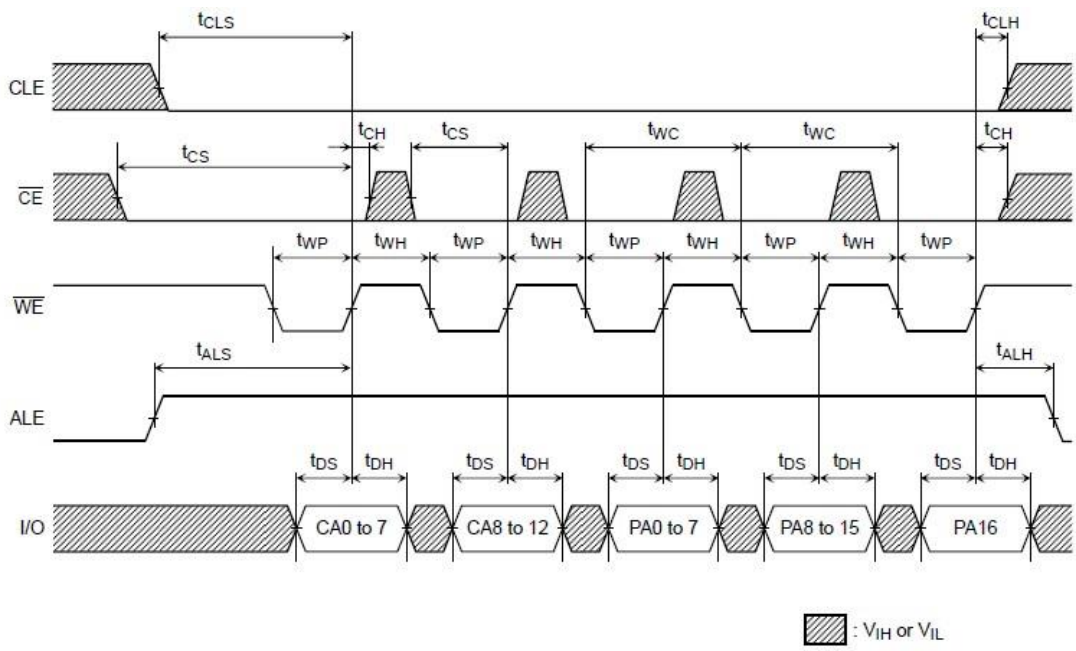
1.15.1. Latch Timing Diagram for Command/Address/Data



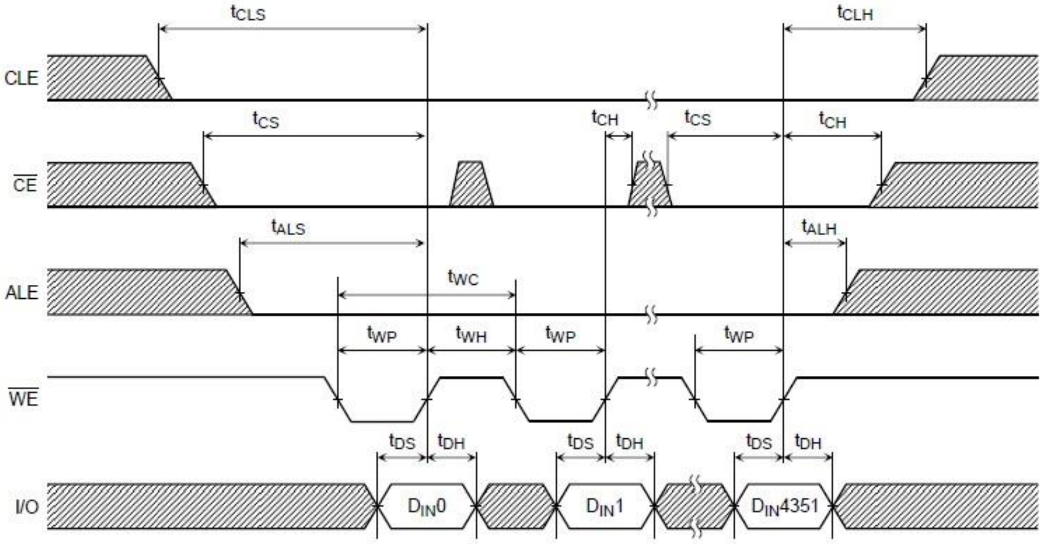
1.15.2. Command Input Cycle Timing Diagram



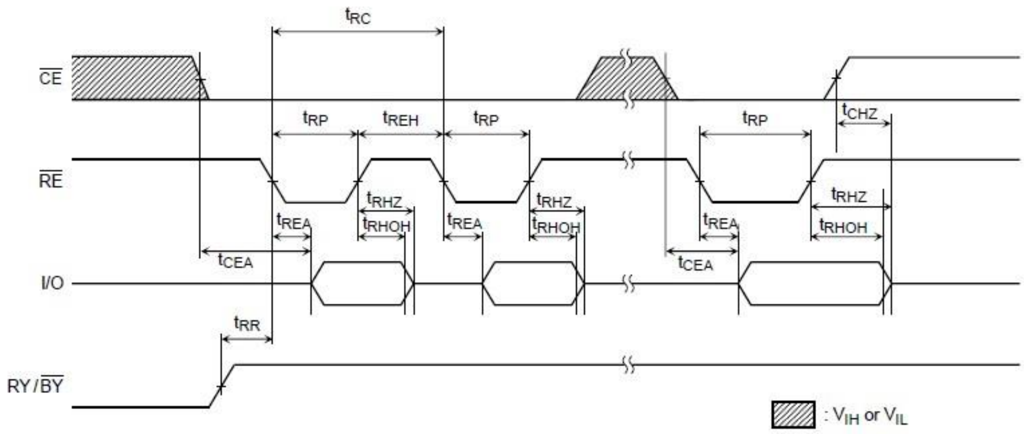
1.15.3. Address Input Cycle Timing Diagram



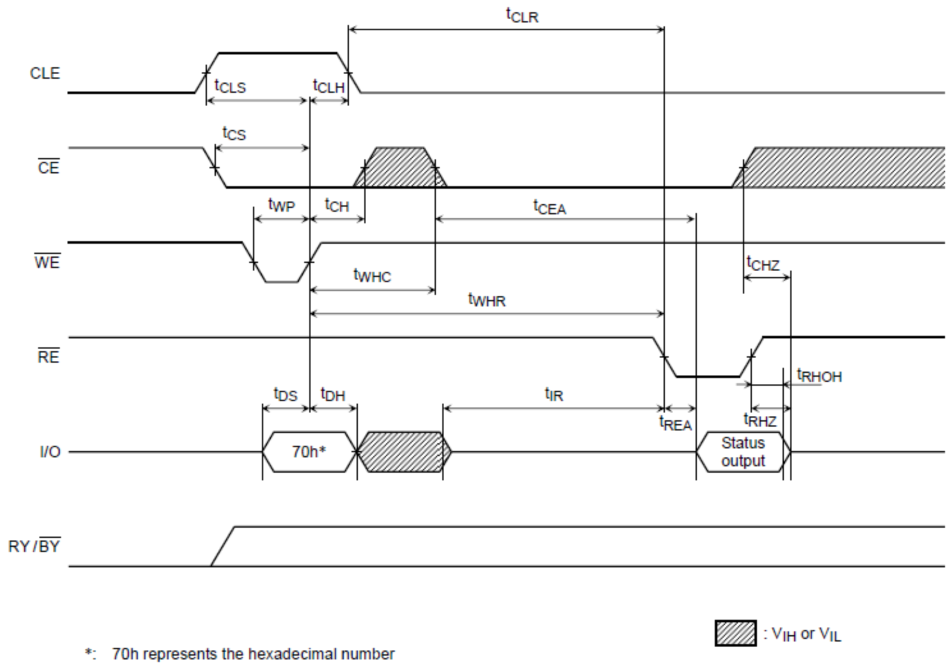
1.15.4. Data Input Cycle Timing Diagram



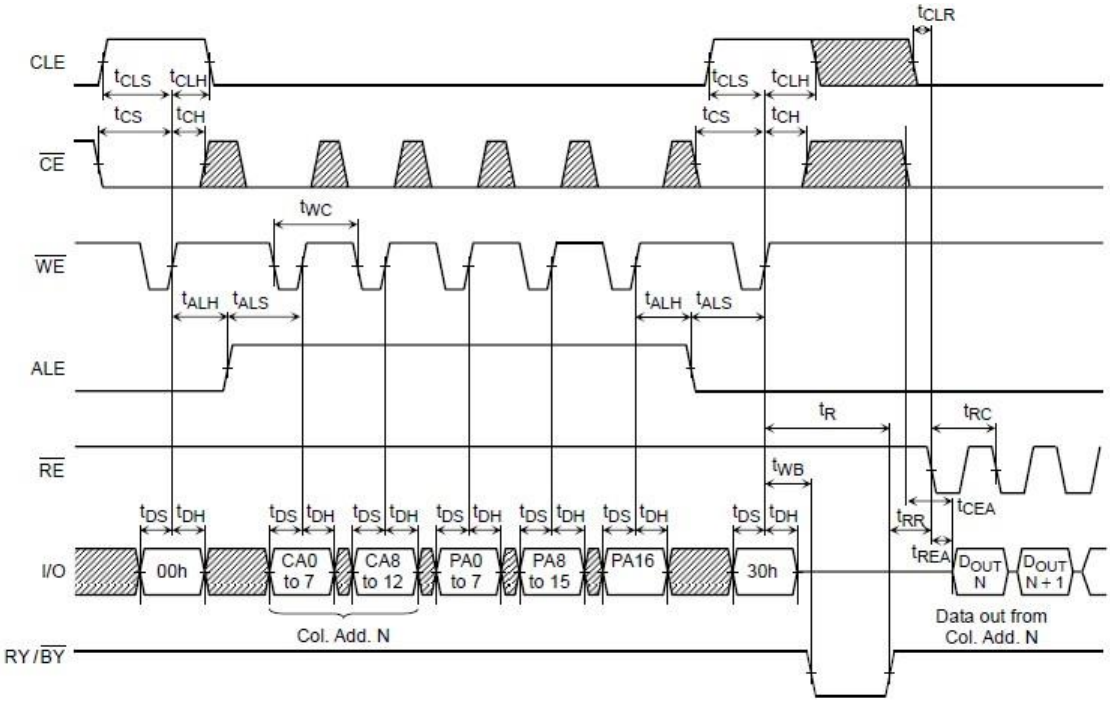
1.15.5. Serial Read Cycle Timing Diagram



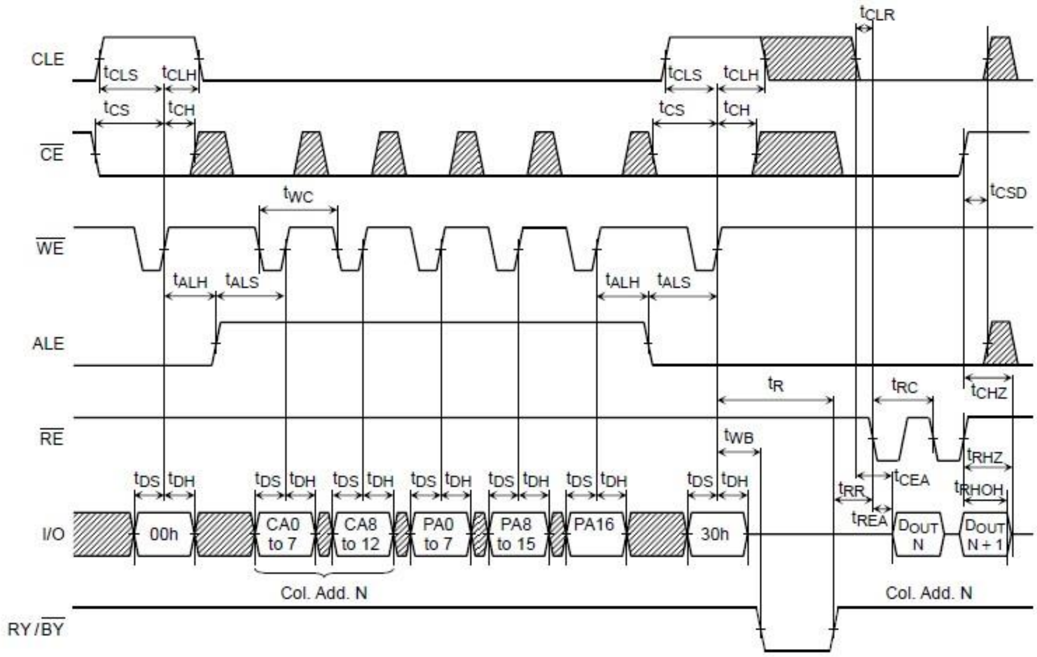
1.15.6. Status Read Cycle Timing Diagram



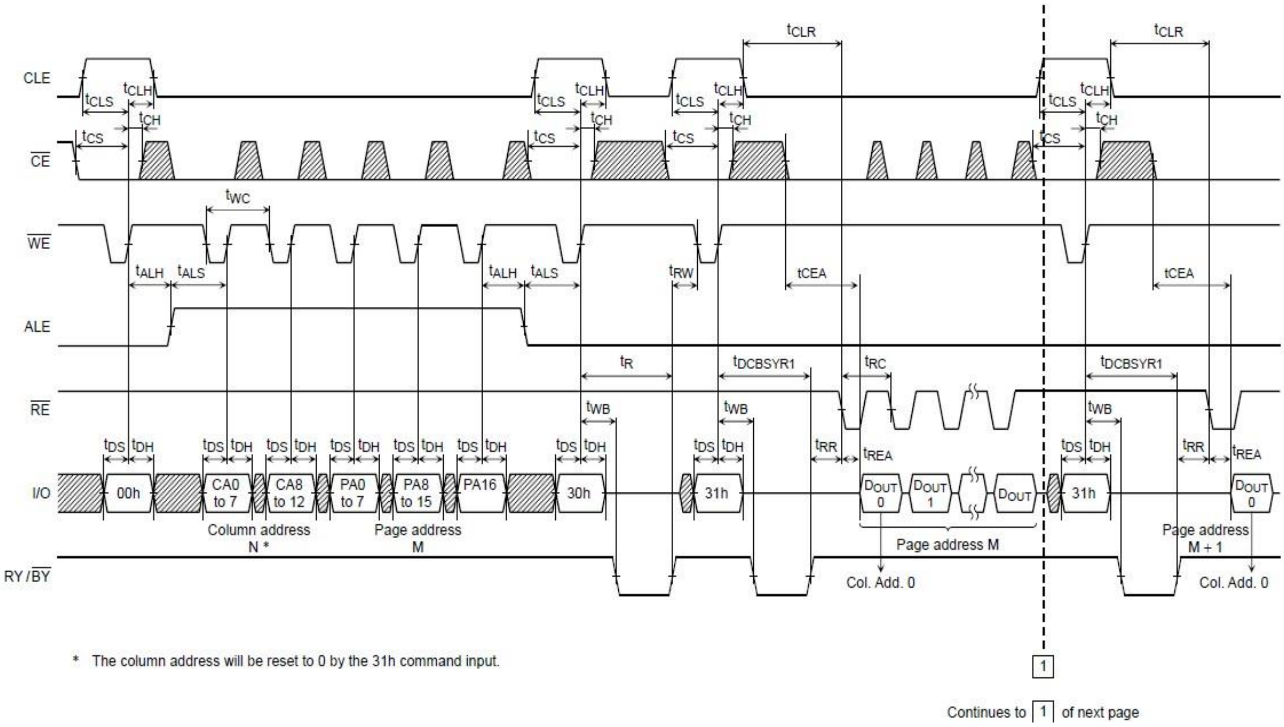
1.15.7. Read Cycle Timing Diagram



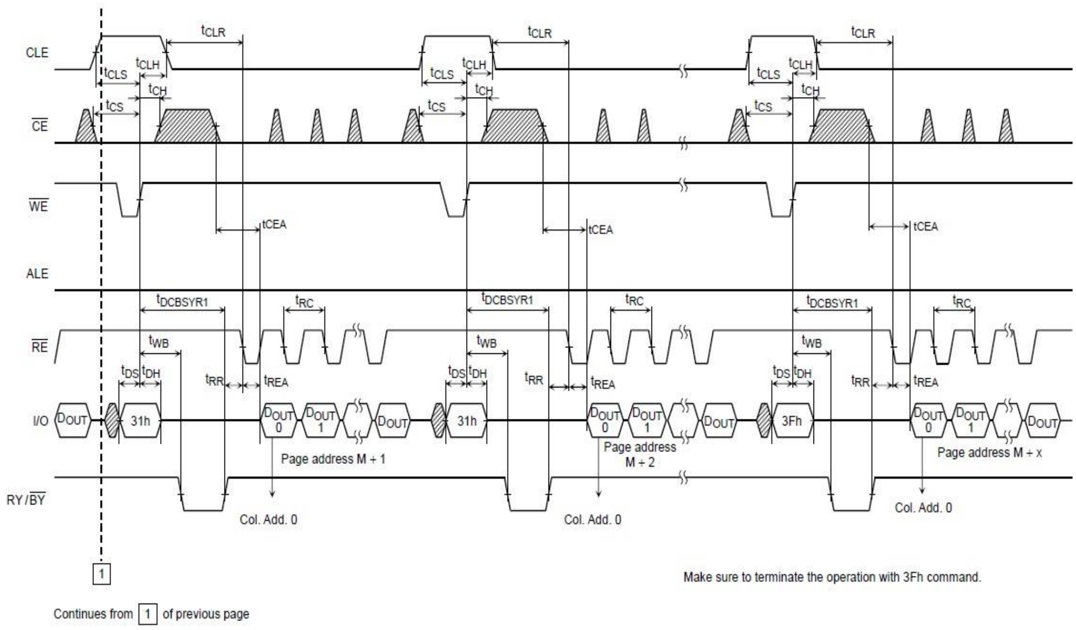
1.15.8. Read Cycle Timing Diagram: When Interrupted by /CE



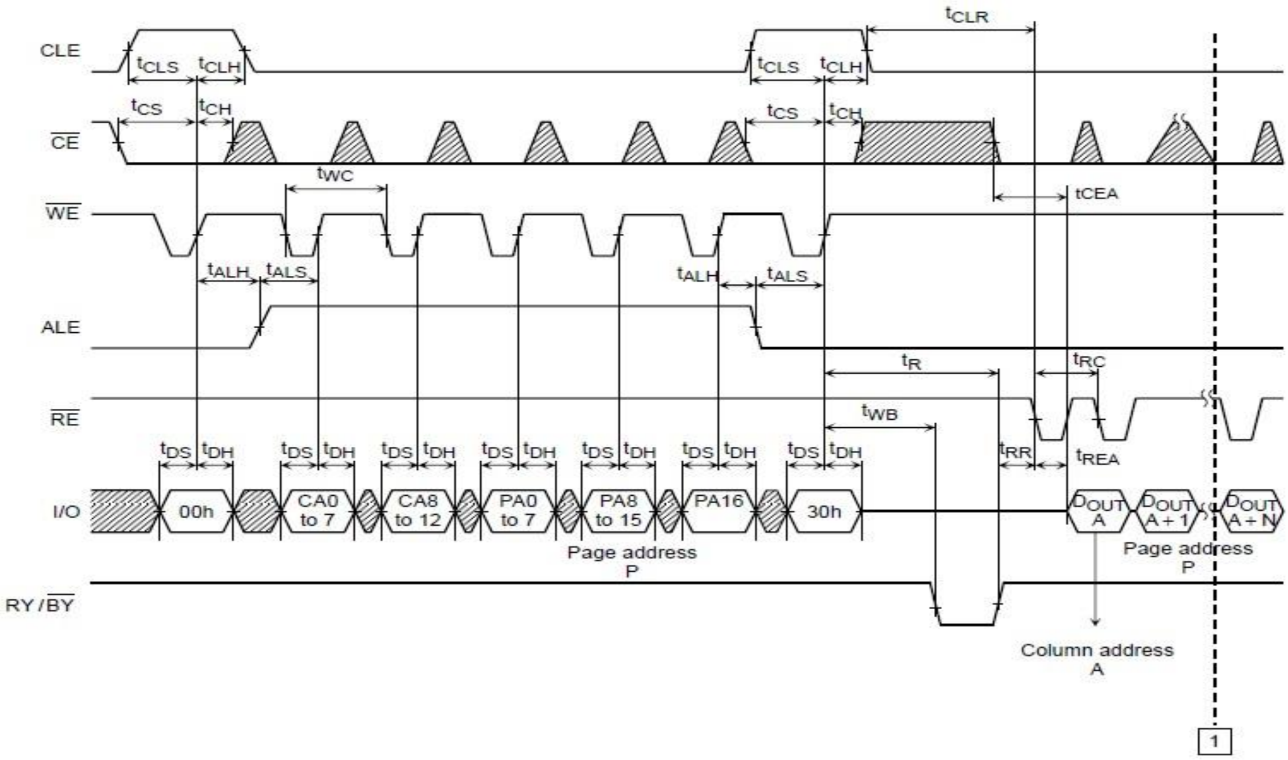
1.15.9. Read Cycle with Data Cache Timing Diagram (1/2)



Read Cycle with Data Cache Timing Diagram (2/2)



1.15.10. Column Address Change in Read Cycle Timing Diagram (1/2)



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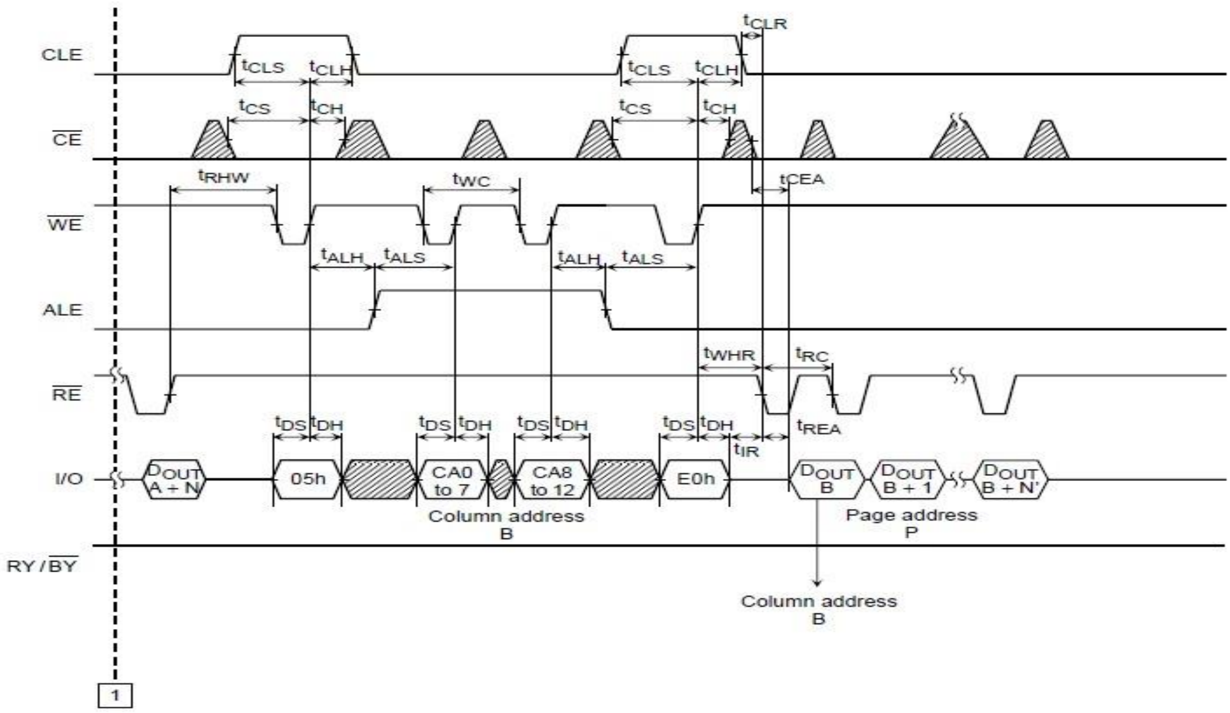
Column Address Change in Read Cycle Timing Diagram (2/2)



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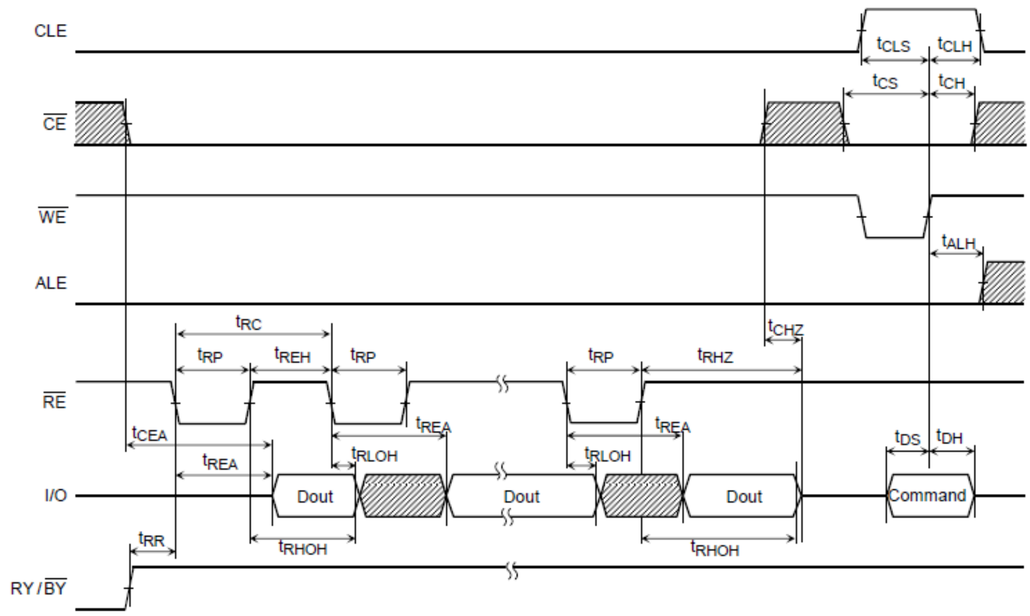
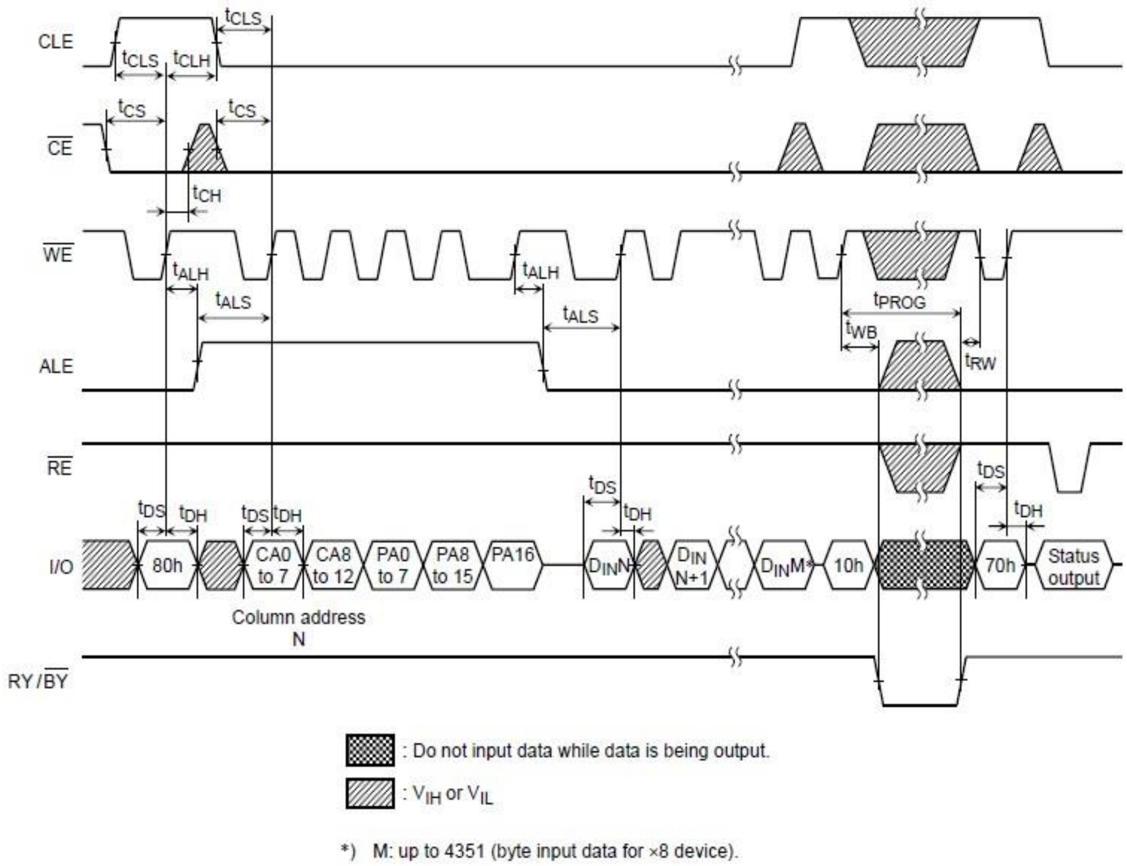
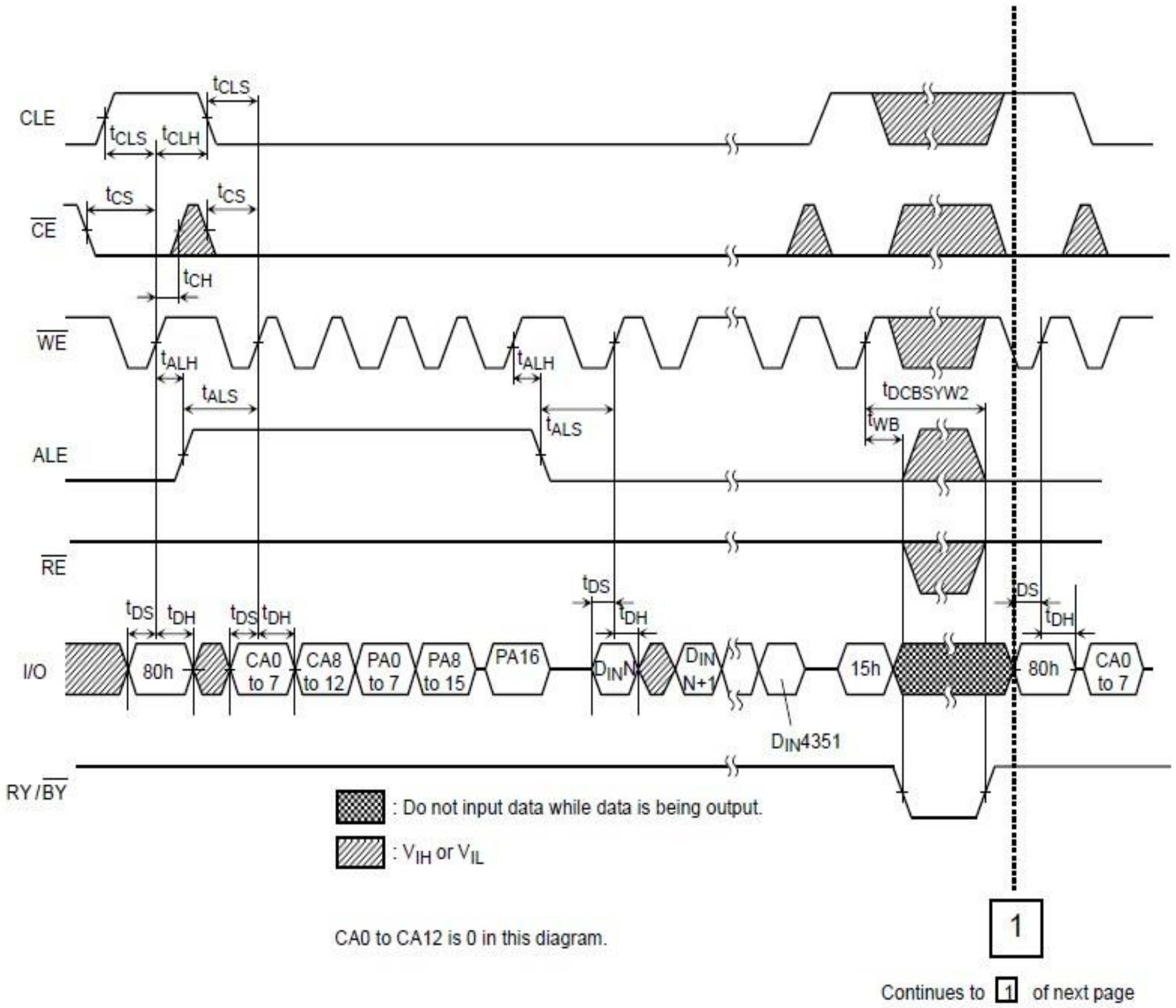
1.15.11. Data Output Timing Diagram



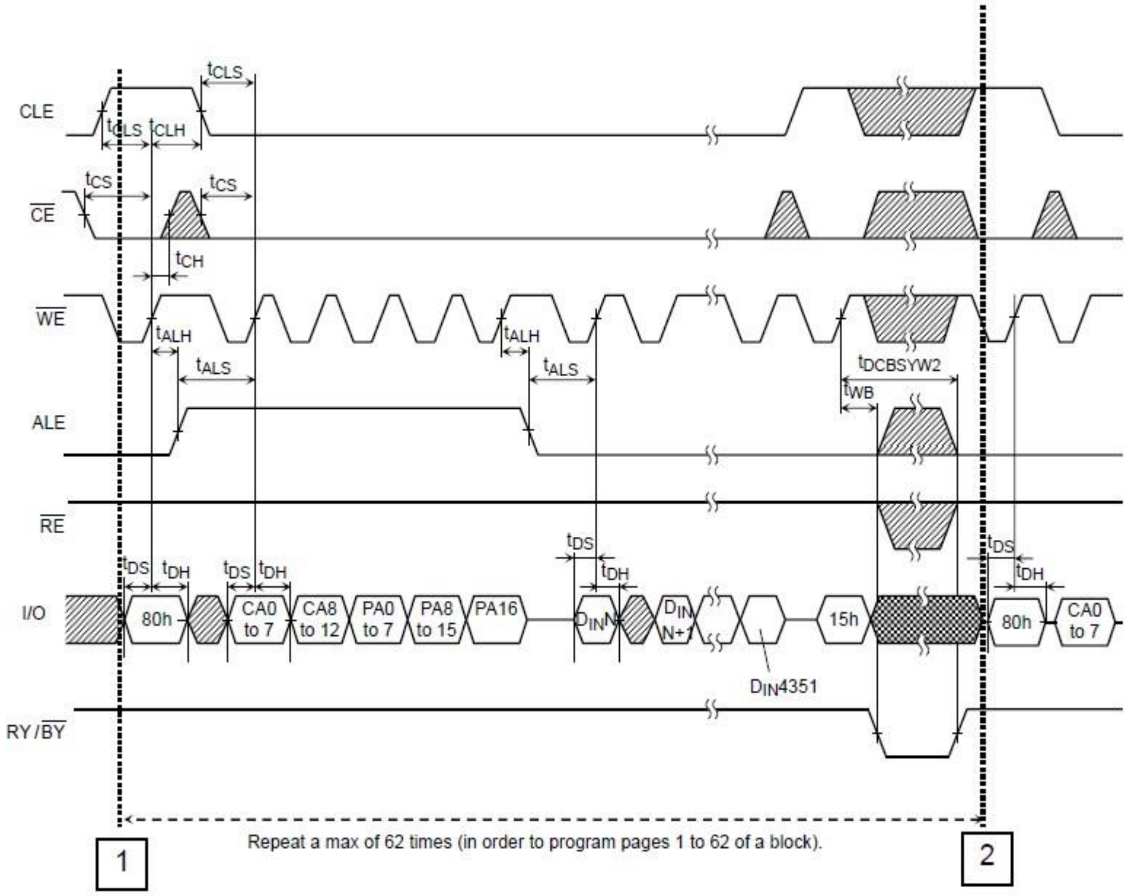
1.15.12. Auto-Program Operation Timing Diagram



1.15.13. Auto-Program Operation with Data Cache Timing Diagram (1/3)



Auto-Program Operation with Data Cache Timing Diagram (2/3)



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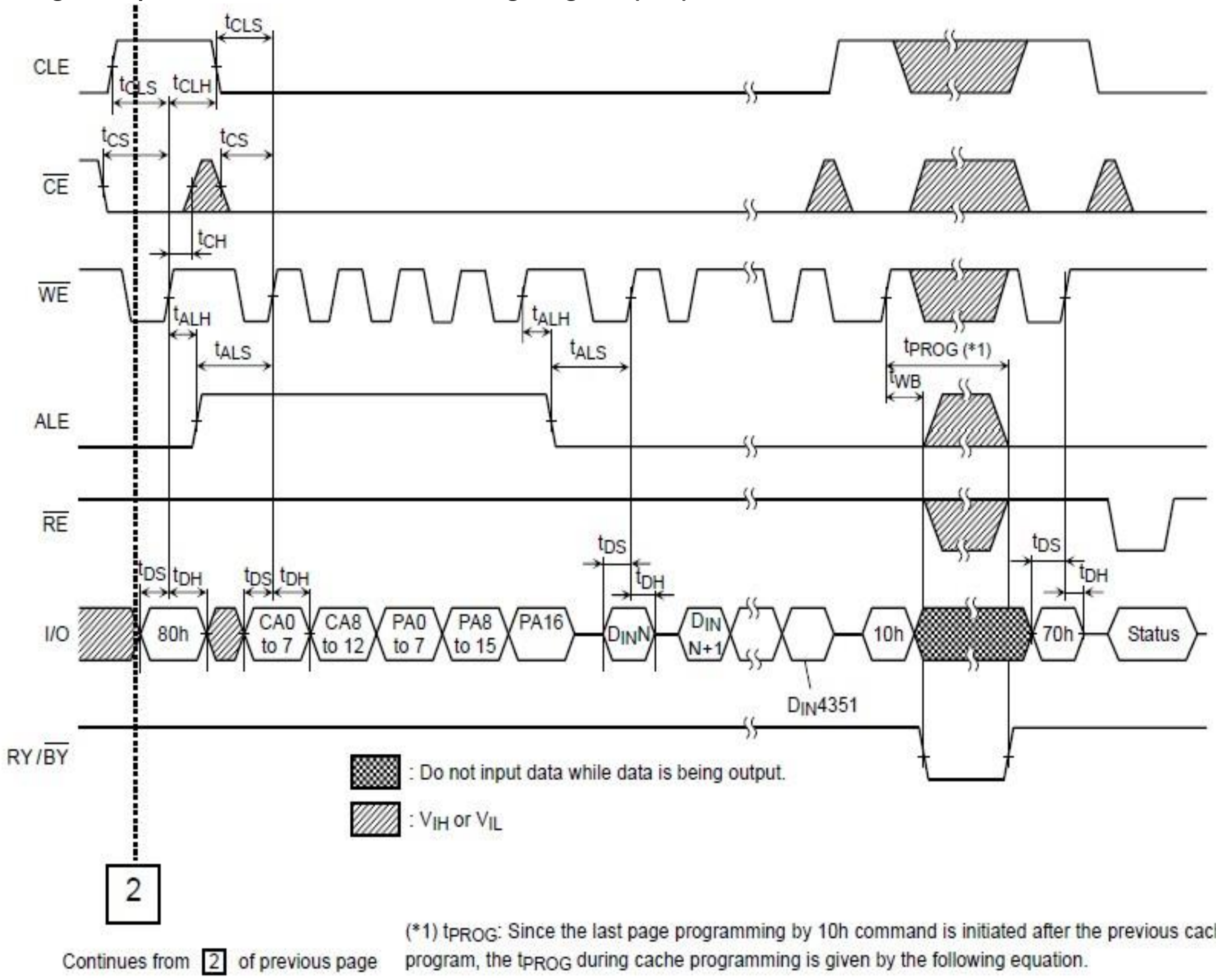
Auto-Program Operation with Data Cache Timing Diagram (3/3)



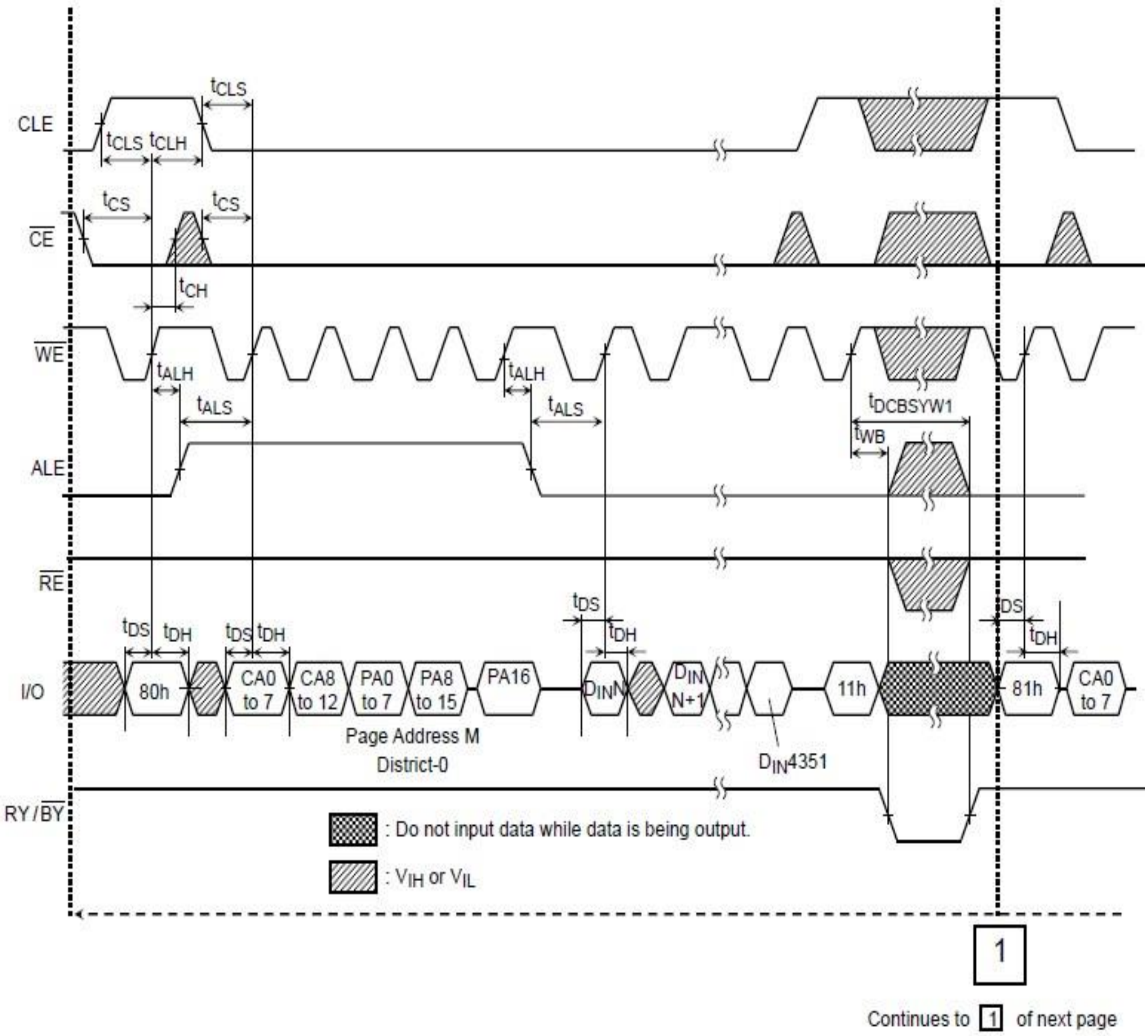
(*1) t_{PROG}: Since the last page programming by 10h command is initiated after the previous cache program, the t_{PROG} during cache programming is given by the following equation.

t_{PROG} = t_{PROG} of the last page + t_{PROG} of the previous page – A
A = (command input cycle + address input cycle + data input cycle time of the last page)

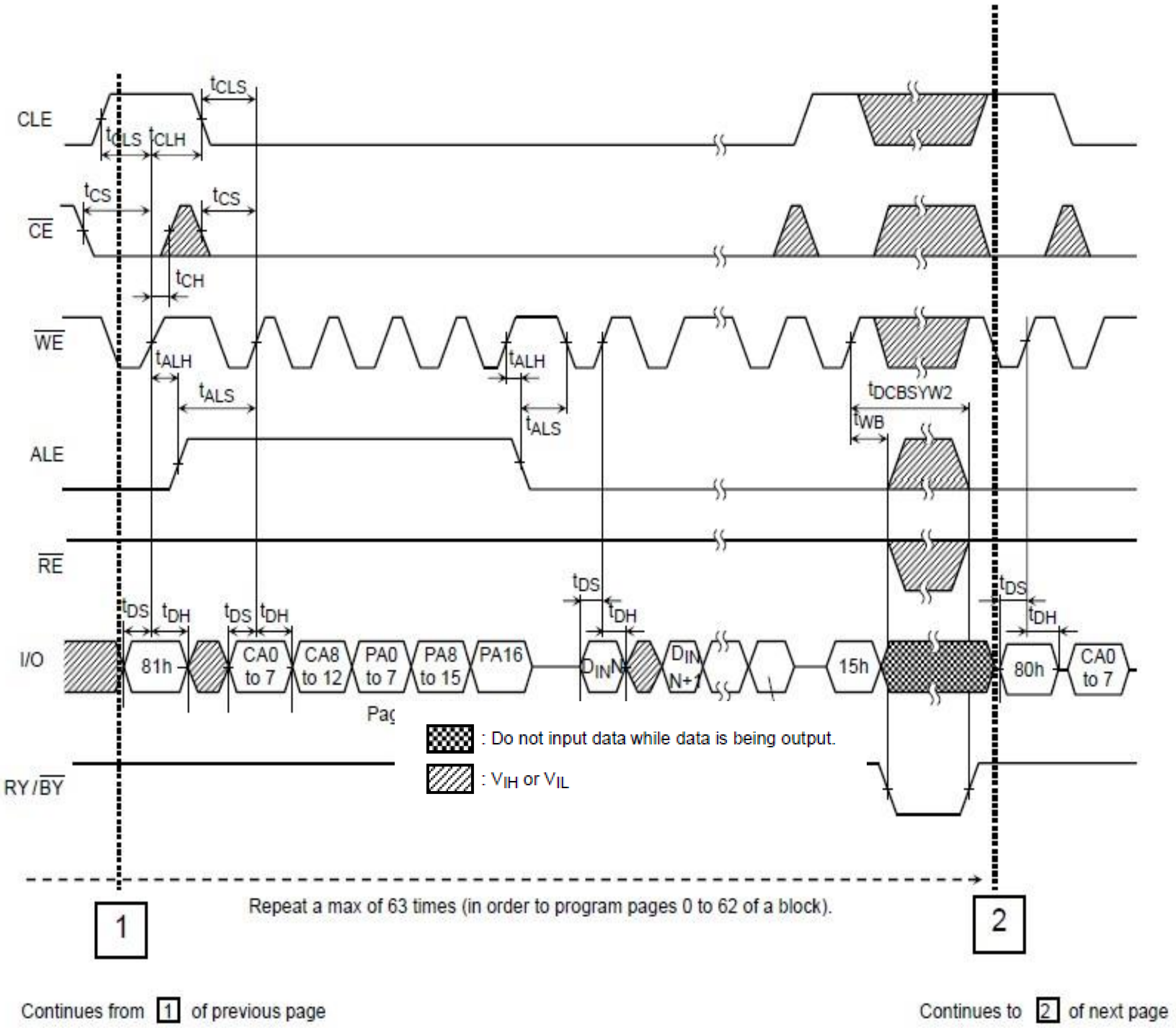
If "A" exceeds the t_{PROG} of previous page, t_{PROG} of the last page is t_{PROG} max.

(Note) Make sure to terminate the operation with 80h-10h- command sequence. If the operation is terminated by 80h-15h command sequence, monitor I/O5 (Ready / Busy) by issuing Status Read command (70h) and make sure the previous page program operation is completed. If the page program operation is completed issue FFh reset before next operation.

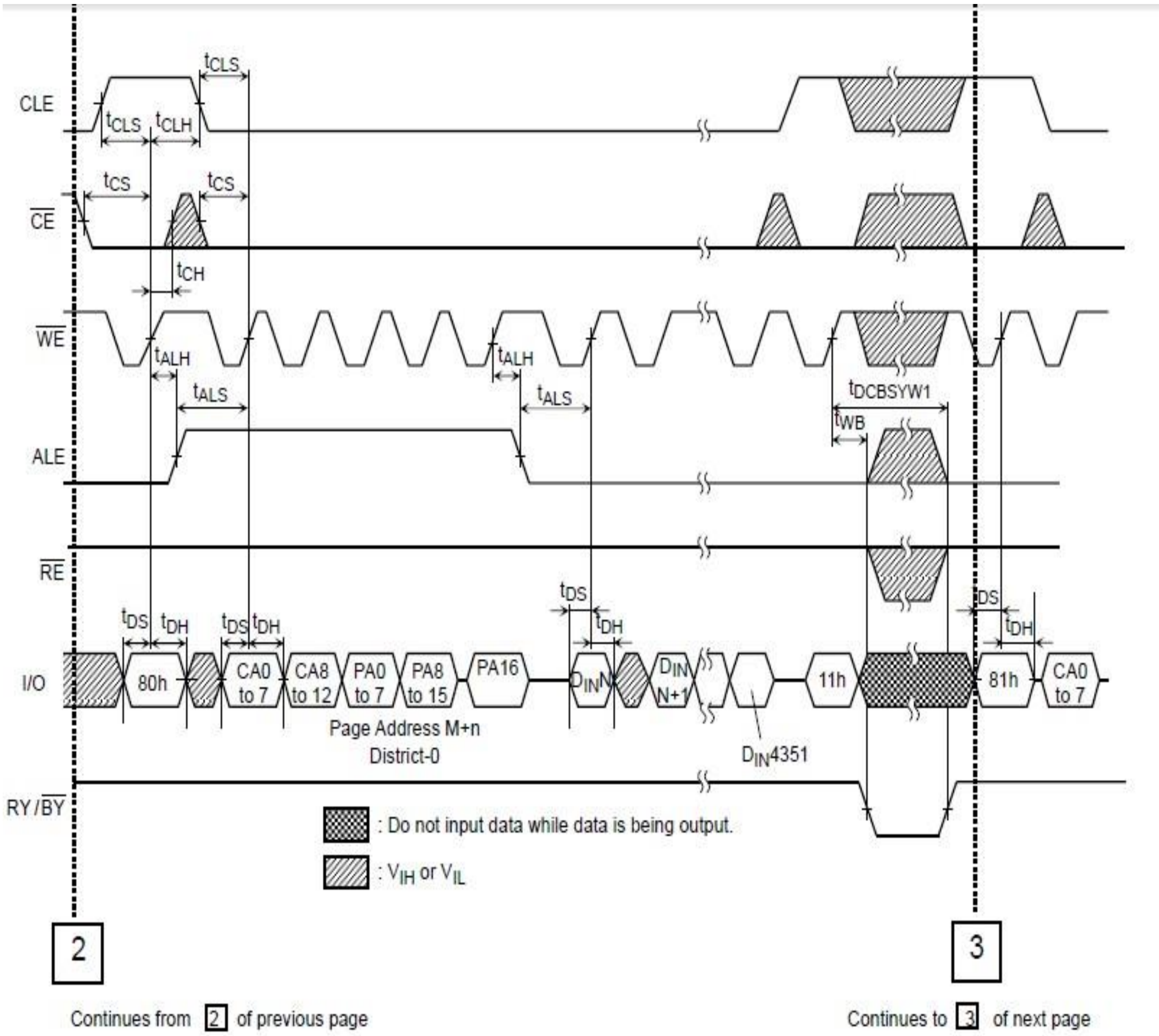
1.15.14. Multi-Page Program Operation with Data Cache Timing Diagram (1/4)



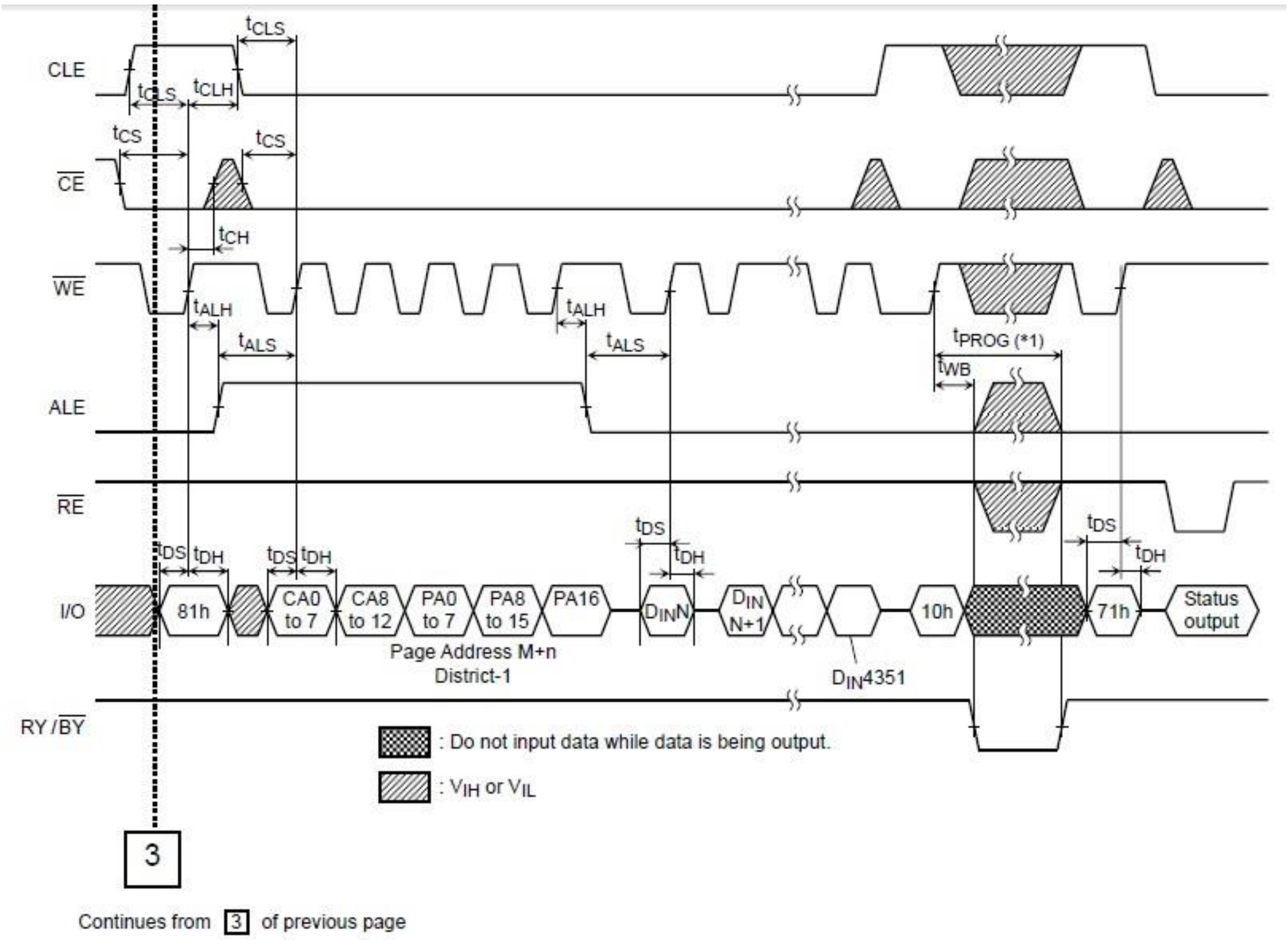
Multi-Page Program Operation with Data Cache Timing Diagram (2/4)



Multi-Page Program Operation with Data Cache Timing Diagram (3/4)



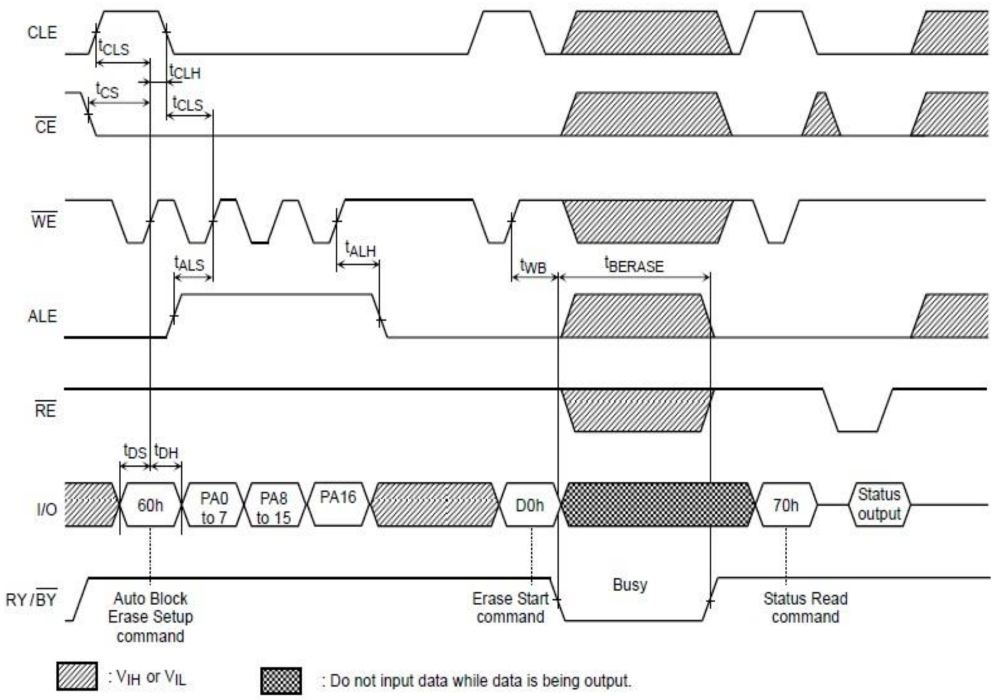
Multi-Page Program Operation with Data Cache Timing Diagram (4/4)



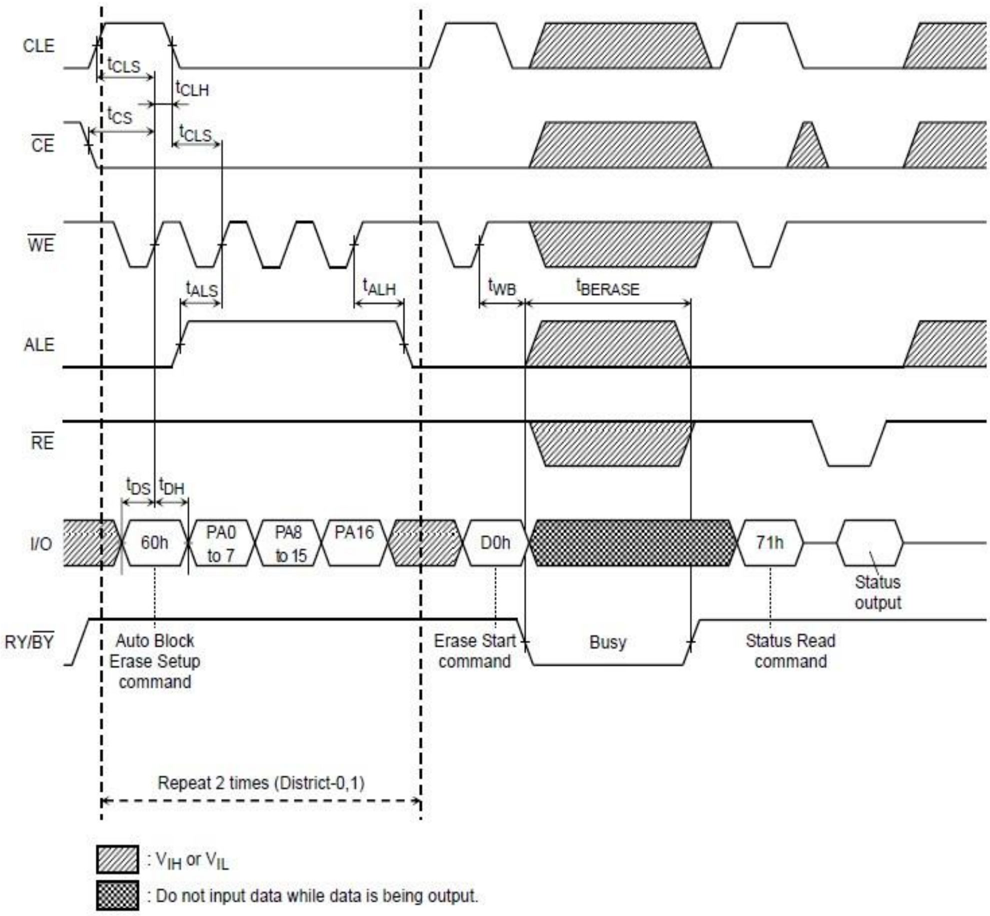
(*1) tPROG: Since the last page programming by 10h command is initiated after the previous cache program, the tPROG during cache programming is given by the following equation. tPROG = tPROG of the last page + tPROG of the previous page – AA = (command input cycle + address input cycle + data input cycle time of the last page) If "A" exceeds the tPROG of previous page, tPROG of the last page is tPROG max.

(Note) Make sure to terminate the operation with 81h-10h- command sequence. If the operation is terminated by 81h-15h command sequence, monitor I/O 5 (Ready / Busy) by issuing Status Read command (70h) and make sure the previous page program operation is completed. If the page program operation is completed issue FFh reset before next operation.

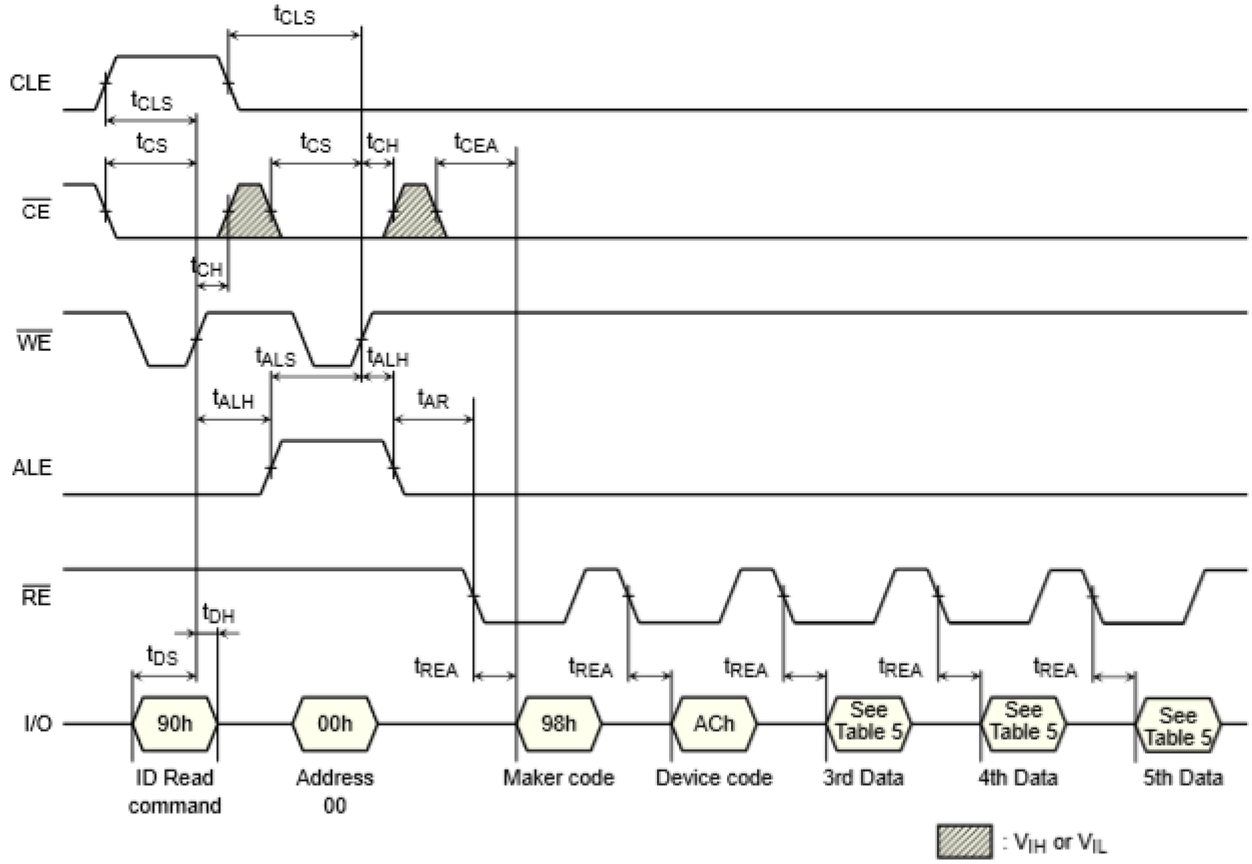
1.15.15. Auto Block Erase Timing Diagram



1.15.16. Multi Block Erase Timing Diagram



1.15.17. ID Read Operation Timing Diagram



2. Low power DDR2 SDRAM Part

2.1 General Description

The low power DDR2 is a high-speed Low Power double data rate synchronous dynamic random access memory (LPDDR2 SDRAM), An access to the LPDDR2 SDRAM is burst oriented. Consecutive memory location in one page can be accessed at a burst length of 2, 4, 8 and 16 when a bank and row is selected by an ACTIVE command. Column addresses are automatically generated by the LPDDR2 SDRAM internal counter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the pre-charging time. By setting programmable Mode Registers, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. The device supports special low power functions such as Partial Array Self Refresh (PASR) and Automatic Temperature Compensated Self Refresh (ATCSR).

2.2 Electrical Specifications

- All voltages are referenced to each GND level (VSS, VSSCA, and VSSQ).
- Execute power-up and Initialization sequence before proper device operation can be achieved.

2.2.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on any pin relative to VSSCA, VSSQ	VT	-0.4 to +1.6	V	
Power supply voltage (core power1) relative to VSS	VDD1	-0.4 to +2.3	V	
Power supply voltage (core power2) relative to VSS	VDD2	-0.4 to +1.6	V	
Power supply voltage for command, address relative to VSS-	VDDCA	-0.4 to +1.6	V	
Power supply voltage for output relative to VSSQ	VDDQ	-0.4 to +1.6	V	
Storage temperature	Tstg	-55 to +125	°C	1
Power dissipation	PD	1.0	W	
Short circuit output current	IOUT	50	mA	

Notes:

Storage temperature the case surface temperature on the center/top side of the DRAM.

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

2.2.2 Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	TC	-25 to +85	°C	1
Extended Operating case temperature	TC	+85 to +105	°C	2

Notes:

Operating temperature is the case surface temperature on the center/top side of the DRAM. Refer to MR4 programing table for Temperature Sensor de-rating & refresh rate numbers.

2.2.3 Recommended DC Operating Conditions

(TC = -25°C to +85°C)

<table>
<tr><th colspan="2">Parameter</th><th>Symbol</th><th>min.</th><th>typical</th><th>max</th><th>Unit</th><th>Note</th></tr>
<tr><td rowspan="8">Supply voltage</td><td rowspan="2">core power1</td><td>VDD1</td><td>1.7</td><td>1.8</td><td>1.95</td><td>V</td><td>1</td></tr>
<tr><td>VSS</td><td>0</td><td>0</td><td>0</td><td>V</td><td></td></tr>
<tr><td rowspan="2">core power2</td><td>VDD2</td><td>1.14</td><td>1.2</td><td>1.3</td><td>V</td><td>1</td></tr>
<tr><td>VSS</td><td>0</td><td>0</td><td>0</td><td>V</td><td></td></tr>
<tr><td rowspan="2">for command, ad-dress</td><td>VDDCA</td><td>1.14</td><td>1.2</td><td>1.3</td><td>V</td><td>1</td></tr>
<tr><td>VSSCA</td><td>0</td><td>0</td><td>0</td><td>V</td><td></td></tr>
<tr><td rowspan="2">for output</td><td>VDDQ</td><td>1.14</td><td>1.2</td><td>1.3</td><td>V</td><td>1</td></tr>
<tr><td>VSSQ</td><td>0</td><td>0</td><td>0</td><td>V</td><td></td></tr>
</table>

Notes:

VDDQ tracks with VDD2, VDDCA tracks with VDD2. AC parameters are measured with VDD2, VDDCA and VDDQ tied together.

2.2.4 AC and DC Input Measurement Levels

[Refer to section 8 in JEDEC Standard No. 209-2E]

2.2.5 DC Characteristics 1

(TC = -25°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Test Condition	Symbol	Power Supply	Max DDR 1066 / DDR 933 / DDR 800 / DDR 667 / DDR 533 / DDR 400 / DDR 333	Unit
Operating one bank active-precharge current	tCK = tCK(min); tRC = tRC(min); CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD01	VDD1	8	mA
		IDD02	VDD2	40	mA
		IDDOIN	VDDCA	5	mA
			VDDQ	1	mA
Idle power-down standby current	tCK = tCK(min); CKE is LOW; CS_n is HIGH; all banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD2P1	VDD1	0.4	mA
		IDD2P2	VDD2	2	mA
		IDD2PIN	VDDCA	0.1	mA
			VDDQ	0.1	mA
Idle power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is LOW;CS_n is HIGH; all banks idle; CA bus inputs are STABLE; Data bust inputs are STABLE;	IDD2PS1	VDD1	0.4	mA
		IDD2PS2	VDD2	2	mA
		IDD2PSIN	VDDCA	0.1	mA
			VDDQ	0.1	mA
Idle non power-down standby current	tCK = tCK(min); CKE is HIGH; CS_n is HIGH, all banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD2N1	VDD1	0.6	mA
		IDD2N2	VDD2	8	mA
		IDD2NIN	VDDCA	5	mA
			VDDQ	1	mA
Idle non power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is HIGH;CS_n is HIGH; all banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD2NS1	VDD1	0.6	mA
		IDD2NS2	VDD2	8	mA
		IDD2NSIN	VDDCA	5	mA
			VDDQ	1	mA
Active power-down standby current	tCK = tCK(min); CKE is LOW; CS_n is HIGH; one bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD3P1	VDD1	0.7	mA
		IDD3P2	VDD2	10	mA
		IDD3PIN	VDDCA	0.1	mA
			VDDQ	0.1	mA
Active power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is LOW; CS_n is HIGH; one bank active; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD3PS1	VDD1	0.7	mA
		IDD3PS2	VDD2	10	mA
		IDD3PSIN	VDDCA	0.1	mA
			VDDQ	0.1	mA
Active non power-down standby current	tCK = tCK(min); CKE is HIGH; CS_n is HIGH; one bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD3NI	VDD1	1	mA
		IDD3N2	VDD2	10	mA
		IDD3NIN	VDDCA	5	mA
			VDDQ	1	mA
Active non power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD3NS1	VDD1	1	mA
		IDD3NS2	VDD2	10	mA
		IDD3NSIN	VDDCA	5	mA
			VDDQ	1	mA

Parameter	Test Condition	Symbol	Power Supply	Max DDR 1066	DDR 933	DDR 800	DDR 667	DDR 533	DDR 400	DDR 333	Unit
Operating burst read current	tCK = tCK(min); CS_n is HIGH between valid commands; one bank active; BL = 4; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	IDD4R1	VDD1	2							mA
		IDD4R2	VDD2	150	140	120	110	90	70	60	mA
		IDD4RIN	VDDCA	5							mA
		IDD4RQ	VDDQ	140	120	100	80	60	45	30	mA
Operating burst write current	tCK = tCK (min); CS_n is HIGH between valid commands; one bank active; BL = 4; WL = WL(min);CA bus inputs are SWITCHING; 50% data change each burst transfer	IDD4W1	VDD1	2							mA
		IDD4W2	VDD2	140	120	100	90	80	70	60	mA
		IDD4WIN	VDDCA	5*1							mA
			VDDQ	12*1							mA
All Bank Auto Refresh Burst Current	tCK = tCK (min); CS_n is HIGH between valid commands; tRC = tRFCab(min); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD51	VDD1	22							mA
		IDD52	VDD2	89							mA
		IDD5IN	VDDCA	3							mA
			VDDQ	0.625							mA
All Bank Auto Refresh Average Current	tCK = tCK(min); CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are SWITCHING; Data bus inputsa are STABLE	IDD5ab1	VDD1	1							mA
		IDD5ab2	VDD2	6							mA
		IDD5abIN	VDDCA	3							mA
			VDDQ	0.625							mA
Per Bank Auto Refresh Average Current	tCK = tCK(min); CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are SWITCHING; Data bus inputsa are STABLE	IDD5pb1	VDD1	1							mA
		IDD5pb2	VDD2	6							mA
		IDD5pdIN	VDDCA	3							mA
			VDDQ	0.625							mA
Self Refresh Current (Standard Tempera-ture Range: -30°C to 85°C)	CK_t = LOW; CK_c = HIGH; CKE is LOW;CA bus inputs are STABLE; Data bus inputs are STABLE; Maximum 1 x Self-refresh rate	IDD61	VDD1	563							μA
		IDD62	VDD2	2000							μA
		IDD6IN	VDDCA	63							μA
			VDDQ	8							μA
Deep Power Down Current (Standard Temperature Range: -30°C to 85°C)	CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD81	VDD1	10							μA
		IDD82	VDD2	31*2							μA
		IDD8IN	VDDCA	44							μA
			VDDQ	8							μA
Self Refresh Current (Extended Tempera-ture Range: +85°C to 105°C)	CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD6ET1	VDD1	2000							μA
		IDD6ET2	VDD2	3000							μA
		IDD6ETIN	VDDCA	63							μA
			VDDQ	31							μA
Deep Power Down Current (Extended Temperature Range: +85°C to 105°C)	CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD8ET1	VDD1	31							μA
		IDD8ET2	VDD2	63							μA
		IDD8ETIN	VDDCA	63							μA
			VDDQ	31							μA

Note :

1. These numbers are under 3sigma(FF corner) worst case numbers which are higher than typical production window.Typical production window is expected to be similar to the following 2sigma table:

Symbol	Max	Unit
IDD2P2	0.9	mA
IDD2PS2	0.9	mA
IDD2N2	4	mA
IDD2NS2	4	mA
IDD3P2	5.5	mA
IDD3PS2	5.5	mA
IDD3N2	5.5	mA
IDD3NS2	5.5	mA

2. Operating burst write VDDQ current is 12mA because all DQ & DQS input buffers run on VDDQ supply. Whereas VDDCA current is smaller because only the CA & control input buffers run on VDDCA Supply.

3. Deep sleep VDD2 current is higher. This is TBD.

2.2.6 Advanced Data Retention Current (Self-refresh current)

(TC = -25°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter		Symbol	Supply	Max	Unit	Test Condition
-30°C ≤ TC ≤ +25°C CKE ≤ 0.2V	Full Array	IDD61	VDD1	113	µA	All devices are in self-refresh CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
		IDD62	VDD2	288	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	6		
	1/2 Array	IDD61	VDD1	94	µA	
		IDD62	VDD2	194	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	6		
	1/4 Array	IDD61	VDD1	88	µA	
		IDD62	VDD2	150	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	6		
	1/8 Array	IDD61	VDD1	81	µA	
		IDD62	VDD2	125	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	6		
+25°C ≤ TC ≤ +45°C CKE ≤ 0.2V	Full Array	IDD61	VDD1	188	µA	
		IDD62	VDD2	531	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	6		
	1/2 Array	IDD61	VDD1	125	µA	
		IDD62	VDD2	313	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	6		
	1/4 Array	IDD61	VDD1	94	µA	
		IDD62	VDD2	188	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	6		
	1/8 Array	IDD61	VDD1	75	µA	
		IDD62	VDD2	125	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	6		
+45°C ≤ TC ≤ +85°C CKE ≤ 0.2V	Full Array	IDD61	VDD1	563	µA	
		IDD62	VDD2	2000	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	8		
	1/2 Array	IDD61	VDD1	344	µA	
		IDD62	VDD2	1500	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	8		

	1/4 Array	IDD61	VDD1	250	µA	
		IDD62	VDD2	1250	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	8		
	1/8 Array	IDD61	VDD1	200	µA	
		IDD62	VDD2	1125	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	8		
+85°C ≤ TC ≤ +105°C CKE ≤ 0.2V	Full Array	IDD61	VDD1	2000	µA	
		IDD62	VDD2	3000	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	31		
	1/2 Array	IDD61	VDD1	938	µA	
		IDD62	VDD2	2125	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	31		
	1/4 Array	IDD61	VDD1	625	µA	
		IDD62	VDD2	1563	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	31		
	1/8 Array	IDD61	VDD1	325	µA	
		IDD62	VDD2	1313	µA	
		IDD6IN	VDDCA	63	µA	
			VDDQ	31		

2.2.7 DC Characteristics 2

(TC = -25°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Symbol	min.	max	Unit	Test Condition	Note
Input leakage current	ILI	-2.0	2.0	µA	0 ≤ VIN ≤ VDDQ	
Output leakage current	ILO	-1.5	1.5	µA	0 ≤ VOUT ≤ VDDQ DQ = disable	
Output high voltage	VOH	0.9×VDDQ	--	V	IOH = -0.1mA	
Output low voltage	VOL	--	0.1×VDDQ	V	IOL = 0.1mA	

2.2.8 DC Characteristics 3

(TC = -25°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Symbol	min.	max	Unit	Note
AC differential input voltage	VID (AC)	-0.2	VDDQ + 0.2	V	
AC differential cross point voltage	VIX (AC)	0.5 x VDDQ - 0.15	0.5 x VDDQ + 0.15	V	
AC differential cross point voltage	VOX (AC)	0.5 x VDDQ - 0.2	0.5 x VDDQ + 0.2	V	

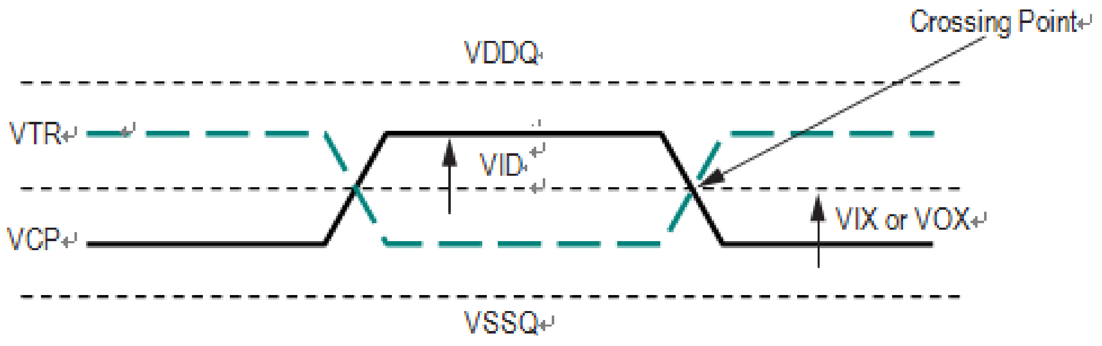


Figure 1. Differential Signal Levels

2.2.9 Pin Capacitance

(TA = +25°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Symbol		LPDDR2 1066-466	LPDDR2 400-200	Unit	Notes
CLK input pin capacitance CK, /CK	CCK	min.	1.0		pF	1,2
		max	2.0			
CLK input pin capacitance Δ CK, /CK	CDCK	min.	0		pF	1,2,3
		max	0.20	0.25		
Input pin capacitance CA, /CS, CKE	CI		1.0		pF	1,2,4
		max	2.0			
Input pin capacitance Δ CA, /CS, CKE	CDI	min.	-0.4	-0.5	pF	1,2,5
		max	0.4	0.5		
Input/output pin capacitance DQS, /DQS, DQ, DM	CIO	min.	1.25		pF	1,2,6,7
		max	2.5			
Input/output pin capacitance Δ DQS, /DQS	CDDQS	min.	0		pF	1,2,7,8
		max	0.25	0.30		
Input/output pin capacitance Δ DQ, DM	CDIO	min.	-0.5	-0.6	pF	1,2,7,9
		max	0.5	0.6		
Calibration pin capacitance	CZQ	min.	0		pF	1,2
			2.5			

Notes:

1) This parameter applies to die device only (does not include package capacitance)
2) This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating.
3) Absolute value of CCK_t-CCK_c.
4) CI applies to /CS, CKE, CA0-CA9.
5) CDI=CI-0.5x(CCK_t+CCK_c)
6) DM loading matches DQ and DQS
7) MR3 I/O configuration DS OP3-OP0=4'b0001 (34.3Ω typical)
8) Absolute value of CDQS_t and CDQS_c.
9) CDIO=CIO-0.5x(CDQS_t+CDQS_c) in byte-lane.

2.2.10 Refresh Requirement Parameters (2Gb)

Parameter	**Symbol**	**Value**	**Unit**
Number of Banks		8	
Refresh Window Tcase ≤ 85°C	tREFW	32	ms
Refresh Window Tcase 85°C < Tcase ≤ 105°C	tREFW	8	ms
Required number of REFRESH commands (min)	R	8,192	
Average time between REFRESH commands	tREFI	3.9	us
Refresh Cycle time	tRFCab	130	ns
Per Bank Refresh Cycle time	tRFCpb	60	ns
Burst Refresh Window = 4 x 8 x tRFC	tREFBW	4.16	µs

2.2.11 AC Characteristics

(TC = −25°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

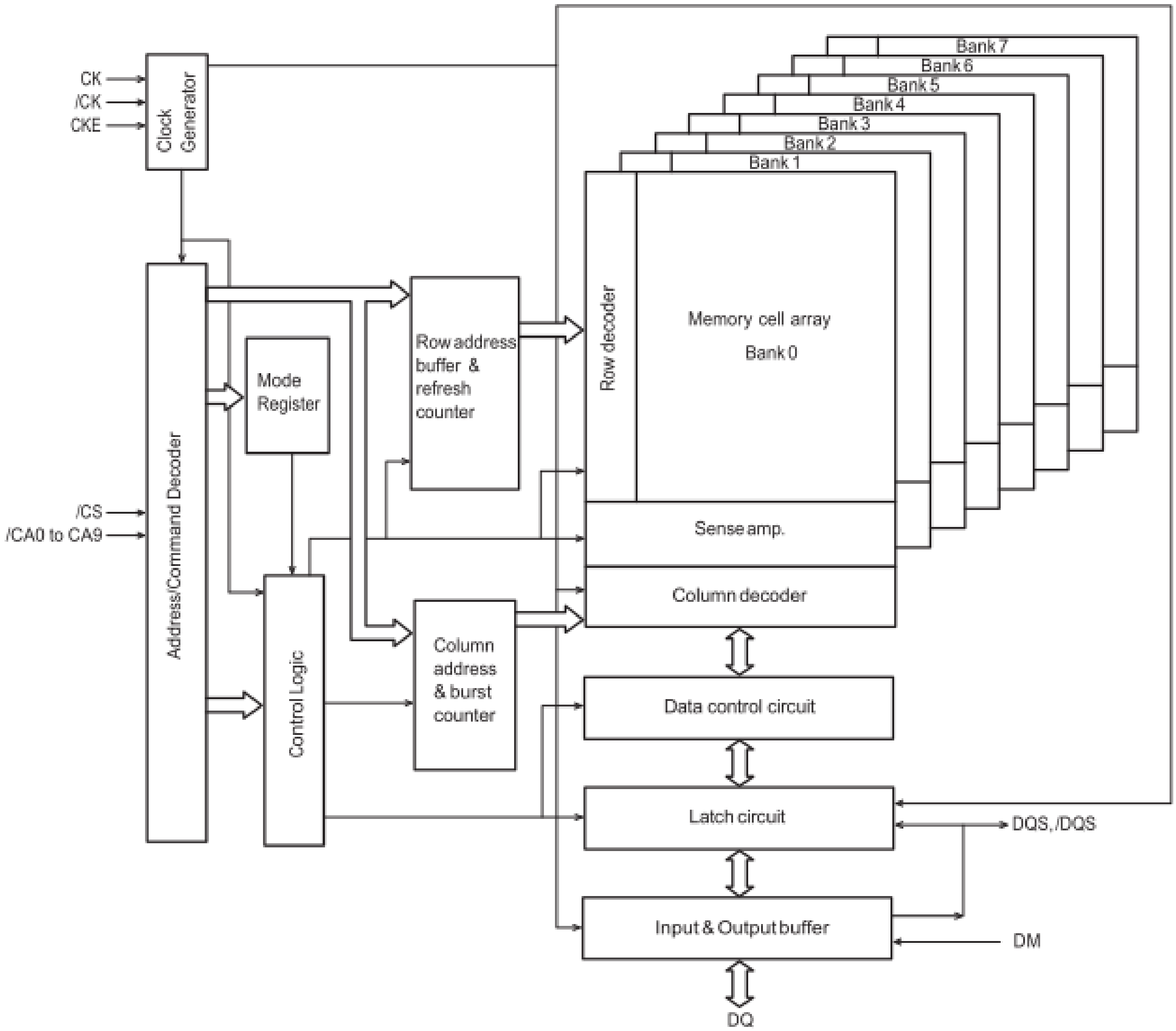
Parameter	Symbol	min/max	min tCK	LPDDR2 1066	933	800	667	533	400	333	Unit Mbps
Max. Frequency		~		533	466	400	333	266	200	166	MHz
Clock Timing											
Average Clock Period	tCK(avg)	min		1.875	2.15	2.5	3	3.75	5	6	ns
		max		100							
Average high pulse width	tCH(avg)	min		0.45							tCK(avg)
		max		0.55							
Average low pulse width	tCL(avg)	min		0.45							tCK(avg)
		max		0.55							
Absolute Clock Period	tCK(abs)	min		tCK(avg)(min) + tJIT(per)(min)							ps
Absolute clock HIGH pulse width (with allowed jitter)	t (abs)	min		0.43							t (avg)
		max		0.57							
Absolute clock LOW pulse width (with allowed jitter)	t (abs)	min		0.43							t (avg)
		max		0.57							
Clock Period Jitter (with allowed jitter)	tJIT(per)	min		-90	-95	-100	-110	-120	-140	-150	ps
		max		90	95	100	110	120	140	150	
Maximum Clock Jitter between two consecutive	tJIT(cc)	max		180	190	200	220	240	280	300	ps
Duty cycle Jitter (with allowed jitter)	tJIT(duty) allowed	min		min((tCH(abs),min - tCH(avg),min) (tCL(abs), min - tCL(avg), min)) x tCK(avg)							ps
		max		max((tCH(abs),max - tCH(avg),max) (tCL(abs), max - tCL(avg), max)) x tCK(avg)							
Cumulative error across 2 cycles	tERR(2per) allowed	min		-132	-140	-147	-162	-177	-206	-221	ps
		max		132	140	147	162	177	206	221	
Cumulative error across 3 cycles	tERR(3per) allowed	min		-157	-166	-175	-192	-210	-245	-262	ps
		max		157	166	175	192	210	245	262	
Cumulative error across 4 cycles	tERR(4per) allowed	min		-175	-185	-194	-214	-233	-272	-291	ps
		max		175	185	194	214	233	272	291	
Cumulative error across 5 cycles	tERR(5per) allowed	min		-188	-199	-209	-230	-251	-293	-314	ps
		max		188	199	209	230	251	293	314	
Cumulative error across 6 cycles	tERR(6per) allowed	min		-200	-210	-222	-244	-266	-311	-333	ps
		max		200	210	222	244	266	311	333	
Cumulative error across 7 cycles	tERR(7per) allowed	min		-209	-221	-232	-256	-279	-325	-348	ps
		max		209	221	232	256	279	325	348	
Cumulative error across 8 cycles	tERR(8per) allowed	min		-217	-229	-241	-256	-290	-338	-362	ps
		max		217	229	241	256	290	338	362	
Cumulative error across 9 cycles	tERR(9per) allowed	min		-224	-237	-294	-274	-299	-349	-374	ps
		max		224	237	294	274	299	349	374	
Cumulative error across 10 cycles	tERR(10per) allowed	min		-231	-244	-257	-282	-308	-359	-385	ps
		max		231	244	257	282	308	359	385	

Cumulative error across 11 cycles	tERR(11per) allowed	min		-237	-250	-263	-289	-316	-368	-395	ps
		max		237	250	263	289	316	368	395	
Cumulative error across 12 cycles	tERR(12per) allowed	min		-242	-256	-269	-296	-323	-377	-403	ps
		max		242	256	269	296	323	377	403	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper) allowed	min		t_{ERR}(nper), allowed, min = (1 + 0.68ln(n)) x tJIT(per), allowed, min							ps
		max		t_{ERR}(nper), allowed, max = (1 + 0.68ln(n)) x tJIT(per), allowed, max							
ZQ Calibration Parameters											
Initialization Calibration Time	tZQINIT	min		1							us
Long Calibration Time	tZQC	min	6	360							ns
Short Calibration Time	tZQCS	min	6	90							ns
Calibration Reset Time	tZQRESET	min	3	50							ns
Read Parameters											
DQS output access time from CK_t/CK_c	tDQSCK	min		2500							ps
		max		5500							
DQSCK Delta Short	tDQSCKDS	max		330	380	450	540	670	900	1080	ps
DQSCK Delta Medium	tDQSCKDM	max		680	780	900	1050	1350	1800	1900	ps
DQSCK Delta Long	tDQSCKDL	max		920	1050	1200	1400	1800	2400	-	ps
DQS-DQ skew	tDQSQ	max		200	220	240	280	340	400	500	ps
Data hold skew factor	tQHS	max		230	260	280	340	400	480	600	ps
DQS Output High Pulse Width	tQSH	min		tCH(abs) - 0.05							tCK(avg)
DQS Output Low Pulse Width	tQSL	min		t (abs) - 0.05							tCK(avg)
Data Half Period	tQHP	min		min(tQSH, tQSL)							tCK(avg)
DQ/DQS output hold time from DQS	tQH	min		tQHP-tQHS							ps
Read preamble	tRPR900E	min		0.9							tCK(avg)
Read Postamble	tRPST	min		tcL(abs) - 0.05							tCK(avg)
DQS low-Z from clock	tLZ(DQS)	min		tDQSCK(min) - 300							ps
DQ low-Z from clock	tLZ(DQ)	min		tDQSCK(min) - (1.4*tQHS(max)							ps
DQS high-Z from clock	tHZ(DQS)	max		tDQSCK(max) - 100							ps

Parameter	Symbol	min/ max	min tCK	LPDDR2							Unit
				1066	933	800	667	533	400	333	Mbps
Write Parameters											
DQ and DM input hold time (Vref based)	tDH	min		210	235	270	350	430	480	600	ps
DQ and DM input setup time (Vref based)	tDS	min		210	235	270	350	430	480	600	ps
DQ and DM input pulse width	tDIPW	min		0.35							tCK(avg)
Write command to 1st DQS latching transition	tDQSS	min		0.75							tCK(avg)
		max		1.25							tCK(avg)
DQS input high-level width	tDQSH	min		0.4							tCK(avg)
DQS input low-level width	tDQSL	min		0.4							tCK(avg)
DQS falling edge to CK setup time	tDSS	min		0.2							tCK(avg)
DQS falling edge hold time from CK	tDSH	min		0.2							tCK(avg)
Write postamble	tWPST	min		0.4							tCK(avg)
Write preamble	tWPRE	min		0.35							tCK(avg)
CKE Input Parameters											
CKE min. pulse width (high and low pulse width)	tCKE	min	3	3							tCK(avg)
CKE input setup time	tISCKE	min		0.25							tCK(avg)
CKE input hold time	tIHCKE	min		0.25							tCK(avg)
Command Address Input Parameters											
Address & control input setup time (Vref based)	tIS	min		220	250	290	370	460	600	740	ps
Address & control input hold time (Vref based)	tIH	min		220	250	290	370	460	600	740	ps
Address & control input pulse width	tIPW	min		0.40							tCK(avg)
Boot Parameters (10 MHz - 55 MHz)											
Clock Cycle Time	tCKb	max	-	100							ns
		min		18							
CKE input setup time	tISCKEb	min	-	2.5							ns
CKE input hold time	tIHCKEb	min	-	2.5							ns
Address & control input setup time	tISb	min	-	1150							ps
Address & control input hold time	tIHb	min	-	1150							ps
DQS Output data access time from CK_t/CK_c	tDQSCKb	min	-	2.0							ns
		max		10.0							
Data strobe edge to output data edge tDQSQb-1.2	tDQSQb	max	-	1.2							ns
Data hold skew factor	tQHSb	max	-	1.2							ns
Mode Register Parameters											
Mode Register Write command period	tMRW	min	5	5							tCK(avg)
Mode Register Read command period	tMRR	min	2	2							tCK(avg)

Parameter	Symbol	min/ma	min tCK	LPDDR2							Unit
				1066	933	800	667	533	400	333	Mbps
LPDDR2 SDRAM Core Parameters											
Read Latency	RL	min	3	8	7	6	5	4	3	3	tCK(avg)
Write Latency	WL	min	1	4	4	3	2	2	1	1	tCK(avg)
Active to Active command period	tRC	min		tRAS + tRPab (with all-bank Precharge) tRAS + tRPpb (with per-bank Precharge)							ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	t	min	3	15							ns
Self refresh exit to next valid command delay	tXSR	min	2	tRFCab+10							ns
Exit power down to next valid command delay	tXP	min	2	7.5							ns
LPDDR2-S4 CAS to CAS delay	tCCD	min	2	2							tCK(avg)
Internal Read to Precharge command delay	tRTP	min	2	7.5							ns
RAS to CAS Delay	tRCD	min	3	18							ns
Row Precharge Time (single bank)	tRPpb	min	3	18							ns
Row Precharge Time (all banks)	tRPab	min	3	21							ns
Row Active Time	tRAS	min	3	42							ns
		max	-	70							µs
Write Recovery Time	tWR	min	3	15							ns
Internal Write to Read command delay	tWTR	min	2	7.5					10		ns
Active bank A to Active bank B	tRRD	min	2	10							ns
Four Bank Activate window	tFAW	min	8	50						60	ns
Minimum Deep Power Down time	tDPD	min		500							µs

2.3 Block Diagram



2.4 Pin Function

2.4.1 CK, /CK (input pins)

The CK and the /CK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the /CK falling edge. When in a read operation, DQSs and DQs are referred to the cross point of the CK and the /CK. When in a write operation, DMs and DQs are referred to the cross point of the DQS and the VDDQ/2 level. DQSs for write operation are referred to the cross point of the CK and the /CK. The other input signals are referred at CK rising edge.

2.4.2 /CS (input pin)

When /CS is low, commands and data can be input. When /CS is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

2.4.3 CA0 to CA9 (input pins)

These pins define the row & column addresses and operating commands (read, write, etc.) depend on their voltage levels. See "Addressing Table" and “Command operation”.

2.4.4 [Addressing Table]

Page Size	Organization	Row address	Column address
4KB	x 16 bits	R0 to R13	C0*1 to C9
	x 32 bits	R0 to R12	C0*1 to C9

	DDR CA Pins										
Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK edge
Active	--	--	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
	R0	R1	R2	R3	R4	R5	R6	R7	R13	--	↓
Write/Read	--	--	--	--	--	C1	C2	BA0	BA1	BA2	↑
	AP	C3	C4	C5	C6	C7	C8	C9	--	--	↓

Remarks: Rx = row address. Cx = column
address Notes:
C0 is not present on the command & address, therefore C0 is implied to be zero.
BA0,1 &2 are bank select signals. The memory array is divided into banks 0, 1, 2, 3, 4, 5, 6 and 7. BA0, 1 & 2 define to which bank an active/read/write/precharge command is being applied.
AP defines the precharge mode when a read command or a write command is issued. If AP = high during a read or write command, auto precharge function is enabled.

2.4.5 [Bank Numbering and BA Input Table]

	BA0	BA1	BA2
Bank0	L	L	L
Bank1	H	L	L
Bank2	L	H	L
Bank3	H	H	L
Bank4	L	L	H
Bank5	H	L	H
Bank6	L	H	H
Bank7	H	H	H

Remarks: H = VIH, L = VIL.

2.4.6 CKE (input pin)

CKE controls power-down mode, self-refresh function and deep power-down function with other command inputs. The CKE level must be kept for 2 clocks at least if CKE changes at the crossing point of the CK rising edge and the /CK falling edge with proper setup time tIS, by the next CK rising edge CKE level must be kept with proper hold time tIH.

2.4.7 DQ0 to DQ15 (x16), DQ0 to DQ31 (x32) - (input/output pins)

Data are input to and output from these pins.

2.4.8 DQSx, /DQSx (input/ output pins, where x = 0 to 3)

DQS and /DQS provide the read data strobes (as output) and the write data strobes (as input). Each DQS (/DQS) pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

2.4.9 DM0 to DM3 (input pins)

DM is the reference signals of the data input mask function. DM is sampled at the crossing point of DQS and VDDQ/2. When DM = high, the data input at the same timing are masked while the internal burst counter will be counting up.

2.4.10 [DM truth table]

Name (Functional)	DM	DQ	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

Notes:

Used to mask write data. Provided coincident with the corresponding data.

Each DM pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

2.4.11 [DQS and DM Correspondence Table]

Part Number	Organization	DQS	Data Mask	DQ
TBD	x 16 bits	DQS0, /DQS0	DM0	DQ0 to DQ7
		DQS1, /DQS1	DM1	DQ8 to DQ15
TBD	x 32 bits	DQS0, /DQS0	DM0	DQ0 to DQ7
		DQS1, /DQS1	DM1	DQ8 to DQ15
		DQS2, /DQS2	DM2	DQ16 to DQ23
		DQS3, /DQS3	DM3	DQ24 to DQ31

2.4.12 VDD1, VSS, VSS2, VDDCA, VSSCA, VDDQ, VSSQ (power supply)

VDD1/2 and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers. VDDCA and VSSCA are power supply pins for command address input buffers.

2.5 Command Operation

2.5.1 Command Truth Table

The LPDDR2 RAM recognizes the following commands specified by the /CS, CA0, CA1, CA2, CA3 and CKE at the rising edge of the clock.

- CAxr refers to the command/address bit x on the rising edge of clock. (↑)
- CAxf refers to the command/address bit x on the falling edge of clock. (↓)

Function	Symbol	CKE			DDR CA Pins										CK
		Previ-ous cy-	Current cycle	/CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	edge
Mode register write	MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA	MA5	↑
				×	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
Mode register read	MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA	MA5	↑
				×	MA6	MA7	×								↓
Refresh per bank	REFpb	H	H	L	L	L	H	L	×						↑
				×	×										↓
Refresh all banks	REFab	H	H	L	L	L	H	H	×						↑
				×	×										↓
Self-refresh entry	SELF	H	L	L	L	L	H	×							↑
		×		×	×										↓
Bank activate	ACT	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
				×	R0	R1	R2	R3	R4	R5	R6	R7	R13	×	↓
Write	WRIT	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				×	AP*1	C3	C4	C5	C6	C7	C8	C9	×		↓
Read	READ	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				×	AP*1	C3	C4	C5	C6	C7	C8	C9	×		↓
Precharge	PRE	H	H	L	H	H	L	H	AB	×		BA0	BA1	BA2	↑
				×	×										↓
Burst terminate	BST	H	H	L	H	H	L	L	×						↑
				×	×										↓
Deep power-down mode entry	DPDEN	H	L	L	H	H	L	×							↑
		×		×	×										↓
No operation	NOP	H	H	L	H	H	H	×							↑
				×	×										↓
Maintain PD/SREF/DPD	NOP	L	L	L	H	H	H	×							↑
				×	×										↓
No operation	NOP	H	H	H	×										↑
				×	×										↓
Device deselect	DESL	H	H	H	×										↑
				×	×										↓
Power-down mode entry	PDEN	H	L	H	×										↑
		×		×	×										↓
Exit power-down/deep	PDEX,	L	H	H	×										↑

power-down mode, self refresh	SELFX, DPDX	×		×	×	↓

Remarks: H = VIH, L = VIL, × = VIH or VIL, Rx = row address, Cx = column address, AB = all banks or selected bank precharge.

Notes:

AP high during a read or write command indicates that an auto precharge will occur to the bank associated with the read or write command.
Bank selects (BA0, 1 & 2) determine which bank is to be operated upon.
Self-refresh exit and deep power-down exit are asynchronous.
/CS and CKE are sampled at the rising edge of clock.
VREF must be maintained during self-refresh and deep power-down operation.

2.5.2 Register Commands [MRR/MRW]

The register commands include both a mode register read (MRR) and a mode register write (MRW) command. The protocol provides support for a total of up to 256 8-bit registers, which will be either read-only, write-only, or both readable and writeable by the memory controller.

2.5.3 Refresh Commands [REF]

The refresh commands include an All Banks refresh command, and a self-refresh command. Entry into self-refresh mode will occur upon the transition of CKE from high to low.

2.5.4 Active Command [ACT]

Only CA0r and CA1r are needed to encode this command. The remaining bits in the CA map specify the row and bank address.

2.5.5 Read/Write Commands [READ/WRIT]

The read and write commands indicate whether a read or write is desired. CA0r, CA1r, and CA2r are needed to encode either command. The remaining bits in the CA map are used to indicate the column address. A bit to indicate whether an auto precharge is desired is provided and is registered on CA0f of both read and write commands. Two bits in the read and write command encoding have been specified as Reserved for Future Use (RFU).

2.5.6 Precharge Commands [PRE]

The Precharge command requires that the bank be specified at command time only when the auto precharge bit indicates that an All Bank pre-charge is not desired (I.E. AB (CA4r) = 0). If the All Bank precharge bit is set (I.E. AB (CA4r) = 1), bank information is not required.

2.5.7 Burst Terminate Command [BST]

The BST command will allow for both read and write commands (without auto precharge) to be interrupted on prefetch boundaries prior to the end of a burst. The desired burst length will be set in one of the mode registers.

2.5.8 Power-down and Deep Power Down [PDEN/DPDEN]

Both power-down and deep power-down modes are supported by the protocol. In normal power-down mode all input and output buffers as well as CK and /CK will be disabled. If all banks are precharged prior to entering power-down mode, the device will be said to be in Precharge power-down mode. If at least one bank is open while entering power-down mode, the SDRAM device will be said to be in Active power-down mode.
In Deep power-down mode all input/output buffers, CK, /CK, and power to the array will be disabled. The contents of the SDRAM will be lost upon entry into deep power-down mode. The command for entry into normal power-

down mode requires that /CS is high, while the command for entry into Deep power-down mode requires that /CS be low. In both cases CKE will remain active and will be the mechanism by which the SDRAM is able to exit either power-down modes.

2.5.9 Exit Command [PDEX, DPDX, SELFX]

Exit from self-refresh, power down, or deep power-down modes requires a low to high transition of CKE.

2.5.10 No Operation Command [NOP]

NOP can either be issued using a command when /CS is low or by simply deselecting /CS.

2.5.11 CKE Truth Table

	CKE		Command (n)*3		
Current state*2	Previous cycle (n-	Current cycle	/CS, CA0r to CA3r	Operation (n)*3	Notes
Active/Idle power-down	L	L	×	Maintain power-down	8
	L	H	DESL or NOP	Power-down exit	4
Deep power-down entry	L	L	×	Maintain power-down	8
	L	H	DESL or NOP	Deep power-down exit	
Self-refresh	L	L	×	Maintain self-refresh	8
	L	H	DESL or NOP	Self-refresh exit	4, 7
Bank Active	H	L	DESL or NOP	Active power down entry	4
All banks idle	H	L	DESL or NOP	Precharge power down entry	4
	H	L	SELF	Self-refresh entry	5
Other	H	H	Refer to the Command Truth Table		6

Remark: H = VIH, L = VIL, × = Don't care Notes:
CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge. Current state is the state of the LPDDR2 RAM immediately prior to clock edge n.
Command (n) is the command registered at clock edge n, and operation (n) is a result of Command (n).
All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document. Self-refresh mode can only be entered from the all banks idle state.
Must be a legal command as defined in the command truth table.
Valid commands for deep power-down exit and power-down exit and self-refresh exit are NOP and DESL only. Deep power-down, power-down and self-refresh cannot be entered while read/write operations, mode register read/write or precharge operations are in progress.
VREF must be maintained during self-refresh operation.
Clock frequency may be changed or stopped during the active power-down or idle power-down state.

2.6 Simplified State Diagram

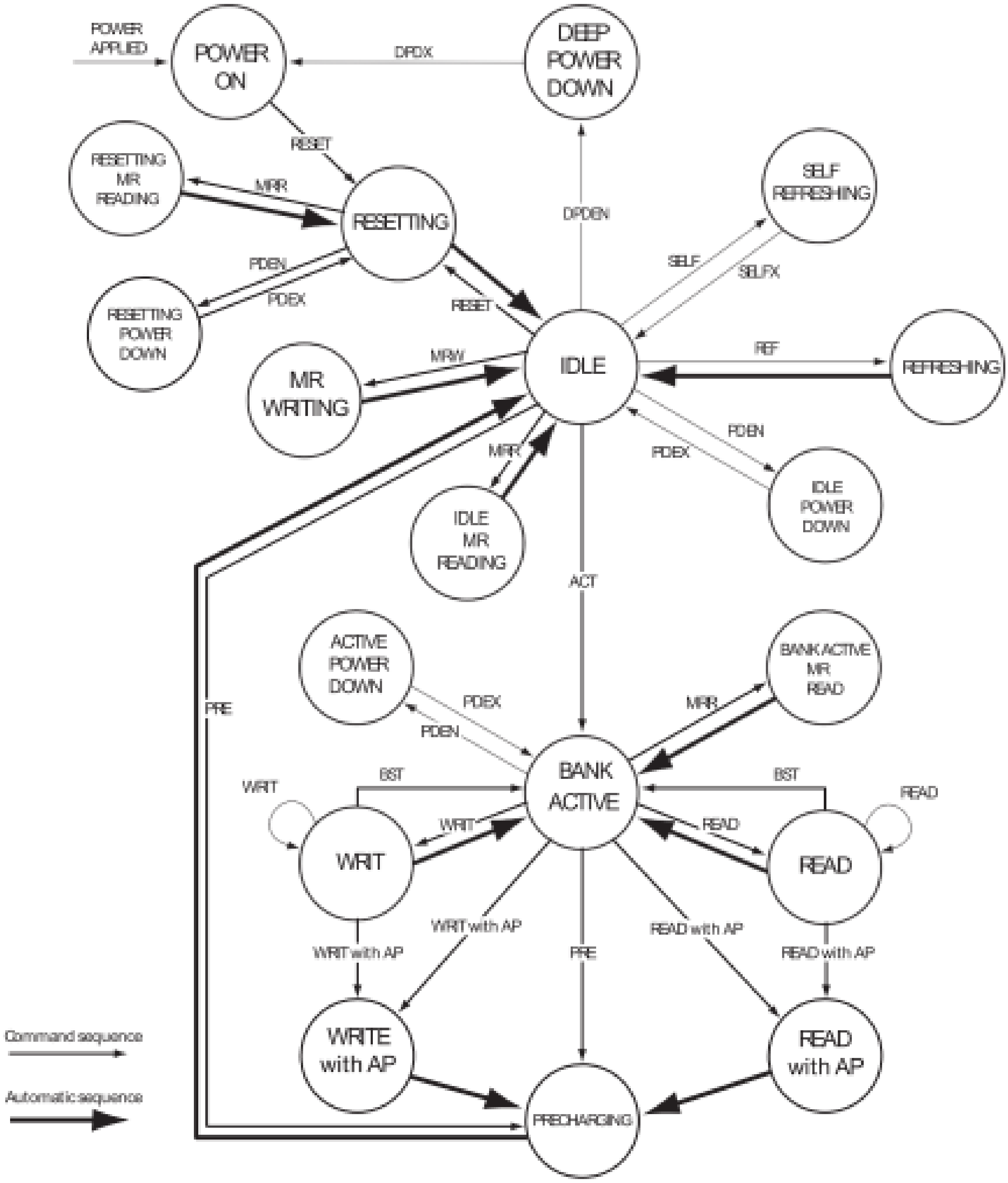


Figure 3 Simplified State Diagram

2.7 Operation of the LPDDR2 RAM

Read and write accesses to the LPDDR2 RAM are burst oriented; accesses start at a selected location and continue for the fixed burst length of four, eight, and sixteen in a programmed sequence. Accesses begin with the registration of an activecommand, which is then followed by a read or write command. The address bits registered coincident with the active command is used to select the bank and row to be accessed (BA0,1 & 2 selects the bank; R0 to R13 selects the row). The address bits registered coincident with the read or write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operations, the LPDDR2 RAM must be initialized. The following sections provide detailed information covering device initialization; register definition, command descriptions and device operation.

2.7.1 LPDDR2 RAM Power-On and Initialization Sequence

2.7.1.1 Power Ramp and Device Initialization

Power Ramp

While applying power (after Ta), CKE shall be held at a logic low level (≤0.2 × VDDCA), all other inputs shall be between VIL (min.) and VIH (max.). The LPDDR2 RAM device will only guarantee that outputs are in a high impedance state while CKE is held low. On or before the completion of the power ramp (Tb) CKE must be held low. Voltage levels at I/Os and outputs must be between VSSQ and VDDQ during voltage ramp time to avoid latch-up.

The following conditions apply:

- Ta is the point where any power supply first reaches 300mV.
- After Ta is reached, VDD1 must be greater than VDD2 – 200mV.
- After Ta is reached, VDD1 and VDD2 must be greater than VDDCA – 200mV.
- After Ta is reached, VDD1 and VDD2 must be greater than VDDQ – 200mV.
- After Ta is reached, VREF must always be less than all other supply voltages.
- The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100mV.
- Tb is the point when all supply and reference voltages are within their respective min/max operating conditions.
- Power ramp duration tINIT0 (Tb – Ta) must be no greater than 20ms.

Note:
VDD2 is not present in some systems. Rules related to VDD2 in those cases do not apply.

CKE and Clock

Beginning at Tb, CKE must remain low for at least tINIT1 = 100ns, after which it may be asserted high. Clock must be stable at least tINIT2 = 5tCK prior to the first low to high transition of CKE (Tc). CKE, /CS and CA inputs must observe setup and hold time (tIS, tIH) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

Reset Command

After tINIT3 is satisfied, a MRW (Reset) command shall be issued (Td). Wait for at least tINIT4 = 1µs while keeping CKE asserted and issuing NOP or DESL commands.

Mode Register Reads and Device Auto-Initialization (DAI) polling

After tINIT4 is satisfied (Te), only MRR commands (including power-down entry/exit) are allowed. It is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0, Device ID, etc.). The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete. As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured. After the DAI-bit (MR0.DAI) is set to "ready" by the memory device, the device is in idle state (Tf). The state of the DAI status bit can be determined by an MRR command to MR0 DAI. The LPDDR2 RAM will set the DAI-bit no later than tINIT5 (10µs) after the Reset command.

Normal Operation

After tINIT5 (Tf), MRW commands may be used to properly configure the memory, for example the output buffer driver strength, latencies etc. The LPDDR2 RAM device will now be in IDLE state and ready for any valid command. After Tf, the clock frequency may be changed according to the clock frequency change procedure described in section Input Clock Stop and Frequency Change during Power-Down of this specification.

2.7.1.2 Timing Parameters for Initialization

	Value			
Symbol	min.	max.	Unit	Test Condition
tINIT0	--	20	ms	Maximum Power Ramp Time
tINIT1	100	--	ns	Minimum CKE low time after completion of power ramp
tINIT2	5	--	tCK	Minimum stable clock before first CKE high
tINIT3	200	--	µs	Minimum Idle time after first CKE assertion
tINIT4	1	--	µs	Minimum Idle time after Reset command, this time will be about 2 × tRF-
tINIT5	--	10	µs	Maximum duration of Device Auto-Initialization
tCKBOOT	18	100	ns	Clock cycle time during boot

[See Figure 134 in JEDEC Standard No. 209-2E]

2.7.2 Programming the Mode Register

Mode Register Assignment

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Remark
0	00h	Device Info.	R	(RFU)						DI	DAI	See MR0
1	01h	Device Feature 1	W	nWR (for AP)			WC	BT	BL			See MR1
2	02h	Device Feature 2	W	(RFU)				RL & WL				See MR2
3	03h	I/O Config-1	W	(RFU)				DS				See MR3
4	04h	SDRAM Refresh	W	TUF	(RFU)				Refresh Rate			See MR4
5	05h	Basic Config-1	R	Company ID								See MR5
6	06h	Basic Config-2	R	Revision ID1								See MR6
7	07h	Basic Config-3	R	Revision ID2								See MR7
8	08h	Basic Config -4	R	I/O Width		Density				Type		See MR8
9	09h	Test Mode	W*1	Vendor-Specific Test Mode								See MR9
10	0Ah	IO Calibration	W	Calibration Code								See MR10
11:15	0Bh TO 0Fh	Reserved		(RFU)								

16	10h	PASR_Bank	W	Bank Mask	See MR16
17	11h	PASR_Seg	W	Segment Mask	See MR17
18:23	12h TO 17h	Reserved		(RFU)	

MR No.24 to 31 are Non-Volatile Memory (NVM) specific mode registers, which LPDDR2 does not have.

32	20h	Calibration Pattern	R	Calibration Pattern A	See MR32
40	28h	Calibration Pattern	R	Calibration Pattern B	See MR40
63	3FH	Reset	W	×	See MR63

MR No. 33 to 39, 41 to 62 and MR 64 to 255 are reserved.

Note: MR9[5] is Fail Bit, and Read-Only.

Remarks:

R = read-only
W = write-only
DAI = Device Auto-Initialization
DI = Device Information
nWR = Write Recovery for auto precharge
WC = Wrap Control
BT = Burst Type
BL = Burst Length
RL & WL = Read latency & Write latency
DS = Drive Strength
TUF = Temperature Update Flag

MR0

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)						DI	DAI

OP<O>	DAI (Device Auto-Initialization Status) 0B: DAI complete 1B: DAI still in progress
OP<1>	DI (Device Information) 0B: DDR2 Mobile RAM 1B: Reserved

MR1

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR(for AP)			WC	BT	BL		

OP<2:0>	BL(Burst Length) 010B: BL4 (default) 011B: BL8 100B: BL16 All others: Reserved
OP<3>	BT(Burst Type) 0B: Sequential (default) 1B: Interleaved

OP<4>	WC(Wrap Control) 0B: Wrap (default) 1B: No Wrap
OP<7:5>	nWR(Write Recovery for Auto-pre-charge) 001 B: nWR=3 (default) 010B: nWR=4 011B: nWR=5 100B: nWR=6 101B: nWR=7 110B: nWR=8 All others: Reserved

Notes:

Programmed value in nWR register is the number of clock cycles which determined when to start internal pre-charge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

MR2

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

OP<3:0>	RL & WL(Read latency and write latency) 0001B: RL3 / WL1 (default) 0010B: RL4 / WL2 0011 B: RL5 / WL2 0100B: RL6 / WL3 0101B: RL7 / WL4 0110B: RL8 / WL4 All others: Reserved

MR3

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

OP<3:0>	DS(Drive Strength) 0000B: Reserved 0001B: 34.3Ω typ. 0010B: 40Ω typ. (default) 0011B: 48Ω typ. 0100B: 60Ω typ. 0101B: Reserved for 68.6Ω typ. 0110B: 80Ω typ. 0111B: 120Ω typ. All others: Reserved

MR4

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)			Refresh Rate			

OP<2:0>	Refresh Rate 000B: Reserved 001B: Reserved 010B: 2× tREF 011B: 1× tREF 100B: RFU 101B: 0.25× tREF, set to 85° C, do not derate 110B: 0.25× tREF , set to 95° C, de-rate 111B: temp>105° C, set to 105° C, stall
OP<7>	TUF(Temperature Update Flag) 0B: OP<2:0> value has not changed since last read of MR4. 1B: OP<2:0> value has changed since last read of MR4.

MR5

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacture ID							

OP<7:0>	Manufacture ID 11111101B

MB6

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1(Die Revision)							

OP<7:0>	Revision ID1 00000000B: Default Value

MB7

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2(RFU)							

OP<7:0>	Revision ID2 00000000B: Default Value

MB8

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

OP<1:0>	Type 00B: S4 SDRAM
OP<5:2>	Density 0101B: 2Gb
OP<7:6>	I/O width 00B: x32 01B: x16 10B: x8

MB9

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-Specific Test Mode							

OP<4>	Tested Die Bit 0B: Untested 1B: Tested(default)
OP<5>	Tested Die Bit 0B: Pass(default) 1B: Fail

MR10

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

OP<7:0>	Calibration Code 0xFF: Calibration command after initialization 0xAB: Long calibration 0x56: Short calibration 0xC3: ZQ Reset Others: Reserved

MR16

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask							

OP<7:0>	Bank Mask 0B: refresh enable to the bank (=unmasked, default) 1B: refresh blocked(=masked)

MB17

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

OP<7:0>	Segment Mask 0B: refresh enable to the segment (=unmasked, default) 1B: refresh blocked(=masked)

MB32

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Pattern “A”							

OP<7:0>	DQ outputs pattern A			
	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
	1	0	1	0

MR40

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Pattern “B”							

OP<7:0>	DQ outputs pattern B			
	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
	0	0	1	1

2.7.3 Bank Activate Command [ACT]

The bank activate command is issued by holding /CS low, CA0 low, and CA1 high at the rising edge of the clock. The bank addresses BA0, 1 & 2 are used to select the desired bank. The row address R0 through R12 is used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any read or write operation can be executed. Immediately after the Bank Active command, the LPDDR2 RAM can accept a read or write command on the following clock cycle at time tRCD after the activate command is sent. Once a bank has been activated it must be precharged before another bank activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive bank activate commands to the same bank is determined by the /RAS cycle time of the device (tRC). The minimum time interval between successive bank activate commands to the different bank is determined by (tRRD).

[See Figure 19 in JEDEC Standard No. 209-2E]

2.7.4 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting /CS low, CA0 high, and CA1 low at the rising edge of the clock. CA2r must also be defined at this time to determine whether the access cycle is a read operation (CA2r high) or a write operation (CA2r low).

The LPDDR2 RAM provides a fast column access operation. A single read or write command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. For example, the 8M bits x 16 I/O x 8 banks chip has a page length of 16384 bits (defined by C1 to C11). The page length of 16384 is divided into 4096, 2048, or 1024 for 16 bits burst respectively. A 4 bits or 8 bits or 16 bits burst operation will occur entirely within one of the 4096, 2048, or 1024 groups beginning with the column address supplied to the device during the read or write command (C1 to C11). The second, third and fourth access will also occur within this group segment. However, the burst order is a function of the starting address, and the burst sequence.

A new burst access must not interrupt the previous 4 bits burst operation in case of BL = 4 setting. In case of BL = 8 and BL= 16 settings, reads may be interrupted by reads and writes may be interrupted by writes provided that this occurs on a 4 bits boundary. The minimum CAS to CAS delay is defined by tCCD.

2.7.5 Burst Mode Operation

							Burst cycle number and burst address sequence															
C3 (CA1f)	C2 (CA6r)	C1 (CA5r)	C0 (0)	BL	BT	WC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
×	×	0	0	4	any	Wrap	0	1	2	3												
×	×	1	0				2	3	0	1												
×	×	×	0		any	NW*5	y	y+1	y+2	y+3												
×	0	0	0	8	Seq	Wrap	0	1	2	3	4	5	6	7								
×	0	1	0				2	3	4	5	6	7	0	1								
×	1	0	0				4	5	6	7	0	1	2	3								
×	1	1	0				6	7	0	1	2	3	4	5								
×	0	0	0		Int		0	1	2	3	4	5	6	7								
×	0	1	0				2	3	0	1	6	7	4	5								
×	1	0	0				4	5	6	7	0	1	2	3								
×	1	1	0				6	7	4	5	2	3	0	1								
0	0	0	0	16	Seq	Wrap	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	1	0				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0	1	0	0				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0	1	1	0				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1	0	0	0				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1	0	1	0				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1	1	0	0				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1	1	1	0				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D

Remarks: NW: no wrap. Int: interleaved. Seq: sequential. Any: sequential or interleaved.
C3 = CA1f. C2 = CA6r. C1 = Ca5r. C0=0.

Notes:

C0 input is not present on CA bus. It is implied zero.
For BL = 4, the burst address represents C1 to C0.
For BL = 8, the burst address represents C2 to C0.
For BL = 16, the burst address represents C3 to C0.
Non-wrap, BL4, data-orders shown below are prohibited:
Not across full page boundary. (x16: 3FE, 3FF, 000, 001)
(x32: 1FE, 1FF, 000, 001)
Not across sub page boundary. (x16: 1FE, 1FF, 200, 201)

2.7.6 Burst Read Command [READ]

The Burst Read command is initiated by having /CS low, CA0 high, CA1 high and CA2 low at the rising edge of the clock. The address inputs, CA5r to CA4r and CA1f to CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the read command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid datum is available RL + tDQSCK + tDQSQ after the rising edge of the clock where the read command is issued. The data strobe output (DQS) is driven low tRPRE before valid data (DQ) is driven onto the data bus.

The first bit of the burst is synchronized with the first rising edge of the data strobe (DQS). Each subsequent dataout appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is defined by mode register.

Pin timings are measured relative to the cross point of DQS and its complement, /DQS.

[See Figures 24, 25 in JEDEC Standard No. 209-2E]

[See Figure 33 in JEDEC Standard No. 209-2E]

The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum read to write latency is RL + RU (tDQSCKmax/tCK) + BL/2 + 1 – WL. Note that if a read burst is interrupted with a Burst Terminate (BST) command, the effective BL of the interrupted read burst should be used to calculate the minimum read to write latency.

[See Figure 35 in JEDEC Standard No. 209-2E]

The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, every 4 clocks for BL = 8 operation, and every 16 clocks for BL = 16 operation. This operation is allowed regardless of whether the same or different banks as long as the banks are activated.

Burst read can only be interrupted by another read with 4 bits burst boundary.

[See Figure 37 in JEDEC Standard No. 209-2E]

Notes:

Read burst interrupt function is only allowed on burst of 8 and 16.

Read burst interrupt may only occur on even clocks after the previous read commands provided that tCCD is met. Reads can only be interrupted by other reads or the BST command.

Read burst interruption is allowed to any bank inside SDRAM. Read burst with auto precharge is not allowed to be interrupted.

The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

2.7.7 Burst Write Command [WRIT]

The Burst Write command is initiated by having /CS low, CA0 high, CA1 high and CA2 high at the rising edge of the clock. The address inputs determine the starting column address. The first valid datum is available Write Latency (WL) cycles + tDQSS from the rising edge of the clock from which the Write command is driven. A data strobe signal (DQS) should be driven low (preamble) nominally half clock prior to the data input. The first data bit of the burst cycle must be applied to the DQ pins tDS prior to the first rising edge of the DQS following the preamble. The subsequent burst bit data are sampled on successive edges of the DQS until the burst length is completed, which is 4, 8 or 16 bit burst.

tWR must be satisfied before a precharge command to the same bank may be issued after a burst write operation. Pin timings are measured relative to the crossing point of DQS and its complement, /DQS.

[See Figure 42 in JEDEC Standard No. 209-2E]

[See Figure 45 in JEDEC Standard No. 209-2E]

The minimum number of clocks from the burst write command to the burst read command for any bank is [WL + 1 + BL/2

+ RU (tWTR/tCK)]. If a write burst is interrupted with a Burst Terminate (BST) command, the effective BL of the interrupted write burst should be used to calculate the minimum write to read latency.

[See Figure 47 in JEDEC Standard No. 209-2E]

The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL = 16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Burst write can only be interrupted by another write with 4 bits burst boundary, provided that tCCD is met.

[See Figure 49 in JEDEC Standard No. 209-2E]

Notes:

Write burst interrupt function is only allowed on burst of 8 and 16.Write burst interrupt may only occur on even clocks after the previous write commands, provided that tCCD is met. Writes can only be interrupted by other writes or the BST command.

Write burst interruption is allowed to any bank inside SDRAM. Write burst with auto precharge is not allowed to be interrupted.

2.7.8 Write Data Mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on LPDDR2 RAM.

DM can mask input data. By setting DM to low, data can be written. When DM is set to high, the corresponding data is not written, and the previous data is held.

The latency between DM input and enabling/disabling mask function is 0.

[See Figure 57 in JEDEC Standard No. 209-2E]

2.7.9 Precharge Command [PRE]

The precharge command is used to precharge or close a bank that has been activated. The precharge command is initiated by having /CS low, CA0 high, CA1 high, CA2 low, and CA3 high at the rising edge of the clock. The precharge command can be used to precharge each bank independently or all banks simultaneously. Three address bits CA4r, CA7r and CA8r are used to define which bank to precharge when the command is issued.

CA4r	CA7r	CA8r	CA9r	Precharged bank(s)
L	L	L	L	Bank 0 only
L	H	L	L	Bank 1 only
L	L	H	L	Bank 2 only
L	H	H	L	Bank 3 only
L	L	L	H	Bank 4 only
L	H	L	H	Bank 5 only
L	L	H	H	Bank 6 only
L	H	H	H	Bank 7 only
H	×	×	×	All banks

Remark: H = VIH, L = VIL, × = VIH or VIL

2.7.10 Burst Read Operation Followed by Precharge

For the earliest possible precharge, the precharge command may be issued on the rising edge of clock BL/2 clocks after a read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (tRP). A precharge command cannot be issued until tRAS is satisfied.

The minimum read to precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefretch of a read to precharge command. This time is called tRTP (Read to Precharge).

[See Figure 64 in JEDEC Standard No. 209-2E]

2.7.11 Burst Write Operation Followed by Precharge

For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the precharge command can be issued. This delay is known as a write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No precharge command should be issued prior to the tWR delay. Minimum Write to Precharge command spacing to the same bank is WL + BL/2 + RU (tWR/tCK) clock cycles. If the data burst is interrupted with a BST command, the effective BL shall be used to calculate the minimum Write to Precharge spacing.

[See Figure 67 in JEDEC Standard No. 209-2E]

2.7.12 Auto Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the precharge command or the auto precharge function. When a read or a write command is given to the LPDDR2 RAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If AP is low when the read or write command is issued, then normal read or write burst operation is executed and the bank remains active at the completion of the burst sequence. If AP is high when the read or write command is issued, then the auto precharge function is engaged. During auto precharge on the rising edge which is Read Latency (RL) clock cycles before the end of the read burst.

Auto precharge can also be implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read latency) thus improving system performance for random data access.

2.7.13 Burst Read with Auto Precharge

If AP (CA0f) is high when a read command is issued, the read with auto precharge function is engaged. The LPDDR2 RAM starts an auto precharge operation on the rising edge of the clock BL/2 or RU (tRTP/tCK) cycles later than the read with AP command.

A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously. The /RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.

The /RAS cycle time (tRC) from the previous bank activation has been satisfied.

[See Figure 68 in JEDEC Standard No. 209-2E]

2.7.14 Burst Write with Auto Precharge

If AP (CA0f) is high when a write command is issued, the write with auto precharge function is engaged. The LPDDR2 RAM starts with an auto precharge operation on the rising edge of which is tWR cycles after the completion of the burst write. A new bank activate (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.

The data-in to bank activate delay time (tWR + tRP) has been satisfied.

The /RAS cycle time (tRC) from the previous bank activation has been satisfied.

[See Figure 70 in JEDEC Standard No. 209-2E]

The LPDDR2 RAM supports the concurrent auto precharge feature, a read with auto precharge enabled, or a write with auto precharge enabled, may be followed by any column command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply. (E.G. Conflict between READ data and WRITE data must be avoided.)

The minimum delay from a read or write command with auto precharge enabled, to a command to a different bank, is summarized below.

From command	To command (different bank, non- interrupting command)	Minimum delay (concurrent AP supported)	Units
Read w/ AP	Read or Read w/ AP	BL/2	tCK
	Write or Write w/ AP	(BL/2) + 2	tCK
	Precharge or Activate	1	tCK
Write w/ AP	Read or Read w/ AP	WL + (BL/2) + tWTR	tCK
	Write or Write w/ AP	BL/2	tCK
	Precharge or Activate	1	tCK

The minimum delay from the read, write and precharge command to the precharge command to the same bank is summarized below.

From Command	To Command	Minimum delay between "From Command" to "To Command"	Units	Notes
Read	Precharge (to same bank as Read)	(BL/2) + Max (2, RU (tRTP/tCK)) -	tCK	1
	Precharge all	(BL/2) + Max (2, RU (tRTP/tCK)) -	tCK	1
Read w/ AP	Precharge (to same bank as Read w/	(BL/2) + Max (2, RU (tRTP/tCK)) -	tCK	1
	Precharge all	(BL/2) + Max (2, RU (tRTP/tCK)) -	tCK	1
Write	Precharge (to same bank as Write)	WL + (BL/2) + tWTR	tCK	1
	Precharge all	WL + (BL/2) + tWTR	tCK	1
Write w/ AP	Precharge (to same bank as Write w/	WL + (BL/2) + tWTR	tCK	1
	Precharge all	WL + (BL/2) + tWTR	tCK	1
Precharge	Precharge (to same bank as precharge)	1	tCK	1
	Precharge all	1	tCK	1
Precharge All	Precharge	1	tCK	1
	Precharge all	1	tCK	1

Notes:

For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP depending on the latest precharge command issued to that bank.

2.7.15 The Burst Terminate [BST]

The Burst Terminate (BST) command is initiated by having /CS low, CA0 high, CA1 high, CA2 low, and CA3 low at the rising edge of clock. The 4-bit prefetch architecture allows the BST command to be asserted on an even number of clock cycles after a write or read command. The BST command only affects the most recent read or write command. The latency of the BST command following a read command is equal to the Read Latency (RL). The latency of the BST command followin

a Write command is equal to the Write Latency (WL). Therefore, the effective burst length of a Read or Write command interrupted by a BST command is an integer multiple of 4 and is defined as follows:

Effective BL = 2 × {Number of clocks from the read or write command to the BST command}

[See Figure 54 in JEDEC Standard No. 209-2E]

Burst Terminate interrupts the burst RL cycles after the BST command for reads. BST can only be issued an even number of clocks after the read command.

[See Figure 53 in JEDEC Standard No. 209-2E]

Burst Terminate interrupts the burst WL cycles after the BST command for writes. BST can only be issued an even number of clocks after the write command.

2.7.16 Refresh Command [REF]

The Refresh command is initiated by having /CS low, CA0 low, CA1 low, and CA2 high at the rising edge of clock. All Bank Refresh is initiated by having CA3 high at the rising edge of clock.

For All Bank Refresh, all banks of the LPDDR2 RAM must be precharged and idle for a minimum of the Precharge time (tRP) before the Refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started. When the All Bank refresh cycle has completed, all banks of the LPDDR2 RAM will be in the precharged (idle) state. A delay between the Refresh Command (REF) and the next Activate command or subsequent Refresh command must be greater than or equal to the Refresh cycle time (tRFC).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given LPDDR2 RAM SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 × tREFI.

[See Figures 76, 77 in JEDEC Standard No. 209-2E]

2.7.17 Self-Refresh [SELF]

The self-refresh command can be used to retain data in the LPDDR2 RAM, even if the rest of the system is powered down. When in the self-refresh mode, the LPDDR2 RAM retains data without external clocking. The LPDDR2 RAM device has a built-in timer to accommodate self-refresh operation. The self-refresh command is defined by having CKE low, /CS low, CA0 low, CA1 low, and CA2 high at the rising edge of the clock. CKE must be high during the previous clock cycle. Once the command is registered, CKE must be held low to keep the device in self-refresh model. Once the LPDDR2 RAM has entered self refresh mode, all of the external signals except CKE, are “don’t care”. For proper self-refresh operation, all power supply pins (VDD1, VDD2, VDDQ and VREF) must be at valid levels. The SDRAM initiates a minimum of one refresh command internally within tCKE period once it enters self-refresh mode. The clock is internally disabled during self-refresh operation to save power. The minimum time that the LPDDR2 RAM must remain in self-refresh mode is tCKE. The user may change the external clock frequency or halt the external clock one clock after self-refresh entry is registered; however, the clock must be restarted and stable before the device can exit self-refresh operation.

The use of self-refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self-refresh mode. Upon exit from self-refresh, the LPDDR2 RAM requires a minimum of one extra auto refresh command before it is put back into self-refresh mode.

[See Figure 78 in JEDEC Standard No. 209-2E]

Note: Device must be in the "All banks idle" state prior to entering self refresh mode.

2.7.18 Mode Register Read Command

The mode register read command is used to read configuration and status data from mode registers. The mode register read (MRR) command is initiated by having /CS low, CA0 low, CA1 low, CA2 low, and CA3 high at the rising edge of the clock. The mode register is selected by {CA1f to CA0f, CA9r to CA4r}. The mode register contents are available on the first data beat of DQ0 to DQ7, RL + tDQSCK + tDQSQ after the rising edge of the clock where the mode register read command is issued. Subsequent data beats contain valid, but undefined content. The MRR command has a burst length of four. The MRR command may not be interrupted by the BST command, MRR command or any other read command. The MRR command period (tMRR) is 2 clocks.

[See Figure 79 in JEDEC Standard No. 209-2E]

Notes:

Mode register read has a burst length of four.

Mode register read may not be interrupted by subsequent read, MRR, or BST command.

Mode register data is valid only on DQ0 to DQ7 on the first beat. Subsequent beats contain valid, but undefined data. The mode register read command period (tMRR) is 2 clocks. No command (other than NOP or DESL) is allowed during this period.

2.7.19 Mode Register Write Command

The mode register write command is used to write configuration data to mode registers. The mode register write (MRW) command is initiated by having /CS low, CA0 low, CA1 low, CA2 low, and CA3 low at the rising edge of the clock. The mode register is selected by {CA1f to CA0f, CA9r to CA4r}. The data to be written to the mode register is contained in CA9f to CA3f. The MRW command period is defined by tMRW.

The MRW may only be issued when all banks are in the idle pre-charge state or to issue a reset command.

The MRW command is also used to initiate the reset command. The reset command is allowed in both the Idle and row active states as well as the power on Initialization sequence and brings the device to the tRESET (tINIT4) state in the power on Initialization sequence.

[See Figure 84 in JEDEC Standard No. 209-2E]

Note: The mode register write command period (tMRW) is 5 clocks. No command (other than NOP or DESL) is allowed during this period.

2.7.20 Power-Down [PDEN]

Power-down is synchronously entered when CKE is registered low and /CS high at the rising edge of clock. CKE is not allowed to go low while mode register read or write operations are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto precharge, or auto-refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power-down.

If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, /CK and CKE. In power-down mode, CKE low must be maintained at the inputs should be in a valid state but all other input signals are “Don’t Care”. CKE low must be maintained until tCKE has been satisfied. Maximum power-down duration is limited by the refresh requirements of the device, which allows a maximum of 9 tREFI if maximum posting of REF is utilized immediately before entering power-down.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or deselect command). CKE high must be maintained until tCKE has been satisfied.

[See Figure 91 in JEDEC Standard No. 209-2E]

The pattern shown below can repeat over a long period of time. With this pattern, LPDDR2 RAM guarantees all AC and DC timing, voltage specifications with temperature and voltage drift.

[See Figure 93 in JEDEC Standard No. 209-2E]

[See Figure 95 in JEDEC Standard No. 209-2E]

[See Figure 96 in JEDEC Standard No. 209-2E]

[See Figure 97 in JEDEC Standard No. 209-2E]

[See Figure 99 in JEDEC Standard No. 209-2E]

[See Figure 100 in JEDEC Standard No. 209-2E]

[See Figure 101 in JEDEC Standard No. 209-2E]

[See Figure 102 in JEDEC Standard No. 209-2E]

[[See Figure 103 in JEDEC Standard No. 209-2E]

[See Figure 104 in JEDEC Standard No. 209-2E]

2.7.21 Deep Power-Down [DPDEN]

Deep power-down is synchronously entered when CKE is registered low with /CS low, CA0 high, CA1 high, and CA2 low at the rising edge of clock. In deep power-down mode, all input buffers except CKE, all output buffers, and the power to the array will be disabled. The contents of the SDRAM will be lost upon entry into deep power-down mode.

The deep power-down state is asynchronously exited when CKE is registered high with a stable clock input. The SDRAM must be fully re-initialized as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence.

[See Figure 105 in JEDEC Standard No. 209-2E]

2.7.22 Input Clock Stop and Frequency Change during Power-Down

LPDDR2 RAM input clock frequency can be changed under following conditions: LPDDR2 RAM is in power down mode.CKE must be at logic low level.

A minimum of 2 clocks must be waited after CKE goes low before clock frequency may change In order to reduce power, the input clock may be stopped during power down. When exiting power down, the clock must be stable prior to CKE going high.

SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, CKE must be held at stable low levels. Once input clock frequency is changed, stable new clocks must be provided to SDRAM before recharge power down may be exited. Depending on new clock frequency an additional MRW command may need to be issued to appropriately set the WR, RL and so on.

[See Figure 91 in JEDEC Standard No. 209-2E]

2.7.23 Clock Stop

Stopping the clocks during idle periods is an effective way of reducing power consumption. In addition to clock stop during power-down states, LPDDR2 RAM also supports clock stop under the following conditions:
The last command (activate, read, write, precharge, mode register write, mode register read, refresh) has executed to completion, including any data-out during read bursts; the number of clock pulses per access command depends on the device's AC timing parameters and the clock frequency.
The related timing conditions (tRCD, tWR, tRP, tMRR, tMRW, etc.) have been
met. CKE is held high.

When the above conditions have been met, the device is either in "idle state" or "row active" state and clock stop mode may be entered with CK held low and /CK held high.

Clock stop mode is exited by restarting the clock. At least one NOP command must be issued before the next command may be applied. Additional clock pulses might be required depending on the system characteristics.

[See Figure 91 in JEDEC Standard No. 209-2E]

2.7.24 No Operation Command [NOP]

The no operation command (NOP) should be used in cases when the LPDDR2 RAM is in an idle or a wait state. The purpose of the no operation command is to prevent the LPDDR2 RAM from registering any unwanted commands between operations. NOP command is holding /CS low, CA0 high, CA1 high, and CA2 high at the rising edge of the clock. NOP command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

2.7.25 Deselect Command [DESL]

The deselect command (DESL) performs the same function as a no operation command. DESL command occurs when /CS is brought high at the rising edge of the clock.