16-Bit ANALOG-TO-DIGITAL CONVERTER with Onboard Reference (compatible to ADS1110A0)

FEATURES

- **COMPLETE DATA ACQUISITION SYSTEM IN A TINY SOT23-6 PACKAGE**
- **ONBOARD REFERENCE:**
  Accuracy: 2.048V ±0.05%
  Drift: 5ppm/°C
- **ONBOARD PGA**
- **ONBOARD OSCILLATOR**
- **16-BITS NO MISSING CODES**
- **INL: 0.01% of FSR max**
- **CONTINUOUS SELF-CALIBRATION**
- **SINGLE-CYCLE CONVERSION**
- **PROGRAMMABLE DATA RATE: 15SPS TO 240SPS**
- **I²C INTERFACE—EIGHT AVAILABLE ADDRESSES**
- **POWER SUPPLY: 2.7V to 5.5V**
- **LOW CURRENT CONSUMPTION: 240∝A**

DESCRIPTION

The HT8110A is a precision, continuously self−calibrating Analog-to-Digital (A/D) converter with differential inputs and up to 16 bits of resolution in a small SOT23-6 package. The onboard 2.048V reference provides an input range of

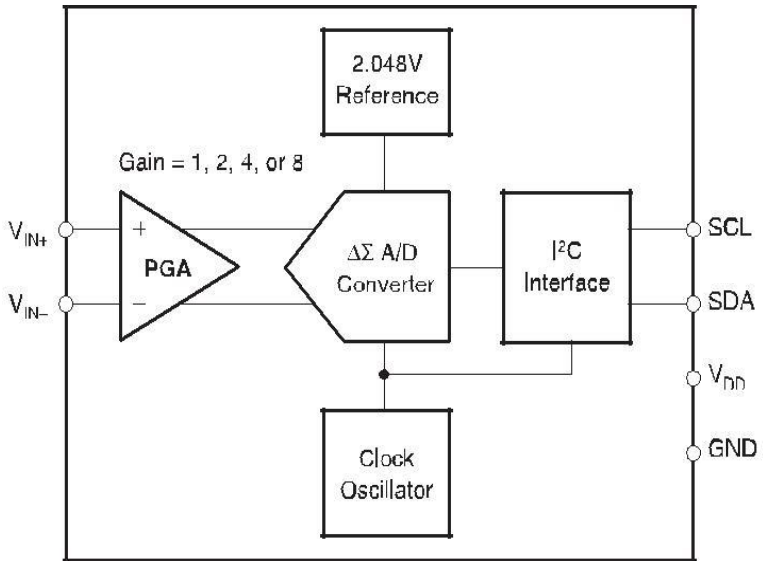
±2.048V differentially. The HT8110A uses an I²C-compatible serial interface and operates from a single power supply ranging from 2.7V to 5.5V.

The HT8110A can perform conversions at rates of 15, 30, 60, or 240 samples per second. The onboard programmable gain amplifier (PGA), which offers gains of up to 8, allows smaller signals to be measured with high resolution. In single-conversion mode, the HT8110A automatically powers down after a conversion, greatly reducing current consumption during idle periods.

The HT8110A is designed for applications requiring high-resolution measurement, where space and power consumption are major considerations. Typical applications include portable instrumentation, industrial process control, and smart transmitters.

APPLICATIONS

- **PORTABLE INSTRUMENTATION**
- **INDUSTRIAL PROCESS CONTROL**
- **SMART TRANSMITTERS**
- **CONSUMER GOODS**
- **FACTORY AUTOMATION**
- **TEMPERATURE MEASUREMENT**



ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND	−0.3V to +6V
Input Current	100mA, Momentary
Input Current	10mA, Continuous
Voltage to GND, V_{IN+}, V_{IN-}	−0.3V to V_{DD} + 0.3V
Voltage to GND, SDA, SCL	−0.5V to 6V
Maximum Junction Temperature	+150°C
Operating Temperature Range	−40 °C to +125°C
Storage Temperature Range	−60 °C to +150°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE/ORDERING INFORMATION

PRODUCT	I^2C ADDRESS	PACKAGE−LEAD	PACKAGE DESIGNATOR (1)	SPECIFIED TEMPERATURE RANGE
HT8110A0	1001 000	SOT23-6	RZ	−40 °C to +85°C

ELECTRICAL CHARACTERISTICS

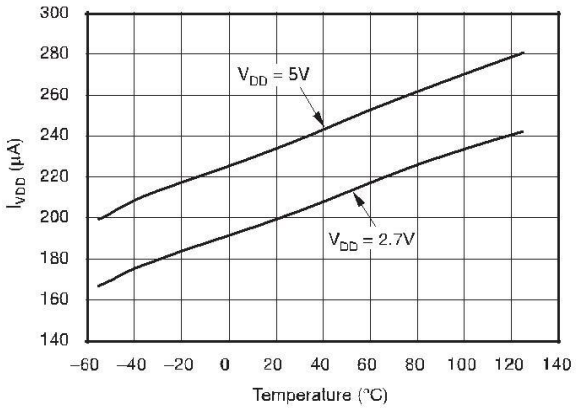
All specifications at −40 °C to +85°C, V_{DD} = 5V, and all PGAs, unless otherwise noted.

PARAMETER	CONDITIONS	HT8110A MIN	HT8110A TYP	HT8110A MAX	UNIT
ANALOG INPUT					
Full-Scale Input Voltage	$(V_{IN+}) - (V_{IN-})$		±2.048/PGA		V
Analog Input Voltage	V_{IN+} to GND or V_{IN-} to GND	GND − 0.2		V_{DD} + 0.2	V
Differential Input Impedance			2.8/PGA		MΩ
Common-Mode Input Impedance	PGA = 1		3.5		MΩ
	PGA = 2		3.5		MΩ
	PGA = 4		1.8		MΩ
	PGA = 8		0.9		MΩ
SYSTEM PERFORMANCE					
Resolution and No Missing Codes	DR = 00	12		12	Bits
	DR = 01	14		14	Bits
	DR = 10	15		15	Bits
	DR = 11	16		16	Bits
Data Rate	DR = 00	180	240	308	SPS
	DR = 01	45	60	77	SPS
	DR = 10	22	30	39	SPS
	DR = 11	11	15	20	SPS
Output Noise	(1)	See Typical Characteristic Curves			
Integral Nonlinearity	DR = 11, PGA = 1, End Point Fit		±0.004	±0.010	% of FSR
Offset Error	PGA = 1		1.2	8	mV
	PGA = 2		0.7	4	mV
	PGA = 4		0.5	2.5	mV
	PGA = 8		0.4	1.5	mV
Offset Drift	PGA = 1		1.2		∝V/°C
	PGA = 2		0.6		∝V/°C
	PGA = 4		0.3		∝V/°C
	PGA = 8		0.3		∝V/°C
Offset vs V_{DD}	PGA = 1		800		∝V/V
	PGA = 2		400		∝V/V
	PGA = 4		200		∝V/V
	PGA = 8		150		∝V/V
Gain Error			0.05	0.40	%
PGA Gain Error Match (3)	Match Between Any Two PGA Gains		0.02	0.10	%
Gain Error Drift			5	40	ppm/°C
Gain vs V_{DD}			80		ppm/V
Common-Mode Rejection	At DC and PGA = 8	95	105		dB
	At DC and PGA = 1		100		dB
DIGITAL INPUT/OUTPUT					
Logic Level					
I_H		0.7 □ V_{DD}		6	V
I_L		GND − 0.5		0.3 □ V_{DD}	V
OL	I_{OL} = 3mA	GND		0.4	V
Input Leakage					
I_H	V_{IH} = 5 .5V			10	∝A
I_L	V_{IL} = GND	−10			∝A
POWER-SUPPLY REQUIREMENTS	V				
Power-Supply Voltage	DD	2.7		5.5	V
Supply Current	Power Down		0.05	2	∝A
	Active Mode		240	350	∝A
Power Dissipation	V_{DD} = 5.0V		1.2	1.75	mW
(1)	V_{DD} = 3.0V		0.675		mW

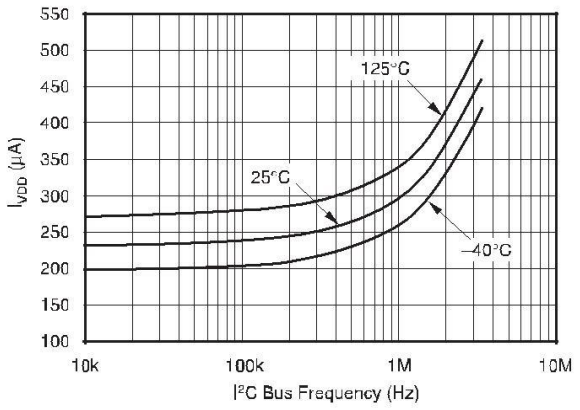
TYPICAL CHARACTERISTICS

At T_A = 25°C and V_{DD} = 5V, unless otherwise noted.

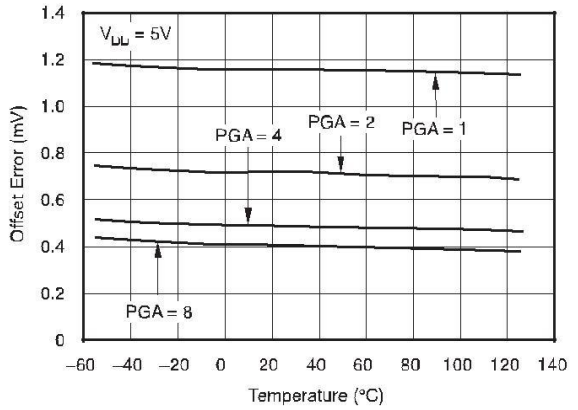
SUPPLY CURRENT vs TEMPERATURE



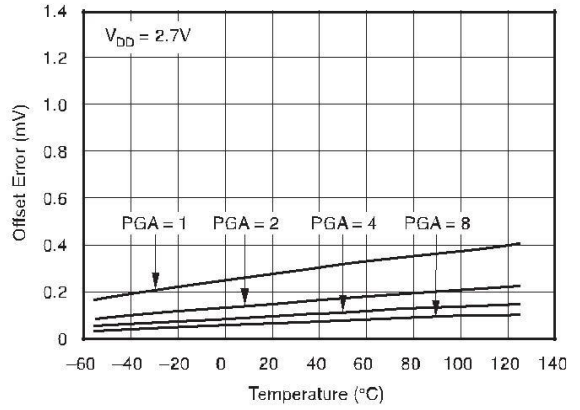
SUPPLY CURRENT vs I²C BUS FREQUENCY



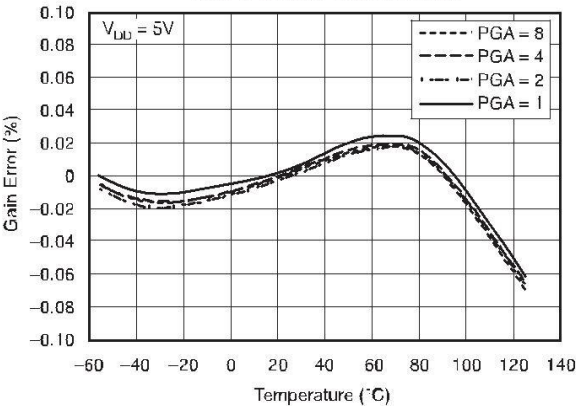
OFFSET ERROR vs TEMPERATURE



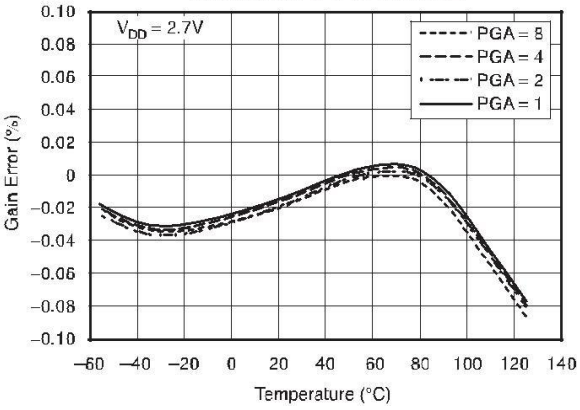
OFFSET ERROR vs TEMPERATURE



GAIN ERROR vs TEMPERATURE



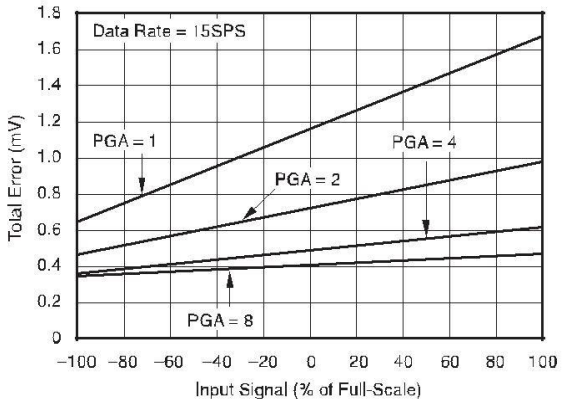
GAIN ERROR vs TEMPERATURE



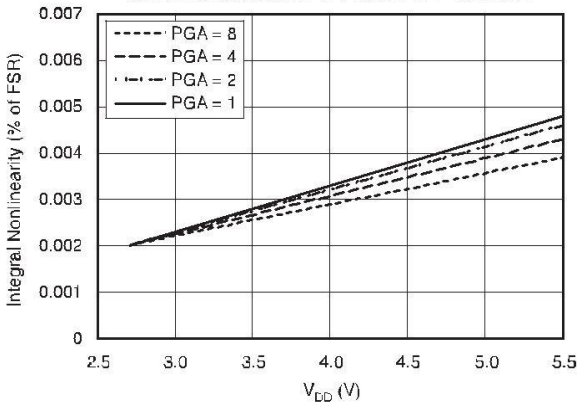
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C and V_{DD} = 5V, unless otherwise noted.

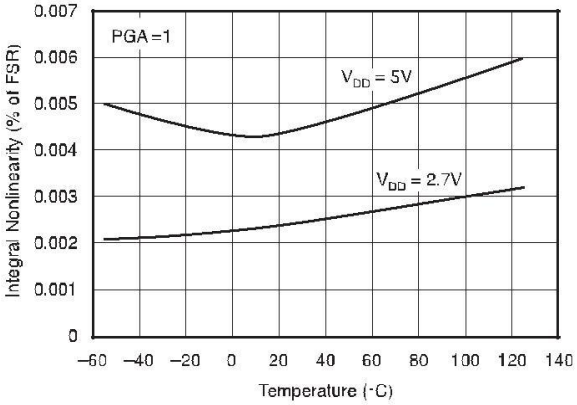
TOTAL ERROR vs INPUT SIGNAL



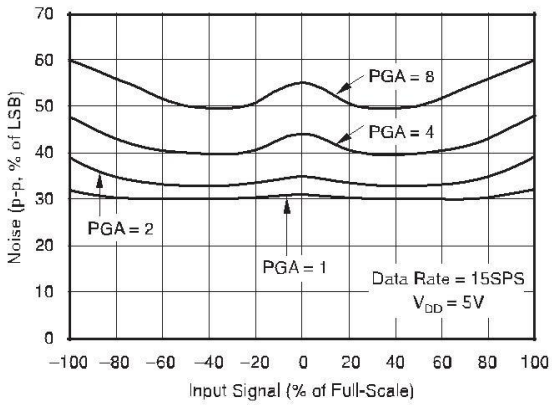
INTEGRAL NONLINEARITY vs SUPPLY VOLTAGE



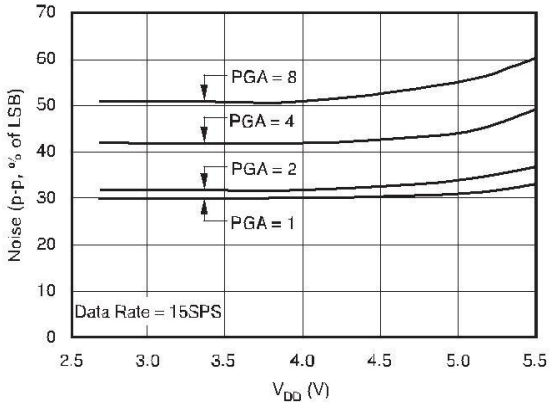
INTEGRAL NONLINEARITY vs TEMPERATURE



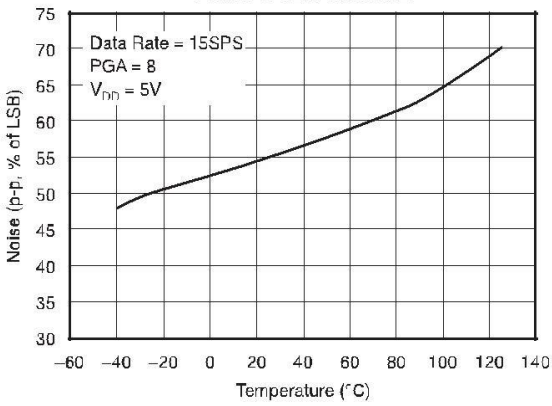
NOISE vs INPUT SIGNAL



NOISE vs SUPPLY VOLTAGE



NOISE vs TEMPERATURE



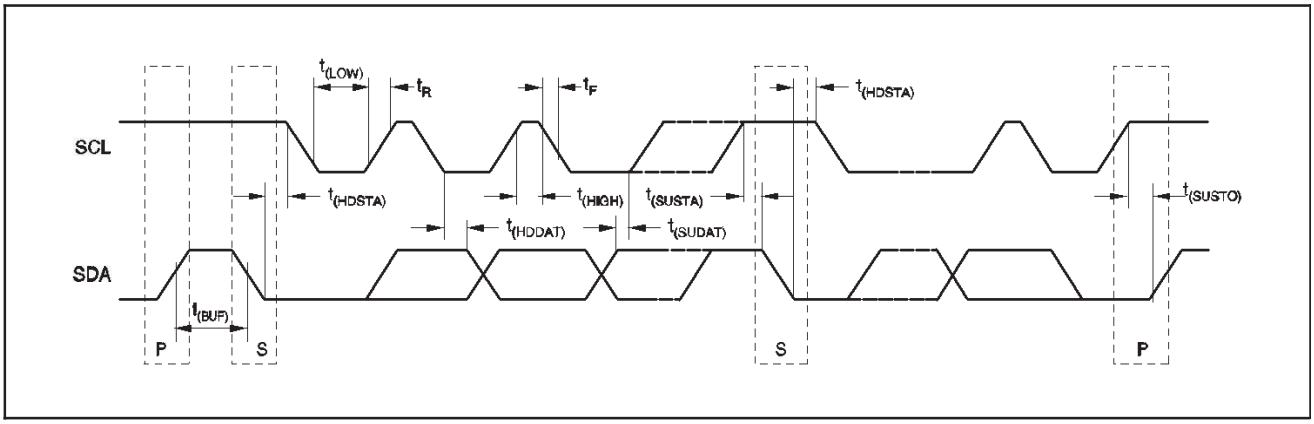


Figure 1. I ^{2}C Timing Diagram

PARAMETER		FAST MODE MIN	FAST MODE MAX	HIGH-SPEED MODE MIN	HIGH-SPEED MODE MAX	UNITS
SCLK operating frequency	$t_{(SCLK)}$		0.4		3.4	MHz
Bus free time between START and STOP condition	$t_{(BUF)}$	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	600		160		ns
Repeated START condition setup time	$t_{(SUSTA)}$	600		160		ns
Stop condition setup time	$t_{(SUSTO)}$	600		160		ns
Data hold time	$t_{(HDDAT)}$	0		0		ns
Data setup time	$t_{(SUDAT)}$	100		10		ns
SCLK clock LOW period	$t_{(LOW)}$	1300		160		ns
SCLK clock HIGH period	$t_{(HIGH)}$	600		60		ns
Clock/data fall time	t_F		300		160	ns
Clock/data rise time	t_R		300		160	ns

Table 3. Timing Diagram Definitions

CONFIGURATION REGISTER

The 8-bit configuration register can be used to control the HT8110A's operating mode, data rate, and PGA settings. The configuration register format is shown in

Table 5. The default setting is 8CH.

BIT	7	6	5	4	3	2	1	0
NAME	ST/DRDY	0	0	SC	DR1	DR0	PGA1	PGA 0
DEFAU LT	1	0	0	0	1	1	0	0

Table 5. Configuration Register

Bit 7: ST/$\overline{\text{DRDY}}$

The meaning of the ST/$\overline{\text{DRDY}}$ bit depends on whether it is being written to or read from.

In single conversion mode, writing a 1 to the ST/$\overline{\text{DRDY}}$ bit causes a conversion to start, and writing a 0 has no effect. In continuous conversion mode, the HT8110A ignores the value written to ST/DRDY.

When read, ST/$\overline{\text{DRDY}}$ indicates whether the data in the output register is new data. If ST/DRDY is 0, the data just read from the output register is new, and has not been read before. If ST/DRDY is 1, the data just read from the output register has been read before.

The HT8110A sets ST/$\overline{\text{DRDY}}$ to 0 when it writes data into the output register. It sets ST/$\overline{\text{DRDY}}$ to 1 after any of the bits in the configuration register have been read. (Note that the read value of the bit is independent of the value written to this bit.)

In continuous-conversion mode, use ST/$\overline{\text{DRDY}}$ to determine when new conversion data is ready. If ST/DRDY is 1, the data in the output register has already been read, and is not new. If it is 0, the data in the output register is new, and has not yet been read.

In single-conversion mode, use ST/$\overline{\text{DRDY}}$ to determine when a conversion has completed. If ST/$\overline{\text{DRDY}}$ is 1, the output register data is old, and the conversion is still in process; if it is 0, the output register data is the result of the new conversion.

Note that the output register is returned from the HT8110A before the configuration register. The state of the ST/DRDY bit applies to the data just read from the output register, and not to the data from the next read operation.

Bits 6−5: Reserved

Bits 6 and 5 must be set to zero.

Bit 4: SC

SC controls whether the HT8110A is in continuous conversion or single conversion mode. When SC is 1, the HT8110A is in single conversion mode; when SC is 0, the HT8110A is in continuous conversion mode. The default setting is 0.

Bits 3−2: DR

Bits 3 and 2 control the HT8110A's data rate, as shown in Table 6.

DR 1	DR 0	DATA RATE
0	0	240SPS
0	1	60SPS
1	0	30SPS
1(1)	1(1)	15SPS(1)

(1) Default setting.

Table 6. DR Bits

Bits 1−0: PGA

Bits 1 and 0 control the HT8110A's gain setting, as shown in Table 7.

PGA1	PGA0	GAIN
0(1)	0(1)	1(1)
0	1	2
1	0	4
1	1	8

(1) Default setting.

Table 7. PGA Bits

READING FROM THE HT8110A

To read the output register and the configuration register from the HT8110A, address the HT8110A for reading, then read three bytes. The first two bytes will be the output register's contents, and the third will be the configuration register's contents.

It is not required to read the configuration register byte. It is permissible to read fewer than three bytes during a read operation.

Reading more than three bytes from the HT8110A has no effect. All bytes following the third will be FF$_H$.

It is possible to ignore the ST/$\overline{DRDY}$ bit and read data from the HT8110A's output register at any time, without regard to whether a new conversion is complete. If the output register is read more than once during a conversion cycle, it will return the same data each time. New data will be returned only when the output register has been updated.

A timing diagram of a typical HT8110A read operation is shown in Figure 2.

WRITING TO THE HT8110A

To write to the configuration register, address the HT8110A for writing, and send one byte. The byte will be written to the configuration register. Note that the output register cannot be written to.

Writing more than one byte to the HT8110A has no effect. The HT8110A will ignore any bytes sent to it after the first one, and it will only acknowledge the first byte.

A timing diagram of a typical HT8110A write operation is shown in Figure 3.

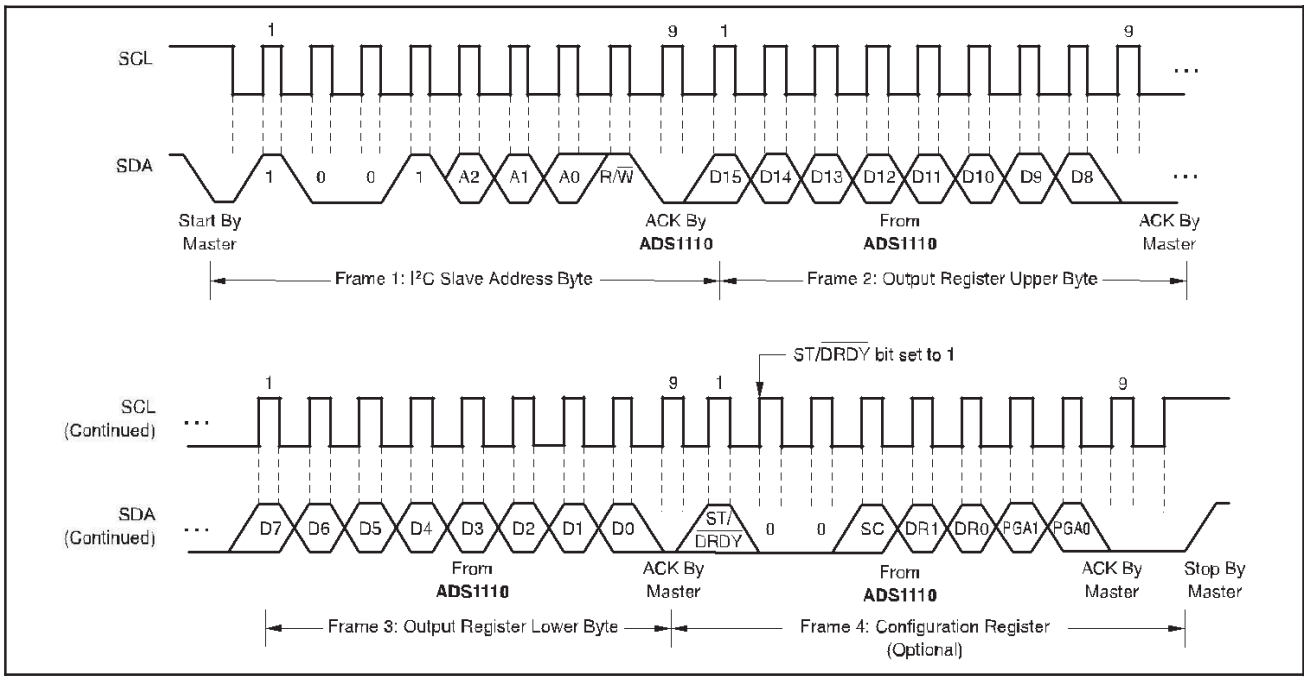


Figure 2. Timing Diagram for Reading From the HT8110A

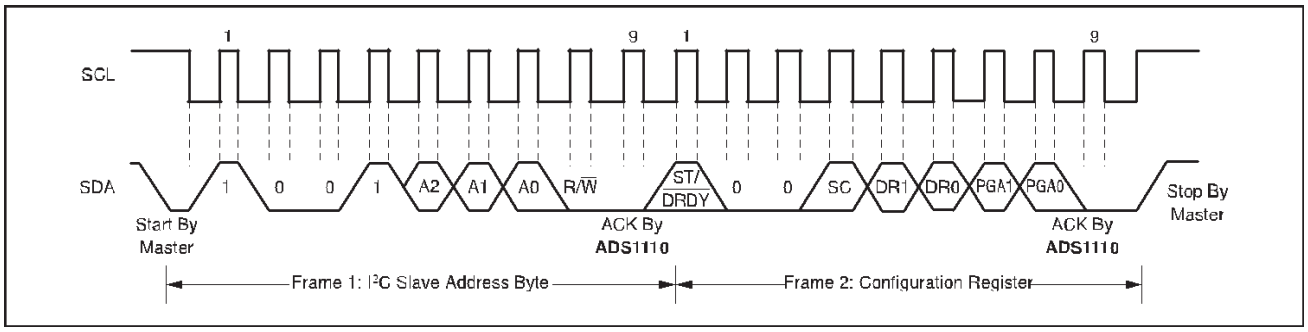
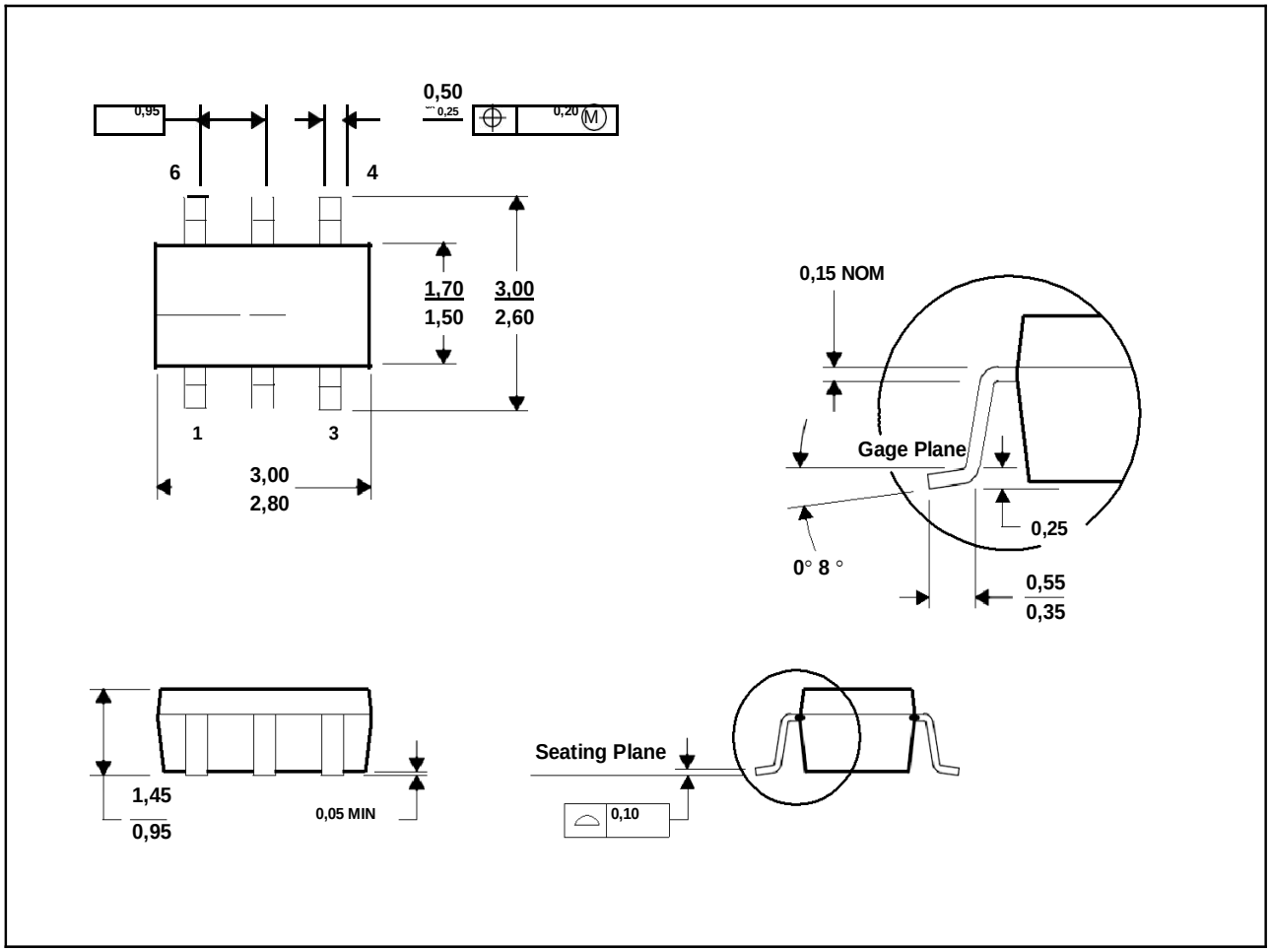


Figure 3. Timing Diagram for Writing To the HT8110A

SOT23-6



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.