NXP Semiconductors
Data Sheet: Advance Information

Document Number MKW40Z160
Rev. 1.2, 05/2018

MKW40Z160 MKW30Z160 MKW20Z160

MKW40Z/30Z/20Z Data Sheet

A Bluetooth® Low Energy and IEEE® 802.15.4 System on a Chip (SoC)
Supports the following:
MKW40Z160VHT4, MKW30Z160VHM4, MKW20Z160VHT4

Key features

- Multi-Standard Radio
  - 2.4 GHz Bluetooth Low Energy version 4.1 compliant
  - IEEE Standard 802.15.4 2011 compliant
  - Typical Receiver Sensitivity (BLE) = -91 dBm
  - Typical Receiver Sensitivity (802.15.4) = -102 dBm
  - Programmable Transmitter Output Power: -18 dBm to +5 dBm
  - Low external component counts for low cost application
- MCU and Memories
  - Up to 48 MHz ARM® Cortex-M0+ core
  - On-chip 160 KB Flash memory
  - On-chip 20 KB SRAM
- Low Power Consumption
  - Typical Rx Current: 6.5 mA (DCDC in buck mode, 3.6 V supply)
  - Typical Tx Current: 8.4 mA (DCDC in buck mode, 3.6 V supply) for a 0 dBm output
  - Low Power Mode (VLLS0) Current: 206 nA
- Clocks
  - 32 MHz Crystal Oscillator
  - 32 kHz Crystal Oscillator
- System peripherals
  - Nine low-power modes to provide power optimization based on application requirements
  - DCDC Converter supporting Buck, Boost, and Bypass modes
  - DMA Controller
  - COP Software watchdog
  - SWD Interface and Micro Trace buffer
  - Bit Manipulation Engine (BME)
- Human-machine interface
  - Touch Sensing Input
  - General-purpose input/output
- Analog modules
  - 16-bit Analog-to-Digital Converter (ADC)
  - 12-bit Digital-to-Analog Converter (DAC)
  - 6-bit High Speed Analog Comparator (CMP)
- Timers
  - 16-bit low-power timer (LPTMR)
  - 3 Timers Modules(TPM): One 4 channels TPM and Two 2 channels TPMs
  - Programmable Interrupt Timer (PIT)
  - Real-Time Clock (RTC)
- Communication interfaces
  - 2 SPI modules
  - 2 I2C modules
  - Low Power UART module
  - Carrier Modulator Timer (CMT)
- Security
  - AES-128 Accelerator (AESA)
  - True Random Number Generator (TRNG)
- Operating Characteristics
  - DCDC Converter supporting Buck, Boost, and Bypass modes
  - Temperature range (ambient): -40 to 85°C

Table of Contents

Introduction

The KW40Z/30Z/20Z (called KW40Z throughout this document) is an ultra low-power, highly integrated single-chip device that enables Bluetooth low energy (BLE) or IEEE Standard 802.15.4 RF connectivity for portable, extremely low-power embedded systems. Applications include portable health care devices, wearable sports and fitness devices, AV remote controls, computer keyboards and mice, gaming controllers, access control, security systems, smart energy and home area networks.

The KW40Z SoC integrates a radio transceiver operating in the 2.36 GHz to 2.48 GHz range supporting a range of FSK/GFSK and O-QPSK modulations, an ARM Cortex-M0+ CPU, 160 KB Flash and 20 KB SRAM, BLE Link Layer hardware, 802.15.4 packet processor hardware and peripherals optimized to meet the requirements of the target applications.

The KW40Z SoC's radio frequency transceiver is compliant with Bluetooth version 4.1 for Low Energy (aka Bluetooth Smart), and the IEEE standard 802.15.4-2011 using O-QPSK in the 2.4 GHz ISM band.

The KW40Z SoC can be used in applications as a "BlackBox" modem by simply adding BLE or IEEE Std. 802.15.4 connectivity to an existing embedded controller system, or used as a stand-alone smart wireless sensor with embedded application where no host controller is required.

NXP provides fully certified protocol stacks and application profiles to support KW40Z. The KW40Z Flash and SRAM memory are available for applications and communication protocols using a choice of NXP or 3rd party software development tools.

The RF section of the KW40Z SoC is optimized to require very few external components, achieving the smallest RF footprint possible on a printed circuit board.

Extremely long battery life is achieved though efficiency of code execution in the Cortex-M0+ CPU core and the multiple low power operating modes of the KW40Z SoC. Additionally, an integrated DC-DC converter enables a wide operating range from 0.9 V to 3.6 V. The DC-DC in Buck mode enables KW40Z to operate from a single coin cell battery with a significant reduction of peak Rx and Tx current consumption. The DC-DC in boost mode enables a single alkaline battery to be used throughout its entire useful voltage range of 0.9 V to 1.795 V.

1 Ordering information

Table 1. Orderable parts details

Device	Operating Temp Range (T_A)	Package	Description
MKW20Z160VHT4(R)	-40 to 85°C	48-pin Laminate QFN	IEEE 802.15.4
MKW30Z160VHM4(R)	-40 to 85°C	32-pin Laminate QFN	Bluetooth Low Energy Only
MKW40Z160VHT4(R)	-40 to 85°C	48-pin Laminate QFN	Bluetooth Low Energy or IEEE 802.15.4

2 Feature Descriptions

This section provides a simplified block diagram and highlights the KW40Z SoC features.

2.1 Block diagram

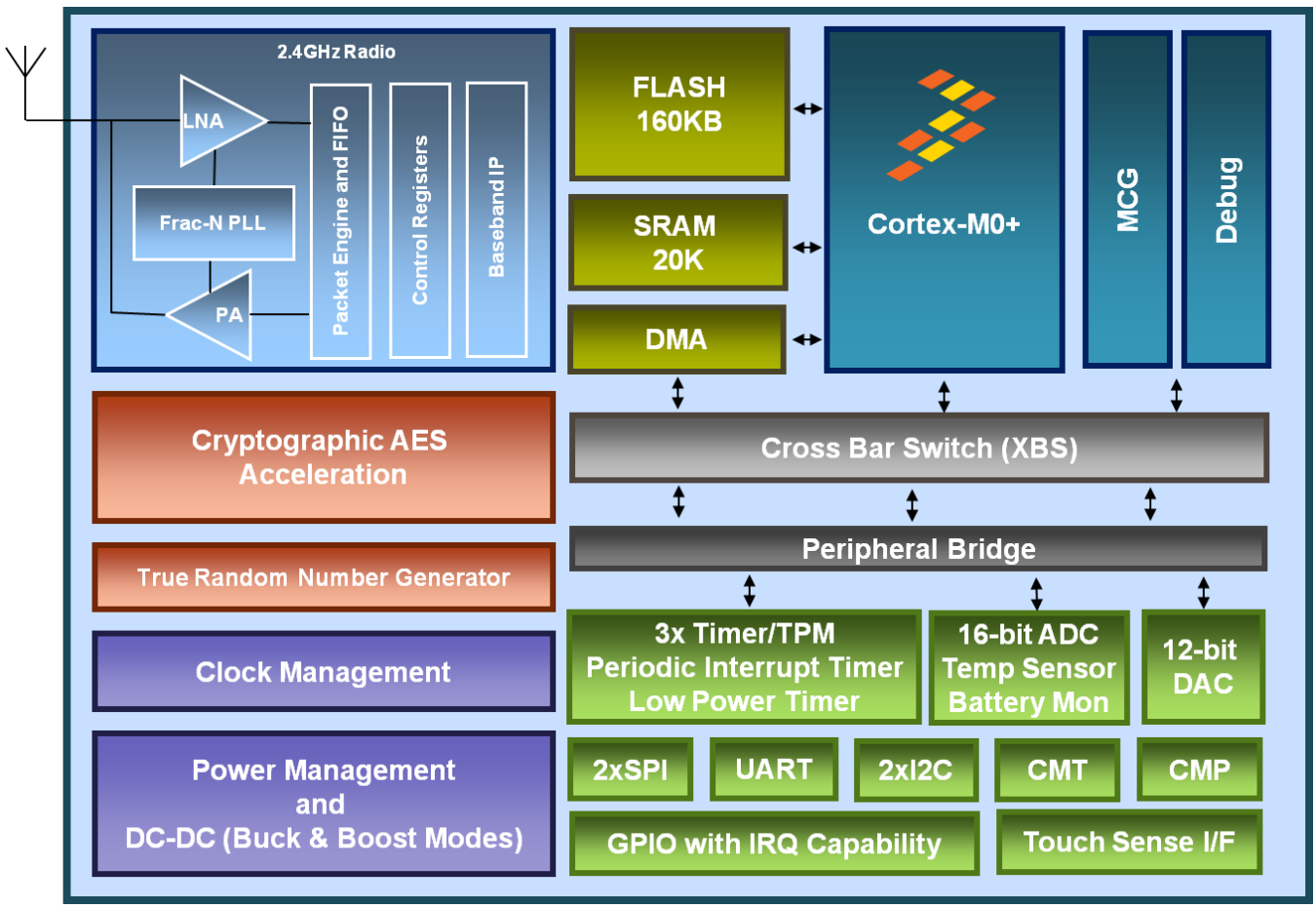


Figure 1. KW40Z/KW30Z/KW20Z simplified block diagram

2.2 Radio features

Operating frequencies:

- 2.4 GHz ISM band (2400-2483.5 MHz)
- MBAN 2360-2400 MHz

Supported standards:

- Bluetooth v4.1 Low Energy compliant 1 Mbps GFSK modulation
- IEEE Std. 802.15.4-2011 compliant O-QPSK modulation
- NXP Thread Networking Stack
- Bluetooth Low Energy(BLE) Application Profiles

Receiver performance:

- Receive sensitivity of -91 dBm for BLE
- Receive sensitivity of -102 dBm typical for IEEE Std. 802.15.4

Other features:

- Programmable transmit output power from -18 dBm to +5 dBm with DC/DC bypass and buck modes of operation
- Bluetooth Low Energy Link Layer hardware
- Hardware acceleration for IEEE Std. 802.15.4 packet processing
- 32 MHz crystal reference oscillator
- Supports antenna diversity option for IEEE Std. 802.15.4
- Supports dual PAN for IEEE Std. 802.15.4 with hardware-assisted address matching acceleration
- Differential RF port shared by transmit and receive
- Low external component count
- Supports transceiver range extension using external PA and/or LNA

2.3 Microcontroller features

ARM Cortex-M0+ CPU

- Up to 48 MHz CPU
- As compared to Cortex-M0, the Cortex-M0+ uses an optimized 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Supports up to 32 interrupt request sources
- Binary compatible instruction set architecture with the Cortex-M0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial Wire Debug (SWD) reduces the number of pins required for debugging
- Micro Trace Buffer (MTB) provides lightweight program trace capabilities using system RAM as the destination memory

Nested Vectored Interrupt Controller (NVIC)

- 32 vectored interrupts, 4 programmable priority levels
- Includes a single non-maskable interrupt

Wake-up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low power modes

- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to very-deep-sleep
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a non-masked interrupt is detected

Debug Controller

- Two-wire Serial Wire Debug (SWD) interface
- Hardware breakpoint unit for 2 code addresses
- Hardware watchpoint unit for 2 data items
- Micro Trace Buffer for program tracing

On-Chip Memory

- 160 KB Flash
  - Firmware distribution protection. Flash can be marked execute-only on a per-sector (4KB) basis to prevent firmware contents from being read by 3rd parties
  - Flash implemented as one 128 KB block and one 32 KB block. Code can execute or read from one block while the other block is being erased or programmed
- 20 KB SRAM
- Security circuitry to prevent unauthorized access to RAM and flash contents through the debugger

2.4 System features

Power Management Control Unit (PMC)

- Programmable power saving modes
- Available wake-up from power saving modes via internal and external sources
- Integrated Power-on Reset (POR)
- Integrated Low Voltage Detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable Low Voltage Warning (LVW) interrupt capability
- Individual peripheral clocks can be gated off to reduce current consumption
- Internal Buffered bandgap reference voltage
- Factory programmed trim for bandgap and LVD
- 1 kHz Low Power Oscillator (LPO)

DC-DC Converter

- Internal switch mode power supply supporting Buck, Boost, and Bypass operating modes

- Buck operation supports external voltage sources of 2.1 V to 3.6 V. This reduces peak current consumption during Rx and Tx by ~25%, ideal for single coin-cell battery operation (typical CR2032 cell).
- Boost operation supports external voltage sources of 0.9 V to 1.795 V, which is efficiently increased to the static internal core voltage level, ideal for single battery operation (typical AA or AAA alkaline cell).
- When DCDC is not used, the device supports an external voltage range of 1.45 V to 3.6 V (1.45 - 3.6 V on VDD_RF1, VDD_RF2, VDD_XTAL and VDD_1P45OUT_PMCIN pins. 1.71 - 3.6 V on VDD_0, VDD_1 and VDDA pins)
- An external inductor is required to support the Buck or Boost modes
- The DCDC Converter 1.8 V output current drive for external devices (MCU in RUN mode, Radio is enabled, other peripherals are disabled)
  - Up to 44 mA in buck mode with VDD_1P8 = 1.8 V
  - Up to 31.4 mA in buck mode with VDD_1P8 = 3.0 V

DMA Controller

- Four independently programmable DMA controller channels provides the means to directly transfer data between system memory and I/O peripherals
- DMA controller is capable of functioning in run and wait modes of operation
- Dual-address transfers via 32-bit master connection to the system bus
- Data transfers in 8-, 16-, or 32-bit blocks
- Continuous-mode or cycle-steal transfers from software or peripheral initiation

DMA Channel Multiplexer (DMA MUX)

- 4 independently selectable DMA channel routers
- 2 periodic trigger sources available
- Each channel router can be assigned to 1 of the peripheral DMA sources

COP Watchdog Module

- Independent clock source input (independent from CPU/bus clock)
- Choice between two clock sources
  - LPO oscillator
  - Bus clock

System Clocks

- 32 MHz crystal reference oscillator provides clock for the radio, and is the main clock option for the MCU
- 32.768 kHz crystal reference oscillator used to maintain precise Bluetooth radio time in low power modes
- Multipurpose Clock Generator (MCG)

- Internal reference clocks — Can be used as a clock source for other on-chip peripherals
  - On-chip RC oscillator range of 31.25 kHz to 39.0625 kHz with 2% accuracy across full temperature range
  - On-chip 4MHz oscillator with 5% accuracy across full temperature range
- Frequency-locked loop (FLL) controlled by internal or external reference
  - 20 MHz to 48 MHz FLL output

Unique Identifiers

- 10 bytes of the Unique ID represents a unique identifier for each chip
- 40 bits of unique MAC address can be used to generate BLE or 802.15.4 device address

2.5 Peripheral features

16-bit Analog-to-Digital Converter (ADC)

- Linear successive approximation algorithm with 16-bit resolution
- Output formatted in 16-, 12-, 10-, or 8-bit right justified format
- Single or continuous conversion
- Configurable sample time and conversion speed / power
- Conversion rates in 16-bit mode with no averaging up to ~500Ksamples/sec
- Input clock selection
- Operation in low power modes for lower noise operation
- Asynchronous clock source for lower noise operation
- Selectable asynchronous hardware conversion trigger
- Automatic compare with interrupt for less-than, or greater than, or equal to programmable value
- Temperature sensor
- Battery voltage measurement
- Hardware average function
- Selectable voltage reverence
- Self-calibration mode

12-Bit Digital-to-Analog Converter (DAC)

- 12-bit resolution
- Guaranteed 6-sigma monotonicity over input word
- High- and low-speed conversions
  - 1 µs conversion rate for high speed, 2 µs for low speed
- Power-down mode

- Automatic mode allows the DAC to generate its own output waveforms including square, triangle, and sawtooth
- Automatic mode allows programmable period, update rate, and range
- DMA support with configurable watermark level

High-Speed Analog Comparator (CMP)

- 6-bit DAC programmable reference generator output
- Up to eight selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
- Two performance modes:
  - Shorter propagation delay at the expense of higher power
  - Low power, with longer propagation delay
- Operational in all MCU power modes

Low Power Timer (LPTMR)

- One channel
- Operation as timer or pulse counter
- Selectable clock for prescaler/glitch filter
  - 1 kHz internal LPO
  - External low power crystal oscillator
  - Internal reference clock
- Configurable glitch filter or prescaler
- Interrupt generated on timer compare
- Hardware trigger generated on timer compare
- Functional in all power modes

Timer/PWM (TPM)

- TPM0: 4 channels, TPM1 and TPM2: 2 channels each
- Selectable source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Generation of hardware triggers
- TPM1 and TPM2: Quadrature decoder with input filters
- Global time base mode shares single time base across multiple TPM instances

Programmable Interrupt Timer (PIT)

- Up to 2 interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency

Real-Time Clock (RTC)

- 32-bit seconds counter with 32-bit alarm
  - Can be invalidated on detection of tamper detect
- 16-bit prescaler with compensation
- Register write protection
  - Hard Lock requires MCU POR to enable write access
  - Soft lock requires system reset to enable write/read access
- Capable of waking up the system from low power modes

Inter-Integrated Circuit (I^2C)

- Two channels
- Compatible with I2C bus standard and SMBus Specification Version 2 features
- Up to 1 Mbps operation
- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low power mode

LPUART

- One channel
- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Programmable 1 or 2 stop bits
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup

- Address match feature in receiver to reduce address mark wakeup ISR overhead
- Interrupt or DMA driven operation
- Receiver framing error detection
- Hardware parity generation and checking
- Configurable oversampling ratio to support from 1/4 to 1/32 bit-time noise detection
- Operation in low power modes
- Hardware Flow Control RTS\CTS
- Functional in Stop/VLPS modes

Serial Peripheral Interface (DSPI)

- Two independent SPI channels
- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Support for both transmit and receive by DMA

Carrier Modulator Timer (CMT)

- Four modes of operation
  - Time; with independent control of high and low times
  - Baseband
  - Frequency shift key (FSK)
  - Direct software control of CMT_IRO signal
- Extended space operation in time, baseband, and FSK modes
- Selectable input clock divider
- Interrupt on end of cycle
- Ability to disable CMT_IRO signal and use as timer interrupt

General Purpose Input/Output (GPIO)

- Hysteresis and configurable pull up device on all input pins
- Independent pin value register to read logic level on digital pin
- All GPIO pins can generate IRQ and wakeup events
- Configurable drive strength on some output pins

Touch Sensor Input (TSI)

- Support up to 16 external electrodes
- Automatic detection of electrode capacitance across all operational power modes

- Internal reference oscillator for high-accuracy measurement
- Configurable software or hardware scan trigger
- Fully support NXP touch sensing software (TSS) library
- Capability to wake MCU from low power modes
- Compensate for temperature and supply voltage variations
- High sensitivity change with 16-bit resolution register
- Configurable up to 4096 scan times
- Support DMA data transfer

Keyboard Interface

- GPIO can be configured to function as a interrupt driven keyboard scanning matrix
  - In the 48pin package there are a total of 28 digital pins
  - In the 32pin package there are a total of 15 digital pins
  - These pins can be configured as needed by the application as GPIO, UART, SPI, I2C, ADC, timer I/O as well as other functions

AES Accelerator (AESA)

- The Advanced Encryption Standard Accelerator (AESA) is a stand-alone symmetric encryption accelerator supporting 128- bit key and data size and the following modes:
  - Electronic Codebook (ECB)
  - Cipher Block Chaining (CBC)
  - Counter (CTR)
  - CTR & CBC-MAC (CCM and CCM*)
  - Cipher-base MAC (CMAC)
  - Extended Cipher Block Chaining Message Authentication Code (XCBC-MAC)
- The AESA supports all BLE and IEEE 802.15.4 packet sizes
- The AESA supports DMA and interrupt-driven operation

True Random Number Generator (TRNG)

- The TRNG is an entropy source
- The TRNG output is intended to be read and used as an input to a deterministic random number generator
- The deterministic random number general will be implemented in software
- A FIPS 180 compliant solution can be realized using the TRNG together with a FIPS compliant determinstic random number generator and SoC-level security

3 Transceiver Description

- Direction Conversion Receiver
- Constant Envelope Transmitter
- 2.36 GHz to 2.483 GHz PLL Range
- Low Transmit and Receive Current Consumption
- Low BOM

3.1 Key Specifications

The KW40Z SoC meets or exceeds all Bluetooth Low Energy v4.1 and IEEE 802.15.4 performance specifications applicable to 2.4 GHz ISM and MBAN (Medical Band Area Network) bands. Key specification for the KW40Z are:

Frequency Band:

- ISM Band: 2400 to 2483.5 MHz
- MBAN Band: 2360 to 2400 MHz

Bluetooth Low Energy v4.1 modulation scheme:

- Symbol rate: 1000 kbps
- Modulation: GFSK
- Receiver sensitivity: -91 dBm, typical
- Programmable transmitter output power: -18 dBm to +5 dBm

IEEE Standard 802.15.4 2.4 GHz modulation scheme:

- Chip rate: 2000 kbps
- Data rate: 250 kbps
- Symbol rate: 62.5 kbps
- Modulation: OQPSK
- Receiver sensitivity: -102 dBm, typical (@1% PER for 20 byte payload packet)
- Differential bidirectional RF input/output port with integrated transmit/receive switch
- Programmable transmitter output power: -18 dBm to +5 dBm

3.2 Frequency Plan for Bluetooth Low Energy

This section describes the frequency plan / channels associated with 2.4GHz ISM and MBAN bands for Bluetooth Low Energy.

2.4GHz ISM Channel numbering:

- Fc=2402 + K * 2 MHz, K=0,.....,39.

MBAN Channel numbering:

- Fc=2363 + 5*K in MHz, for K=0,.....,6)
- Fc=2367 + 5*(K-7) in MHz, for K=7,8.....,13)

Table 2. 2.4 GHz ISM and MBAN frequency plan and channel designations

2.4 GHz ISM[1]		MBAN[2]		2.4GHz ISM + MBAN	
Channel	Freq (MHz)	Channel	Freq (MHz)	Channel	Freq (MHz)
0	2402	0	2360	28	2390
1	2404	1	2361	29	2391
2	2406	2	2362	30	2392
3	2408	3	2363	31	2393
4	2410	4	2364	32	2394
5	2412	5	2365	33	2395
6	2414	6	2366	34	2396
7	2416	7	2367	35	2397
8	2418	8	2368	36	2398
9	2420	9	2369	0	2402
10	2422	10	2370	1	2404
11	2424	11	2371	2	2406
12	2426	12	2372	3	2408
13	2428	13	2373	4	2410
14	2430	14	2374	5	2412
15	2432	15	2375	6	2414
16	2434	16	2376	7	2416
17	2436	17	2377	8	2418
18	2438	18	2378	9	2420
19	2440	19	2379	10	2422
20	2442	20	2380	11	2424
21	2444	21	2381	12	2426
22	2446	22	2382	13	2428
23	2448	23	2383	14	2430
24	2450	24	2384	15	2432
25	2452	25	2385	16	2434
26	2454	26	2386	17	2436
27	2456	27	2387	18	2438
28	2458	28	2388	19	2440
29	2460	29	2389	20	2442
30	2462	30	2390	21	2444
31	2464	31	2391	22	2446
32	2466	32	2392	23	2448

Table continues on the next page...

Table 2. 2.4 GHz ISM and MBAN frequency plan and channel designations (continued)

2.4 GHz ISM[1]		MBAN[2]		2.4GHz ISM + MBAN	
Channel	Freq (MHz)	Channel	Freq (MHz)	Channel	Freq (MHz)
33	2468	33	2393	24	2450
34	2470	34	2394	25	2452
35	2472	35	2395	26	2454
36	2474	36	2396	27	2456
37	2476	37	2397	37	2476
38	2478	38	2398	38	2478
39	2480	39	2399	39	2480

1. ISM frequency of operation spans from 2400.0 MHz to 2483.5 MHz
2. Per FCC guideline rules, IEEE (R) 802.15.1 and Bluetooth Low Energy V4.0 single mode operation is allowed in these channels.

3.3 Frequency Plan for 802.15.4 and 802.15.4j (MBAN)

This section describes the frequency plan / channels associated with 2.4GHz ISM and MBAN bands for 802.15.4.

2.4GHz ISM Channel numbering:

- Fc=2402.0 + 5*(K-11) MHz, K=11, 12, ..,26.

MBAN Channel numbering:

- Fc=2363.0 + 5*K in MHz, for K=0,.....,6)
- Fc=2367.0 + 5*(K-7) in MHz, for K=7,.....,14)

Table 3. 2.4 GHz ISM and MBAN frequency plan and channel designations

2.4 GHz ISM		MBAN[1]	
Channel #	Frequency (MHz)	Channel #	Frequency (MHz)
11	2405	0	2363
12	2410	1	2368
13	2415	2	2373
14	2420	3	2378
15	2425	4	2383
16	2430	5	2388
17	2435	6	2393
18	2440	7	2367

Table continues on the next page...

Table 3. 2.4 GHz ISM and MBAN frequency plan and channel designations (continued)

2.4 GHz ISM		MBAN[1]	
Channel #	Frequency (MHz)	Channel #	Frequency (MHz)
19	2445	8	2372
20	2450	9	2377
21	2455	10	2382
22	2460	11	2387
23	2465	12	2392
24	2470	13	2397
25	2475	14	2395
26	2480		

1. Usable channel spacing to assit in co-existence.

3.4 Transceiver Functions

Receive

- The receiver architecture is Zero IF (ZIF) where the received signal after passing through RF front end is down-converted to a baseband signal. The signal is filtered and amplified before it is fed to a sigma-delta analog-to-digital converter. The digital signal is then decimated to a baseband clock frequency before it is digitally processed, demodulated and passed on to packet processing.

Transmit

- The transmitter transmits O-QPSK or GFSK/FSK modulation having power and channel selection adjustment per user application. After the channel of operation is determined, coarse and fine tuning is executed within the Frac-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is then routed to a multi-stage amplifier for transmission. The differential signals at the output of the PA (RF_P, RF_N) are converted as single ended (SE) signals with off chip components as required.

4 System and Power Management

4.1 Power Management

The KW40Z SoC includes internal power management features that can be used to control the power usage. The power management of the KW40Z includes power management controller (PMC) and a DCDC converter which can operate in a buck, boost or bypass configuration. The PMC is designed such that the RF radio will remain in state-retention while the core is in various stop modes. It can make sure the device can stay in low current consumption mode while the RF radio can wakeup quick enough for communication.

4.1.1 DCDC Converter

The features of the DCDC converter include the following:

- Single inductor, multiple outputs
- Buck and boost modes (pin selectable; CFG=VDCDC_IN -> buck; CFG=GND -> boost)
- Continuous or pulsed operation (hardware/software configurable)
- Power switch input to allow external control of power up, and to select bypass mode
- Output signal to indicate power stable. Purpose is for the rest of the chip to use as a POR
- Scaled battery output voltage suitable for SAR ADC utilization
- Internal oscillator for support when the reference oscillator is not present
- 1.8V output is capable to supply external device: max 38.9mA (V1P8 = 1.8V, VDCDC_IN = 3.0V) and 20.9mA (V1P8 = 3.0V, VDCDC_IN = 3.0V), with MCU in RUN mode, peripherals are disabled

4.2 Modes of Operation

The ARM Cortex-M0+ core in the KW40Z SoC has three primary modes of operation: Run, Wait, and Stop modes. For each run mode, there is a corresponding wait and stop mode. Wait modes are similar to ARM sleep modes. Stop modes are similar to ARM deep sleep modes. The very low power run (VLPR) operation mode can drastically reduce runtime power when the maximum bus frequency is note required to handle the application needs.

The WFI instruction invokes both wait and stop modes for KW40Z. The primary modes are augmented in a number of ways to provide lower power based on application needs.

4.2.1 Power modes

The power management controller (PMC) provides multiple power options to allow the user to optimize power consumption for the level of functionality needed.

Depending on the stop requirements of the user application, a variety of stop modes are available that provide state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation. The following table compares the various power modes available.

For each run mode there is a corresponding wait and stop mode. Wait modes are similar to ARM sleep modes. Stop modes (VLPS, STOP) are similar to ARM sleep deep mode. The very low power run (VLPR) operating mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The three primary modes of operation are run, wait and stop. The WFI instruction invokes both wait and stop modes for the chip. The primary modes are augmented in a number of ways to provide lower power based on application needs.

Table 4. Power modes (At 25 deg C)

Power mode	Description	CPU recovery method	Radio
Normal Run (all peripherals clock off)	Allows maximum performance of chip.	—	Radio can be active
Normal Wait - via WFI	Allows peripherals to function, while allowing CPU to go to sleep reducing power.	Interrupt	
Normal Stop - via WFI	Places chip in static state. Lowest power mode that retains all registers while maintaining LVD protection.	Interrupt	
PStop2 (Partial Stop 2)	Core and system clocks are gated. Bus clock remains active. Masters and slaves clocked by bus clock reamin in Run or VLPRun mode. The clock generators in MCG and the on-chip regulator in the PMC also remain in Run or VLPRun mode.	Interrupt	
PStop1 (Partial Stop 1)	Core, system clocks and bus clock are gated. All bus masters and slaves enter Stop mode. The clock generators in MCG and the on-chip regulator in the PMC also remain in Run or VLPRun mode.	Interrupt	
VLPR (Very Low Power Run) (all peripherals off)	Reduced frequency (1MHz) Flash access mode, regulator in low power mode, LVD off. Internal oscillator can provide low power 4 MHz source for core. (Values @2MHz core/ 1MHz bus and flash, module off, execution from flash). Biasing is disabled when DCDC is configured for continuous mode in VLPR/W	—	Radio operation is possible only when DCDC is configured for continuous mode.[1] However, there may be insufficient MIPS with a 4MHz MCU to support much in the way of radio operation.
VLPW (Very Low Power Wait) - via WFI (all peripherals off)	Similar to VLPR, with CPU in sleep to further reduce power. (Values @4MHz core/ 1MHz bus, module off) Biasing is disabled when DCDC is configured for continous mode in VLPR/W	Interrupt	

Table continues on the next page...

Table 4. Power modes (At 25 deg C) (continued)

Power mode	Description	CPU recovery method	Radio
VLPS (Very Low Power Stop) via WFI	Places MCU in static state with LVD operation off. Lowest power mode with ADC and all pin interrupts functional. LPTMR, RTC, CMP, TSI can be operational. Biasing is disabled when DCDC is configured for continuous mode in VLPS	Interrupt	
LLS3 (Low Leakage Stop)	State retention power mode. LLWU, LPTMR, RTC, CMP, TSI can be operational. All of the radio Sea of Gates(SOG) logic is in state retention	Wakeup Interrupt	Radio SOG is in state retention in LLSx. The BTLL DSM[2] logic can be active using the 32kHz clock
LLS2 (Low Leakage Stop)	State retention power mode. LLWU, LPTMR, RTC, CMP, TSI can be operational. Only 4KBytes of RAM retained.All of the radio SOG logic is in state retention	Wakeup Interrupt	
VLLS3 (Very Low Leakage Stop3)	Full SRAM retention. LLWU, LPTMR, RTC, CMP, TSI can be operational. All of the radio SOG logic is in state retention	Wakeup Reset	Radio SOG is in state retention in VLLS3/2. The BTLL DSM logic can be active using the 32kHz clock
VLLS2 (Very Low Leakage Stop2)	Partial SRAM retention. 4KBytes of RAM retained. LLWU, LPTMR, RTC, CMP, TSI can be operational.All of the radio SOG logic is in state retention	Wakeup Reset	
VLLS1 (Very Low Leakage Stop1) with RTC + 32kHz OSC	All SRAM powered off. The 32-byte system register file remains powered for customer-critical data. LLWU, LPTMR, RTC, CMP can be operational. Radio logic is power gated.	Wakeup Reset	Radio operation not supported. The Radio SOG is power-gated in VLLS1/0. Radio state is lost at VLLS1 and lower power states
VLLS1 (Very Low Leakage Stop1) with LPTMR + LPO	All SRAM powered off. The 32-byte system register file remains powered for customer-critical data. LLWU, LPTMR, RTC, CMP, TSI can be operational.	Wakeup Reset	
VLLS0 (Very Low Leakage Stop0) with Brown-out Detection	VLLS0 is not supported with DCDC The 32-byte system register file remains powered for customer-critical data. Disable all analog modules in PMC and retains I/O state and DGO state. LPO disabled, POR brown-out detection enabled, Pin interrupt only. Radio logic is power gated.	Wakeup Reset	Radio operation not supported. The Radio digital is power-gated in VLLS1/0
VLLS0 (Very Low Leakage Stop0)	VLLS0 is not supported with DCDC buck/boost configuration but is supported with bypass configuration The 32-byte system register file remains powered for customer-critical data. Disable all analog modules in PMC and retains I/O state and DGO state. LPO disabled, POR brown-out detection disabled, Pin interrupt only. Radio logic is power gated.	Wakeup Reset	

1. Biasing is disabled, but the Flash is in a low power mode for VLPx, so this configuration can realize some power savings over use of Run/Wait/Stop
2. DSM refers to BTLL's deepsleep mode. DSM does not refer to the ARM sleep deep mode.

5 Transceiver Electrical Characteristics

5.1 Recommended radio operating conditions

Table 5. Recommended operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
RF and Analog Power Supply Voltage	VDD_{RF1}, VDD_{RF2}, VDD_{XTAL}	1.45	2.7	3.6	Vdc
Input Frequency	fin	2.360	—	2.480	GHz
Ambient Temperature Range	TA	-40	25	85	°C
Logic Input Voltage Low	VIL	0	—	30% VDD_{INT} [1]	V
Logic Input Voltage High	VIH	70% VDD_{INT}	—	VDD_{INT}	V
SPI Clock Rate	f_{SPI}	—	—	16.0	MHz
RF Input Power	Pmax	—	—	0	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 Standard.)	fref	32 MHz only			

1. VDD_{INT} is the internal LDO regulated voltage supplying various circuit blocks, VDD_{INT}=1.2 V

5.2 Receiver Feature Summary

Table 6. Top Level Receiver Specifications (TA=25°C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Supply current power down on VDD_RFx supplies	I_{pdn}	—	200	1000	nA
Supply current Rx On with DC-DC converter enable (Buck; Vbat = 3.6V)	I_{Rxon}	—	6.5	—	mA
Supply current Rx On with DC-DC converter disabled (Bypass) [2]	I_{Rxon}	—	15.4	—	mA
Input RF Frequency	f_{in}	2.360	—	2.4835	GHz
BLE Rx Sensitivity [3]	$SENS_{BLE}$	—	-91	—	dBm
IEEE 802.15.4 Rx Sensitivity [4]	$SENS_{15.4}$	—	-102	—	dBm
Noise Figure for max gain mode @ typical sensitivity	NF_{HG}	—	6.5	—	dB
Receiver Signal Strength Indicator Range	$RSSI_{Range}$	-96	—	0	dBm
Receiver Signal Strength Indicator Resolution	$RSSI_{Res}$	—	1	—	dB

Table continues on the next page...

Table 6. Top Level Receiver Specifications (TA=25°C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
BLE Co-channel Interference (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz).			-6		dB
IEEE 802.15.4 Co-channel Interference (Wanted signal 3 dB over reference sensitivity level)	$C/I_{CO\text{-}channel}$	—	0	—	dB
Adjacent/Alternate Channel Performance[5]					
BLE Adjacent +/- 1 MHz Interference offset (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz.)	$C/I_{BLE,\ 1\ MHz}$	—	-4	—	dB
BLE Adjacent +/- 2 MHz Interference offset (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz.)	$C/I_{BLE,\ 2\ MHz}$	—	28	—	dB
BLE Alternate ≥ +/-3 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.)	$C/I_{BLE,\ 3\ MHz}$	—	35	—	dB
IEEE 802.15.4 Adjacent +/- 5 MHz Interference offset (Wanted signal 3 dB over reference sensitivity level , PER <1%)		—	43	—	dB
IEEE 802.15.4 Alternate ≥ +/- 10 MHz Interference offset (Wanted signal 3 dB over reference sensitivity level , PER <1%.)		—	50	—	dB
Blocking Performance[5]					
BLE Out of band blocking from 30 MHz to 2000 MHz (Wanted signal at -67 dBm , BER <0.1%. Interferer continuous wave signal.)	—	—	-30	—	dBm
BLE Out of band blocking from 2003 MHz to 2339 MHz (Wanted signal at -67 dBm, BER <0.1%. Interferer continuous wave signal.)	—	—	-35	—	dBm
BLE Out of band blocking from 2484 MHz to 2997 MHz (Wanted signal at -67 dBm , BER <0.1%. Interferer continuous wave signal.)	—	—	-35	—	dBm
BLE Out of band blocking from 3000 MHz to 12750 MHz (Wanted signal at -67 dBm , PER<1%, Interferer continuous wave signal.)	—	—	-30	—	dBm
IEEE 802.15.4 Out of band blocking for frequency offsets > 10 MHz (Wanted signal 3 dB over reference sensitivity level , PER <1%. Interferer continuous wave signal.)		—	-44	—	dBm
Spurious Emission < 1.6 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc|< 1.6MHz	—	—	-50	—	dBc
Spurious Emission > 2.5 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc|> 2.5 MHz[6]	—	—	-63	—	dBc

1. All the RX parameters are measured at the KW40 RF pins
2. Transceiver power consumption

3. Measured at 0.1% BER using 37 byte long packets in max gain mode and nominal conditions
4. In max gain mode and nominal conditions
5. BLE Adjacent and Block parameters are measured with modulated interference signals
6. Exceptions allowed for reference frequency multiples

5.3 Transmit and PLL Feature Summary

- Supports constant envelope modulation of 2.4 GHz ISM and 2.36 GHz MBAN frequency bands
- Fast PLL Lock time: < 50 µs
- Reference Frequency: 32 MHz
- Low Integrated Phase Noise: -81 dBVrms (1 kHz to 1 MHz)

Table 7. Top level Transmitter Specifications (TA=25°C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Supply current power down on VDD_RFx supplies	I_{pdn}	—	200	—	nA
Supply current Tx On with P_{RF} = 0dBm and DC-DC converter enabled (Buck; Vbat = 3.6V)	I_{Txone}	—	8.4	—	mA
Supply current Tx On with P_{RF} = 0dBm and DC-DC converter disabled (Bypass) [2]	I_{Txond}	—	18.5	—	mA
Output Frequency	fin	2.360	—	2.4835	GHz
Maximum RF Output power	$P_{RF,max}$	—	5	—	dBm
Minimum RF Output power [3]	$P_{RF,min}$	—	-18	—	dBm
RF Output power control range	P_{RFCR}	—	23	—	dB
IEEE 802.15.4 Peak Frequency Deviation	$F_{dev15.4}$	—	±500	—	kHz
IEEE 802.15.4 Error Vector Magnitude[4]	$EVM_{15.4}$		8		%
IEEE 802.15.4 Offset Error Vector Magnitude[5]	$OEVM_{15.4}$		2		%
IEEE 802.15.4 TX spectrum level at 3.5MHz offset[4, 6]	$TXPSD_{15.4}$			-30	dBc
BLE TX Output Spectrum 20dB BW	$TXBW_{BLE}$		1.0	—	MHz
BLE average frequency deviation using a 00001111 modulation sequence	$\Delta f1_{avg,BLE}$		250		kHz
BLE average frequency deviation using a 01010101 modulation sequence	$\Delta f2_{avg,BLE}$		210		kHz
BLE Maximum Deviation of the Center Frequency[7]	$F_{cdev,BLE}$	—	±10	—	kHz
BLE Adjacent Channel Transmit Power at 2MHz offset[6]	$P_{RF2MHz,BLE}$	—	—	-35	dBm
BLE Adjacent Channel Transmit Power at >= 3MHz offset[6]	$P_{RF3MHz,BLE}$	—	—	-45	dBm
BLE Frequency Hopping Support			YES		

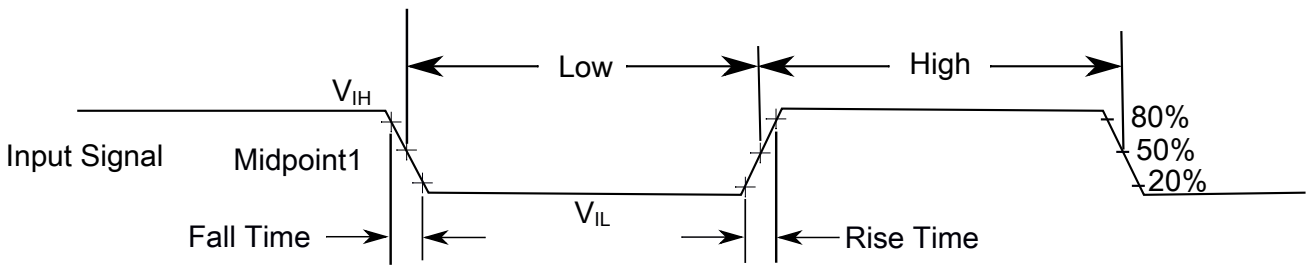
1. All the TX parameters are measured at test hardware SMA connector
2. Transceiver power consumption, Pout = 0 dBm
3. Measured at the KW40 RF pins
4. Measured as per IEEE Std. 802.15.4-2011
5. Offset EVM is computed at one point per symbol, by combining the I value from the beginning of each symbol and the Q value from the middle of each symbol into a single complex value for EVM computations

6. Measured at Pout = 5dBm and recommended TX match
7. Maximum drift of carrier frequency of the PLL during a BLE packet with a nominal 32MHz reference crystal

6 MCU Electrical Characteristics

6.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Slew rate disabled
- Normal drive strength

6.2 Nonswitching electrical specifications

6.2.1 Voltage and current operating requirements

Table 8. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	

Table continues on the next page...

Table 8. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICIO}	IO pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-3	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|.
2. Open drain outputs must be pulled to V_{DD}.

6.2.2 LVD and POR operating requirements

Table 9. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					
V_{LVW1H}	• Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
	Low-voltage warning thresholds — low range					1

Table continues on the next page...

Table 9. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW1L}	• Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	—

1. Rising thresholds are falling threshold + hysteresis voltage

6.2.3 Voltage and current operating behaviors

Table 10. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad (except RESET_b)				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -2.5 mA	V_{DD} – 0.5	—	V	
V_{OH}	Output high voltage — High drive pad (except RESET_b)				2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	—	0.5	V	
V_{OL}	Output low voltage — High drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	3
I_{IN}	Input leakage current (total all pins) for full temperature range	—	65	µA	3
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	20	50	kΩ	4

1. PTB0-1 and PTC0-3 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at V_{DD} = 3.6 V
4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

6.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLSx→RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

Table 11. Power mode transition operating behaviors

Symbol	Description	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	300	µs	1
	• VLLS0 → RUN	147	µs	
	• VLLS1 → RUN	144	µs	
	• VLLS3 → RUN	76	µs	
	• LLS → RUN	5.8	µs	
	• VLPS → RUN	6.2	µs	
	• STOP → RUN	6.2	µs	

1. Normal boot (FTFA_FOPT[LPBOOT]=11). When the DCDC converter is in bypass mode, TPOR will not meet the 300µs spec when 1) VDD_1P45 < 1.6V at 25°C and 85°C. 2) 1.45V ≤ VDD_1P45 ≤ 1.8V. For the bypass mode special case where VDD_1P45 = VDD_1P8, TPOR did not meet the 300µs maximum spec when the supply slew rate <=100V/s.

6.2.5 Power consumption operating behaviors

Table 12. Power consumption operating behaviors

Symbol	Description	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	See note	mA	1
$I_{DD\_RUNCO\_CM}$	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus disabled, LPTMR running using 4 MHz internal reference clock, CoreMark benchmark code executing from flash • at 3.0 V	6.1	7.2	mA	2
I_{DD_RUNCO}	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash • at 3.0 V	3.8	5.2	mA	
I_{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash • at 3.0 V	4.8	6.3	mA	3

I_{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash
	• at 3.0 V
	  • at 25 °C
	  • at 85 °C
		
		6.1
		
		6.3
			
			6.4
			
			6.6
				
				mA
				
				mA
					3

I_{DD_WAIT}	Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled • at 3.0 V	3.0	4.4	mA	3
I_{DD_WAIT}	Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled • at 3.0 V	2.3	3.7	mA	3
I_{DD_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus • at 3.0 V	2.2	3.7	mA	3
$I_{DD\_VLPRCO\_CM}$	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, LPTMR running with 4 MHz internal reference clock, CoreMark benchmark code executing from flash • at 3.0 V	0.732	2.5	mA	5
I_{DD_VLPRCO}	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash • at 3.0 V	145	485	µA	

Table continues on the next page...

Table 12. Power consumption operating behaviors (continued)

Symbol	Description	Typ.	Max.	Unit	Notes
I_{DD_VLPR}	Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash • at 3.0 V	180	515	µA	6
I_{DD_VLPR}	Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash • at 3.0 V	227	572	µA	4, 6
I_{DD_VLPW}	Very-low-power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled • at 3.0 V	125	515	µA	6
I_{DD_STOP}	Stop mode current at 3.0 V				
	at 25 °C	200	215	µA	
	at 50 °C	217	239	µA	
	at 70 °C	251	304	µA	
	at 85 °C	304	405	µA	
I_{DD_VLPS}	Very-low-power stop mode current at Bypass mode(3.0 V), 25 °C	2.9	4.3	µA	
	Very low power stop mode current at Buck mode[7], 25°C	2.3	6.6	µA	
	Very low power stop mode current at Boost mode[8], 25°C	6	14.3	µA	
I_{DD_LLS3}	Low-leakage stop mode 3 current at Bypass mode(3.0 V), 25 °C	2.2	2.7	µA	
	Low-leakage stop mode 3 current at Buck mode[7], 25°C	3.07	10.4	µA	
	Low-leakage stop mode 3 current at Boost mode[8], 25°C	5.11	8.71	µA	
I_{DD_LLS2}	Low-leakage stop mode 2 current at Bypass mode(3.0 V), at 25 °C	2.1	2.4	µA	
	Low-leakage stop mode 2 current at Buck mode[7], 25°C	2.30	6.92	µA	
	Low-leakage stop mode 2 current at Boost mode[8], 25°C	5.06	8.92	µA	
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current at Bypass mode(3.0 V), at 25 °C	1.7	2.1	µA	
	Very-low-leakage stop mode 3 current at Buck mode[7], 25°C	1.39	2.44	µA	
	Very-low-leakage stop mode 3 current at Boost mode[8], 25°C	3.70	6.31	µA	
I_{DD_VLLS2}	Very-low-leakage stop mode 2 current at Bypass mode(3.0 V), at 25 °C	1.6	1.8	µA	
		1.43	2.19	µA	

Table continues on the next page...

Table 12. Power consumption operating behaviors (continued)

Symbol	Description	Typ.	Max.	Unit	Notes
	Very-low-leakage stop mode 2 current at Buck mode[7], 25°C	3.45	5.08	µA	
	Very-low-leakage stop mode 2 current at Boost mode[8], 25°C				
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current at Bypass mode(3.0 V), at 25°C	992	1103	nA	
	Very-low-leakage stop mode 1 current at Buck mode[7], 25°C	1.04	1.58	µA	
	Very-low-leakage stop mode 1 current at Boost mode[8], 25°C	2.50	3.7	µA	
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V			nA	
	at 25 °C	390	495	µA	
	at 50 °C	1.2	1.5	µA	
	at 70 °C	3.1	4.3	µA	
	at 85 °C	6.6	8.7		
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V				9
	at 25 °C	206	309	nA	
	at 50 °C	1	1.9	µA	
	at 70 °C	3.1	4.5	µA	
	at 85 °C	6.6	10.8	µA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for PEE mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
6. MCG configured for BLPI mode.
7. DCDC_IN = 3.0V, VDD1P8 = 1.8V, VDD1P45 = 1.45V with 10uF on both VDD1P8 and VDD1P45 pins
8. DCDC_IN = 1.3V, VDD1P8 = 1.8V, VDD1P45 = 1.45V with 10uF on both VDD1P8 and VDD1P45 pins
9. No brownout

Table 13. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)					Unit
		-40	25	50	70	85	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	µA

Table continues on the next page...

Table 13. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)					Unit
		-40	25	50	70	85	
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the RTC bits. Measured by entering all modes with the crystal enabled.						
	VLLS1	440	490	540	560	570	
	VLLS3	440	490	540	560	570	nA
	LLS	490	490	540	560	570	
	VLPS	510	560	560	560	610	
	STOP	510	560	560	560	610	
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.						
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	µA
		259	271	275	277	281	
I_{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.						
	MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	µA
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low-power mode using the internal clock and continuous conversions.	366	366	366	366	366	µA

6.2.6 Diagram: Typical IDD_RUN operating behavior

The following data was measured from previous devices with same MCU core (ARM® Cortex-M0+) under these conditions:

- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

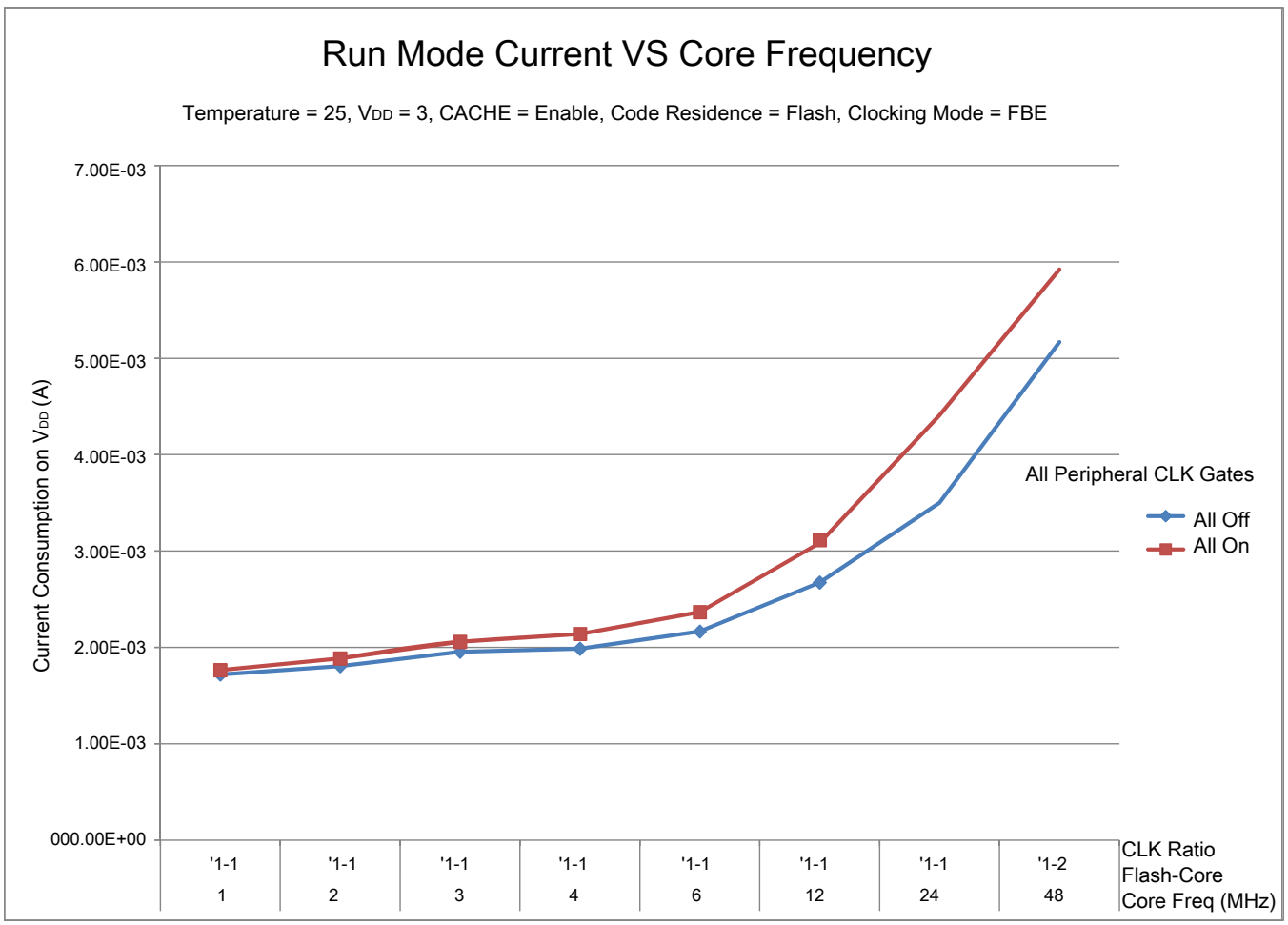


Figure 3. Run mode supply current vs. core frequency

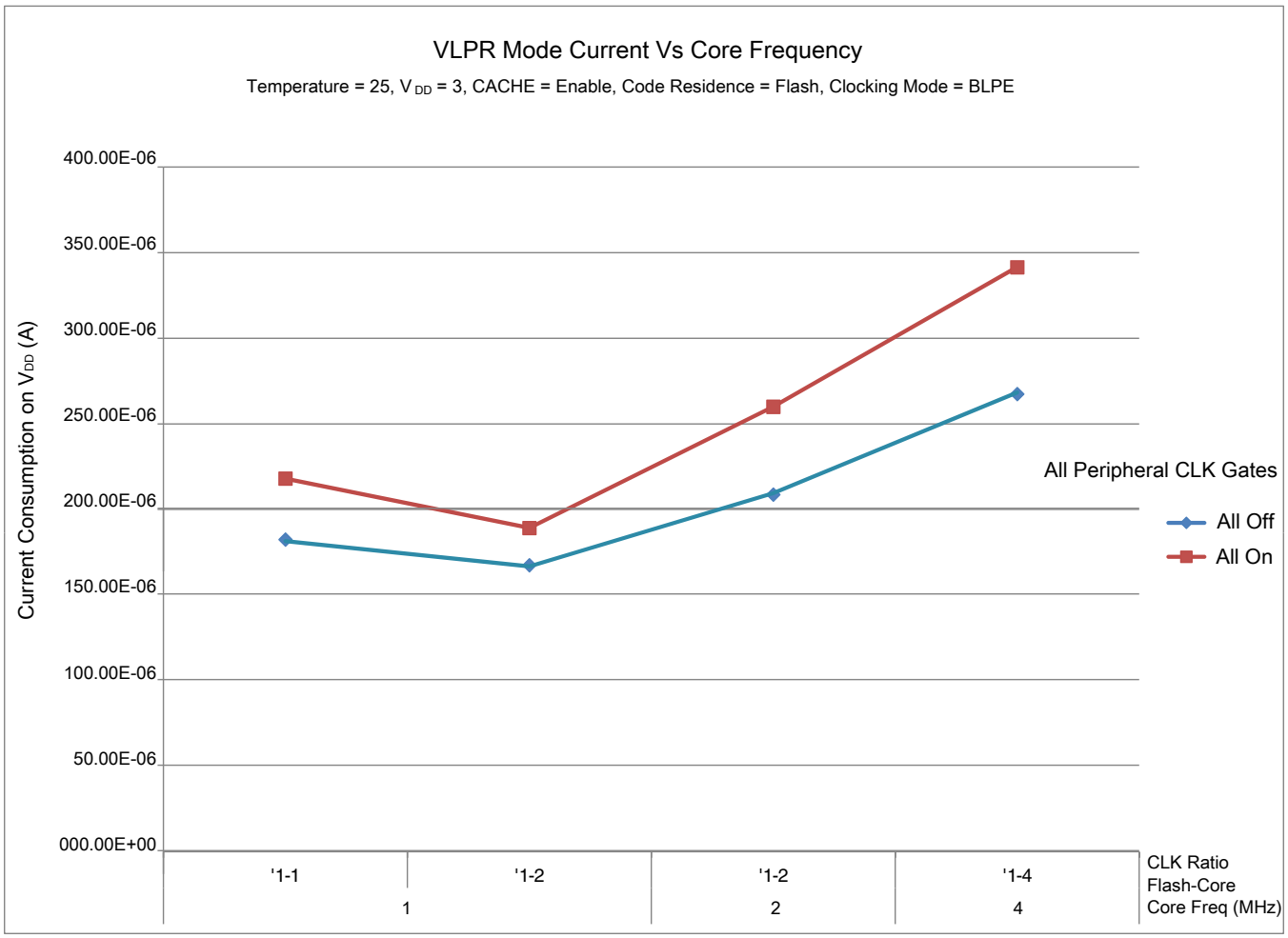


Figure 4. VLPR mode current vs. core frequency

6.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com
2. Perform a keyword search for “EMC design.”

6.2.8 Capacitance attributes

Table 14. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

6.3 Switching electrical specifications

6.3.1 Device clock specifications

Table 15. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	24	MHz
f_{FLASH}	Flash clock	—	24	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes[1]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock[2]	—	24	MHz
f_{ERCLK}	External reference clock	—	16	MHz
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz
f_{TPM}	TPM asynchronous clock	—	8	MHz
f_{UART0}	UART0 asynchronous clock	—	8	MHz

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

6.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, UART, CMT and I^2C signals.

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	-	Bus clock cycles	1, 2
NMI_b pin interrupt pulse width (analog filter enabled) — Asynchronous path	200	-	ns	3
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	20	-	ns	3
External RESET_b input pulse width (digital glitch filter disabled)	100	-	ns	

Table continues on the next page...

Description	Min.	Max.	Unit	Notes
Port rise and fall time(low drive strength) • Slew enabled • 1.71 ≤ VDD ≤ 2.7 V • 2.7 ≤ VDD ≤ 3.6 V • Slew disabled • 1.71 ≤ VDD ≤ 2.7 V • 2.7 ≤ VDD ≤ 3.6 V	 - - - -	 25 16 8 6	 ns ns ns ns	4, 5
Port rise and fall time(low drive strength) • Slew enabled • 1.71 ≤ VDD ≤ 2.7 V • 2.7 ≤ VDD ≤ 3.6 V • Slew disabled • 1.71 ≤ VDD ≤ 2.7 V • 2.7 ≤ VDD ≤ 3.6 V	 - - - -	 24 16 10 6	 ns ns ns ns	6, 7

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry in run modes.
2. The greater of synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized
4. PTB0, PTB1, PTC0, PTC1, PTC2, PTC3.
5. 75 pF load.
6. Ports A, B, and C.
7. 25 pF load.

6.4 Thermal specifications

6.4.1 Thermal operating requirements

Table 16. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	100	°C	
T_A	Ambient temperature	–40	85	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

6.4.2 Thermal attributes

Table 17. Thermal attributes

Board type	Symbol	Description	48-pin Laminate QFN	32-pin Laminate QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	83.5	96.9	°C/W	1, 2

Table continues on the next page...

Table 17. Thermal attributes (continued)

Board type	Symbol	Description	48-pin Laminate QFN	32-pin Laminate QFN	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	51.3	53.3	°C/W	1, 2, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	66.3	76.2	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	46.4	47.8	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	31.4	27.4	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	19.1	19.5	°C/W	5
Natural Convention	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.5	0.6	°C/W	6
Natural Convention	$R_{\theta JC\_CSB}$	Junction to Package Bottom	28.6	17.8	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal resistance between the die and the central solder balls on the bottom of the package based on simulation.

6.5 Peripheral operating requirements and behaviors

6.5.1 Core modules

6.5.1.1 SWD electricals

Table 18. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation			

Table continues on the next page...

Table 18. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
	• Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

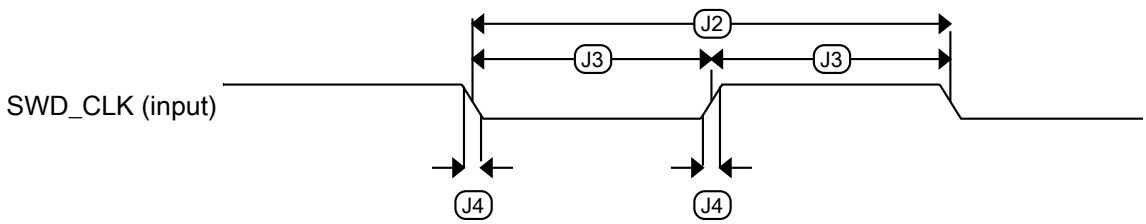


Figure 5. Serial wire clock input timing

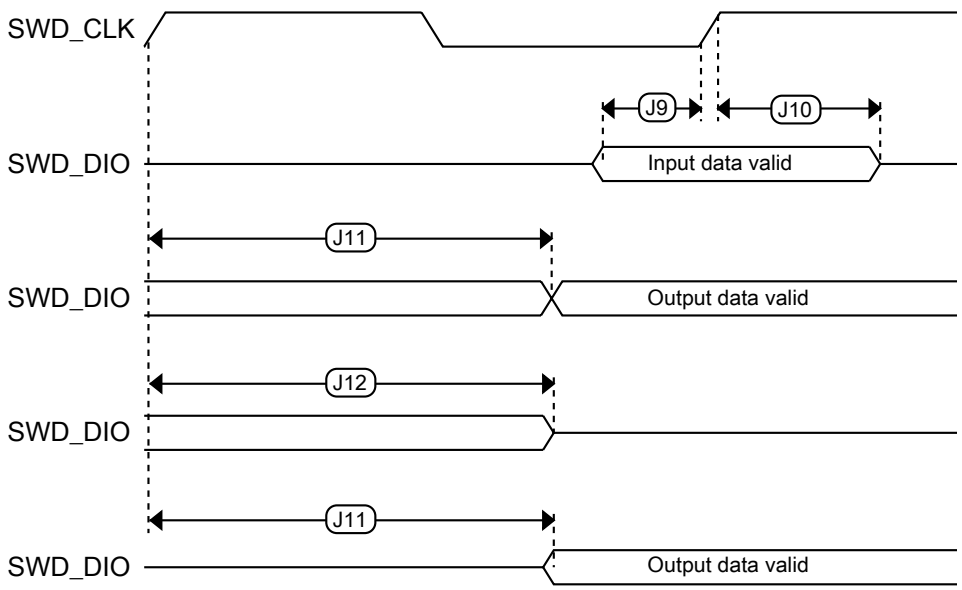


Figure 6. Serial wire data timing

6.5.2 System modules

There are no specifications necessary for the device's system modules.

6.5.3 Clock modules

6.5.3.1 MCG specifications

Table 19. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTRIM] and C4[SCFTRIM]		—	± 0.3	± 0.6	$\%f_{dco}$	
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	± 3	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70 °C		—	± 0.4	± 1.5	$\%f_{dco}$	1, 2
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C		—	4	—	MHz	
Δf_{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V_{DD} and 25 °C		—	+1/-2	± 3	$\%f_{intf\_ft}$	2
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS = 00) 640 × f_{fll_ref}	20	20.97	25	MHz	
		Mid range (DRS = 01) 1280 × f_{fll_ref}	40	41.94	48	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS = 00) 732 × f_{fll_ref}	—	23.99	—	MHz	
		Mid range (DRS = 01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz		—	180	—	ps	

Table continues on the next page...

Table 19. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{fll\_acquire}$	FLL target frequency acquisition time	—	—	1	ms	

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, f_{ints_ft}.

6.5.3.2 Reference Oscillator Specification

The KW40Z SoC has been designed to meet targeted specifications with a +/-20ppm frequency error over the life of the part, which includes the temperature, mechanical and aging excursions.

The table below shows typical specifications for the Crystal Oscillator to be used with KW40Z. NDK EXS00A-CS07637 32 MHz crystal is recommended.

Table 20. Reference Crystal Specification

Symbol	Description	Comment	min.	typ.	max.	Unit
V_{VDD_XTAL}	Nominal Operating Voltage		1.8		3.6	V
	Operating Temperature		-40		85	deg C
ESR	Equiv Series Resistance			60		ohms
Cload	Max Load Capacitance				10	pF
Faging	Frequency accuracy over aging	1st year	-5		5	ppm - 1st yr
iFacc	Initial Frequency accuracy	with respect to XO	-10		10	ppm
Fstab	Frequency stability	across temperature, mechanical , load and voltage changes	-10		10	ppm

6.5.4 Memories and memory interfaces

6.5.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.5.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 21. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	
$t_{hversblk32k}$	Erase Block high-voltage time for 32 KB	—	52	452	ms	1
$t_{hversblk128k}$	Erase Block high-voltage time for 128 KB	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.5.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					1
$t_{rd1blk32k}$	• 32 KB program flash	—	—	0.5	ms	
$t_{rd1blk128k}$	• 128 KB program flash	—	—	1.7	ms	
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
	Erase Flash Block execution time					2
$t_{ersblk32k}$	• 32 KB program flash	—	60	500	ms	
$t_{ersblk128k}$	• 128 KB program flash	—	88	600	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	1
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	150	1200	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

6.5.4.1.3 Flash high voltage current behaviors

Table 23. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.5.4.1.4 Reliability specifications

Table 24. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.

6.5.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.5.6 Analog

6.5.6.1 ADC electrical specifications

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications. The following specification is defined with the DCDC converter operating in Bypass mode.

6.5.6.1.1 16-bit ADC operating conditions

Table 25. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2

Table continues on the next page...

Table 25. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	3
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 × VREFH VREFH	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	4
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	5
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	ksps	
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	ksps	6

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated VREFH and VREFL pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SSA}.
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
5. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
6. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

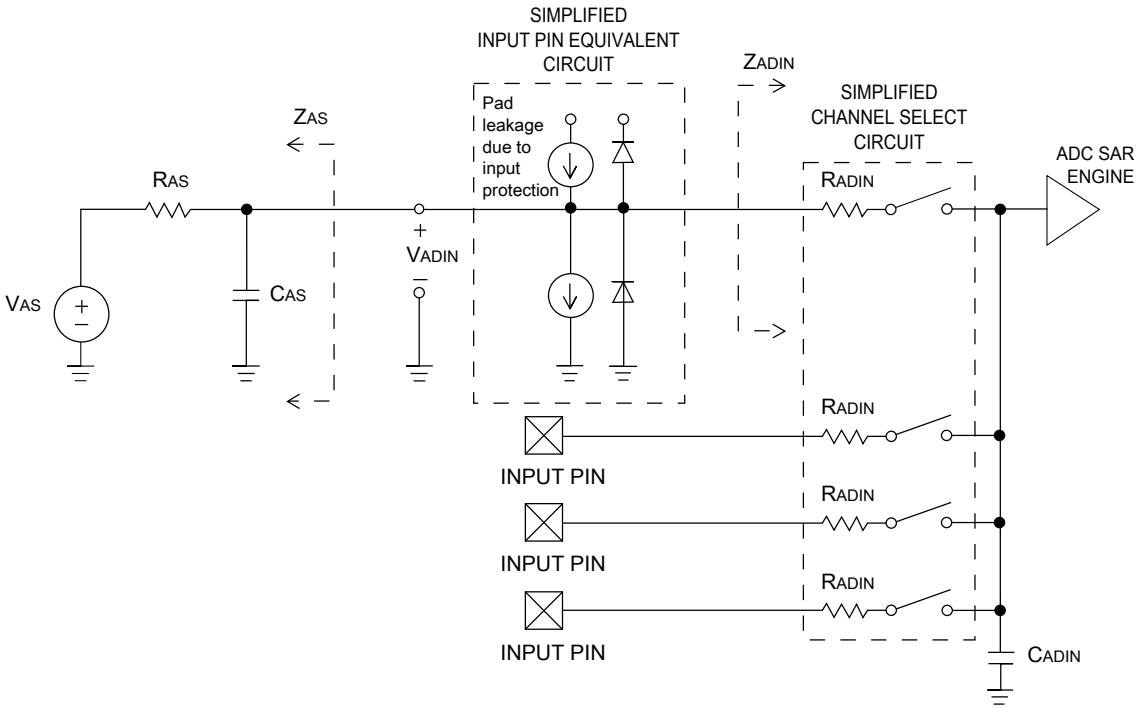


Figure 7. ADC input impedance equivalency diagram

6.5.6.1.2 16-bit ADC electrical characteristics

Table 26. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	2
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t_{ADACK} = 1/ f_{ADACK}
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes	—	±4	±6.8	LSB	
		• <12-bit modes	—	±1.4	±2.1		
DNL	Differential non-linearity	• 12-bit modes	—	±0.7	–1.1 to +1.9	LSB[3]	4
		• <12-bit modes	—	±0.2	–0.3 to 0.5		
INL	Integral non-linearity	• 12-bit modes	—	±1.0	–2.7 to +1.9	LSB[3]	4
		• <12-bit modes	—	±0.5	–0.7 to +0.5		

Table continues on the next page...

Table 26. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.	Max.	Unit	Notes
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[3]	V_{ADIN} = V_{DDA}[4]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[3]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 11.54 10.33 10.3 9.22	 13.5 12.5 13 12	 — — — —	 bits bits bits bits	
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 -88 -80	 — —	dB dB	
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 79 72	 88 85	 — —	dB dB	5
E_{IL}	Input leakage error		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.67	1.74	1.81	mV/°C	
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	6

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
3. 1 LSB = (V_{REFH} - V_{REFL})/2^N
4. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
5. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
6. ADC conversion clock < 3 MHz

6.5.6.2 CMP and 6-bit DAC electrical specifications

Table 27. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

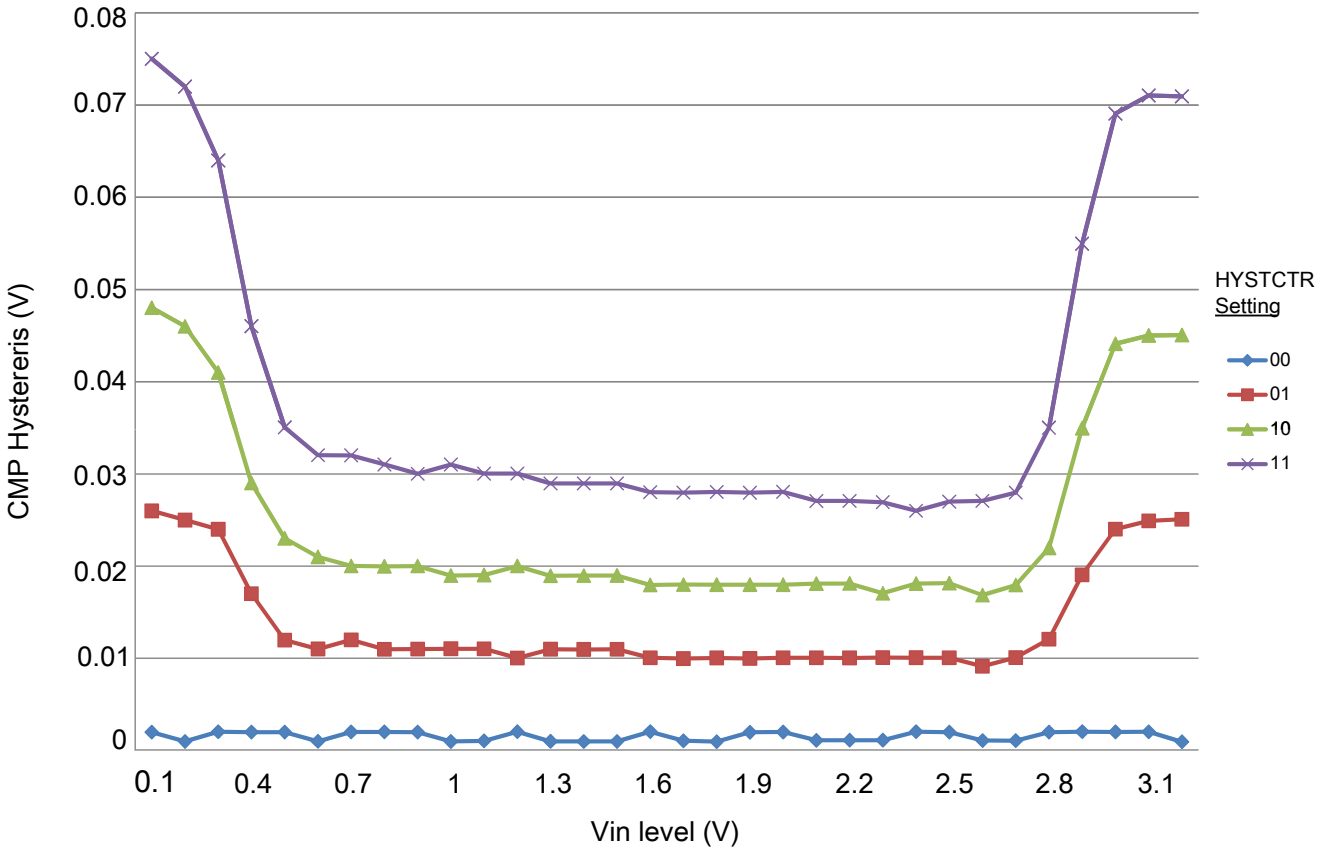


Figure 8. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

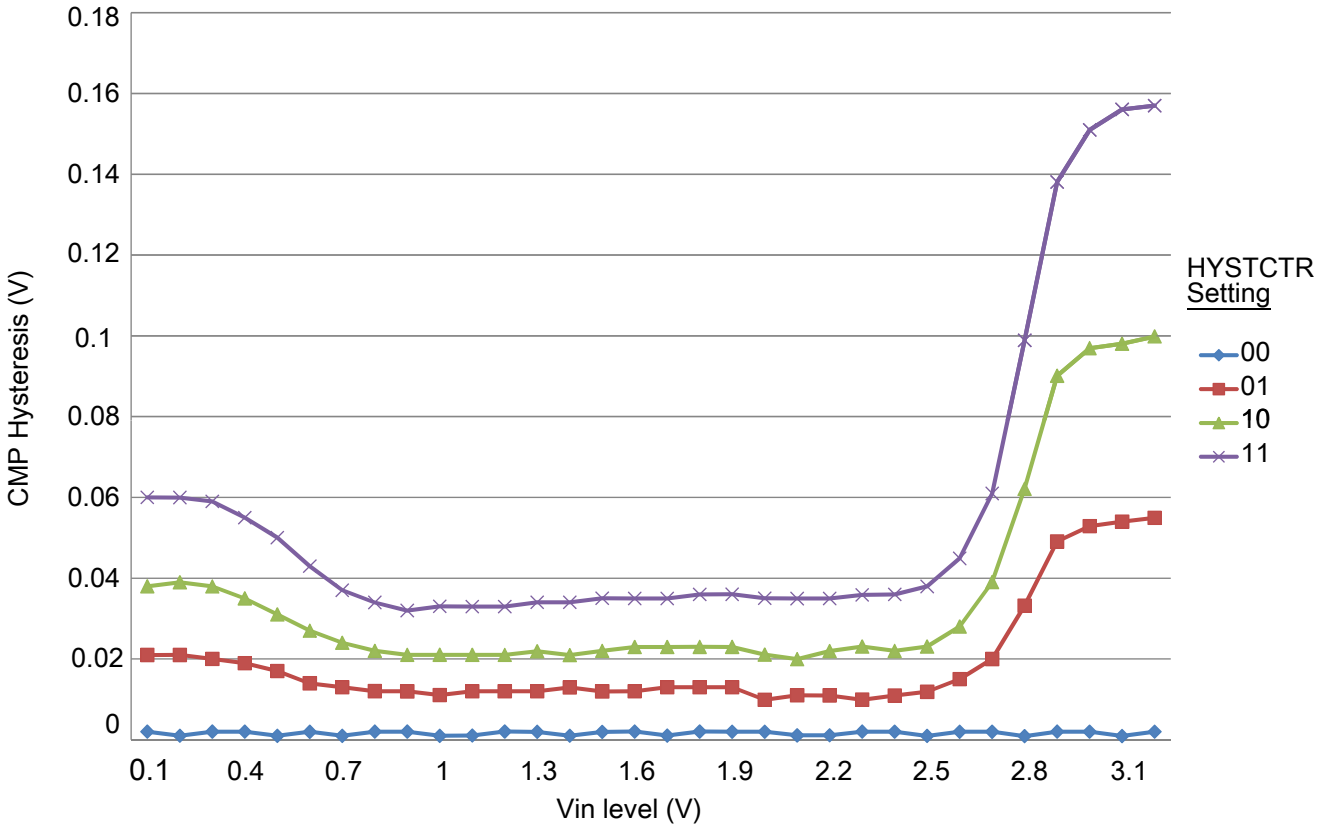


Figure 9. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

6.5.6.3 12-bit DAC electrical characteristics

6.5.6.3.1 12-bit DAC operating requirements

Table 28. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

6.5.6.3.2 12-bit DAC operating behaviors

Table 29. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	250	μA	

Table continues on the next page...

Table 29. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	900	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	μV/C	
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/μs	
	• High power (SP_{HP})	1.2	1.7	—		
	• Low power (SP_{LP})	0.05	0.12	—		
BW	3dB bandwidth				kHz	
	• High power (SP_{HP})	550	—	—		
	• Low power (SP_{LP})	40	—	—		

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV

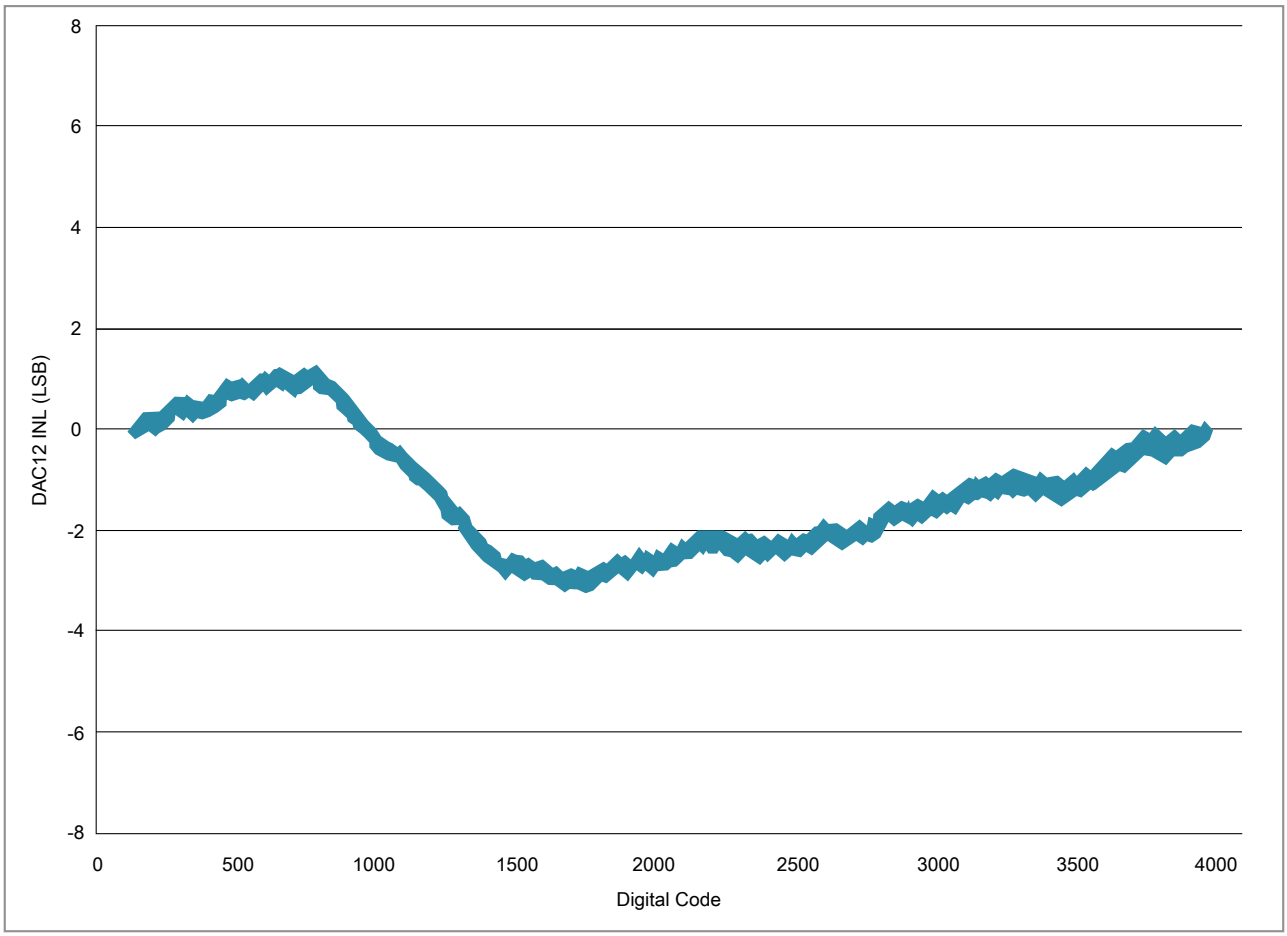


Figure 10. Typical INL error vs. digital code

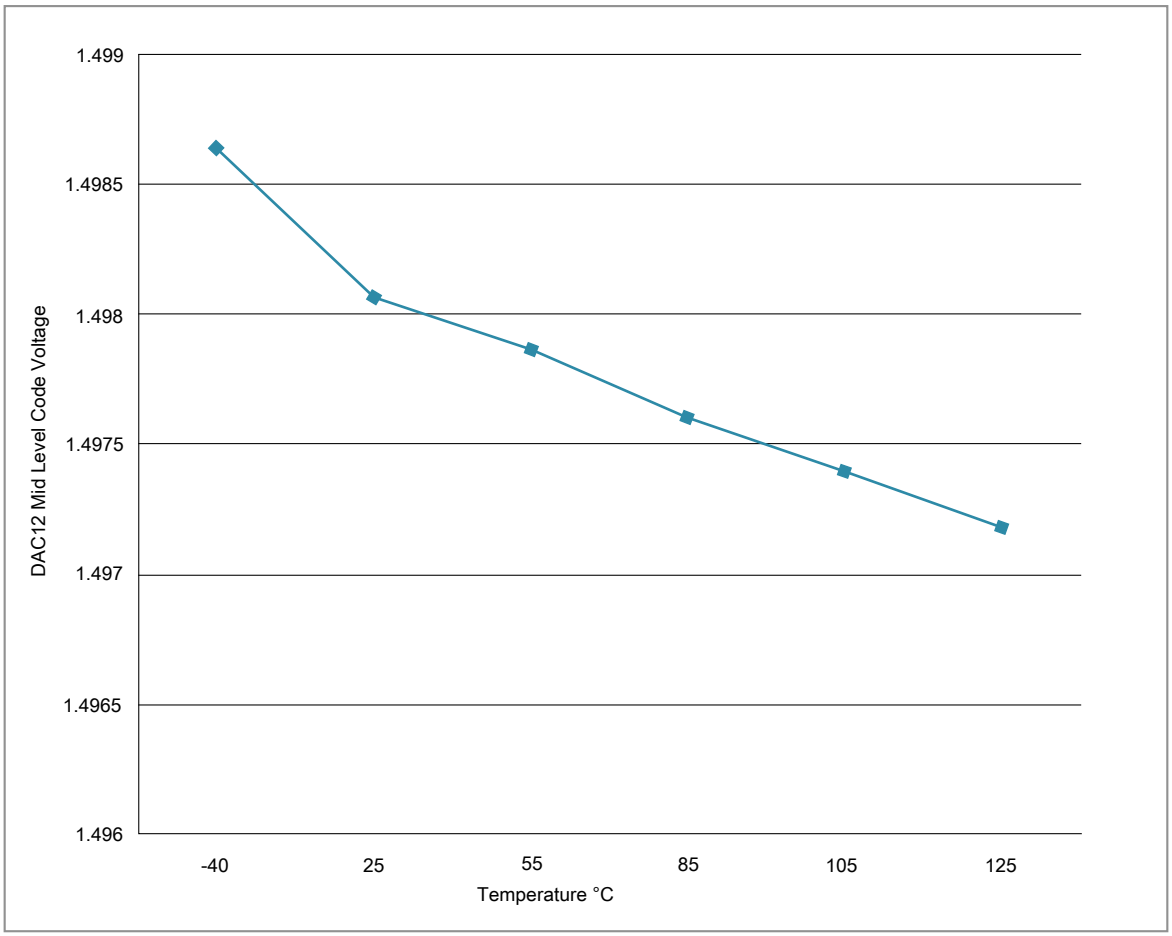


Figure 11. Offset at half scale vs. temperature

6.5.7 Timers

See General switching specifications.

6.5.8 Communication interfaces

6.5.8.1 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 30. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	12	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

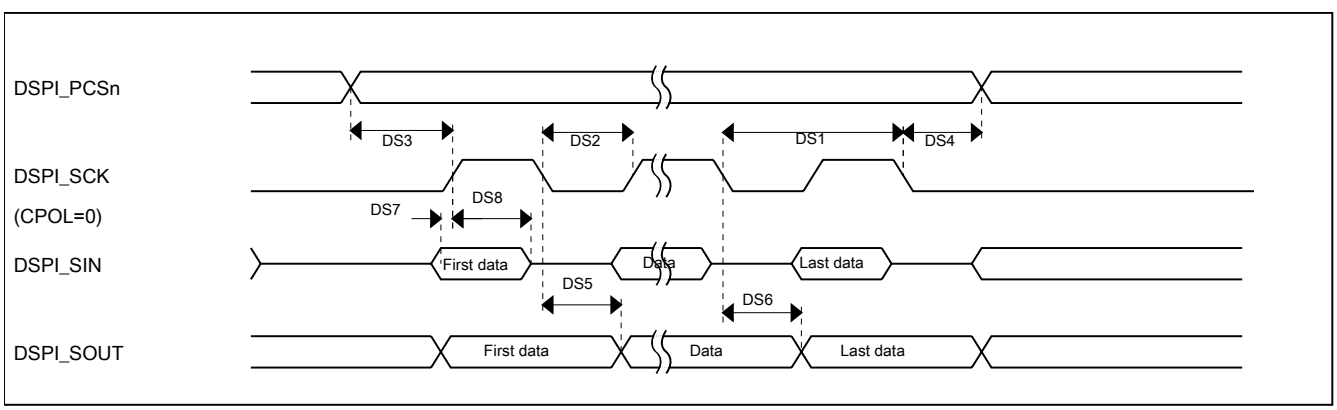


Figure 12. DSPI classic SPI timing — master mode

Table 31. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		6	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns

Table continues on the next page...

Table 31. Slave mode DSPI timing (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	21.4	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

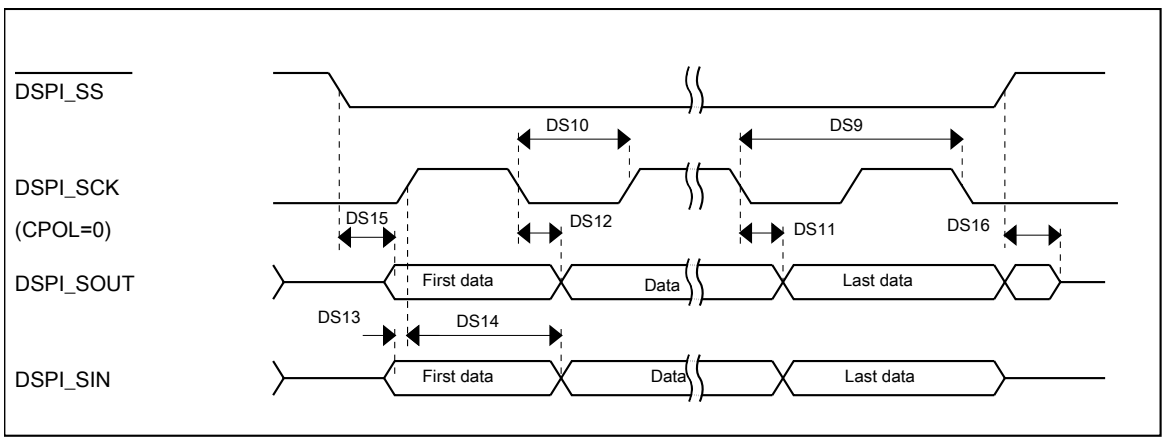


Figure 13. DSPI classic SPI timing — slave mode

6.5.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 32. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3

Table continues on the next page...

Table 32. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24.6	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

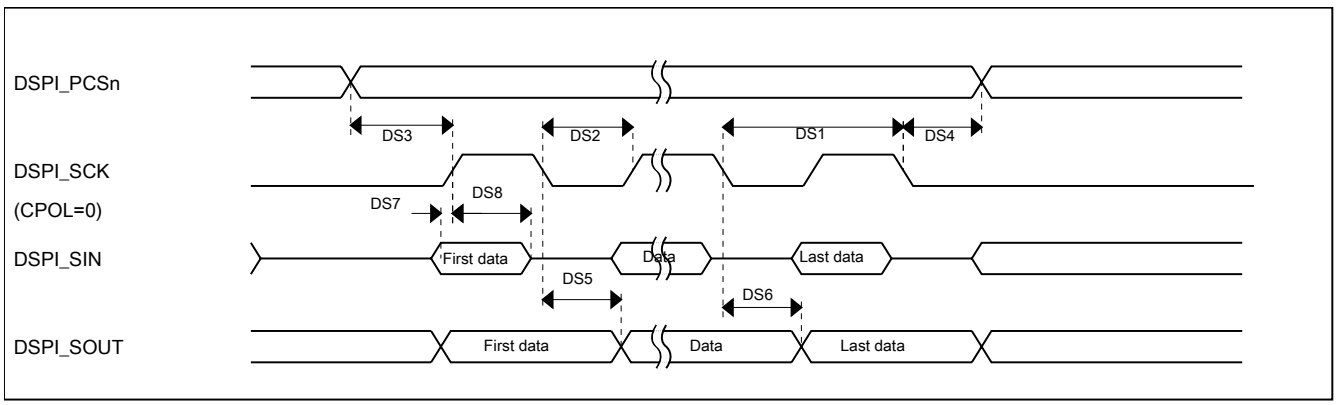


Figure 14. DSPI classic SPI timing — master mode

Table 33. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	29.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	25	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	25	ns

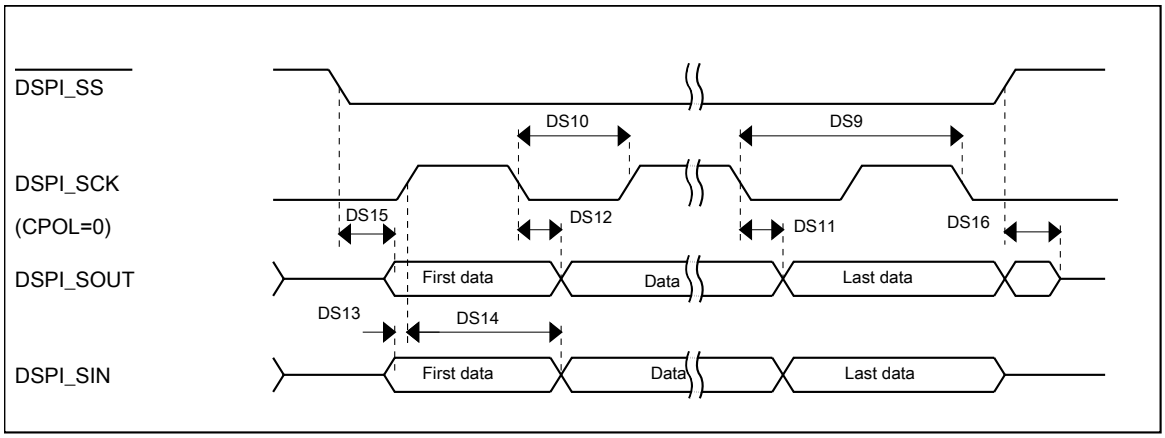


Figure 15. DSPI classic SPI timing — slave mode

6.5.8.3 Inter-Integrated Circuit Interface (I^2C) timing

Table 34. I^2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0	3.45	0	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250	—	100[2]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[4]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[3]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\,DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\,DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
4. C_b = total capacitance of the one bus line in pF.

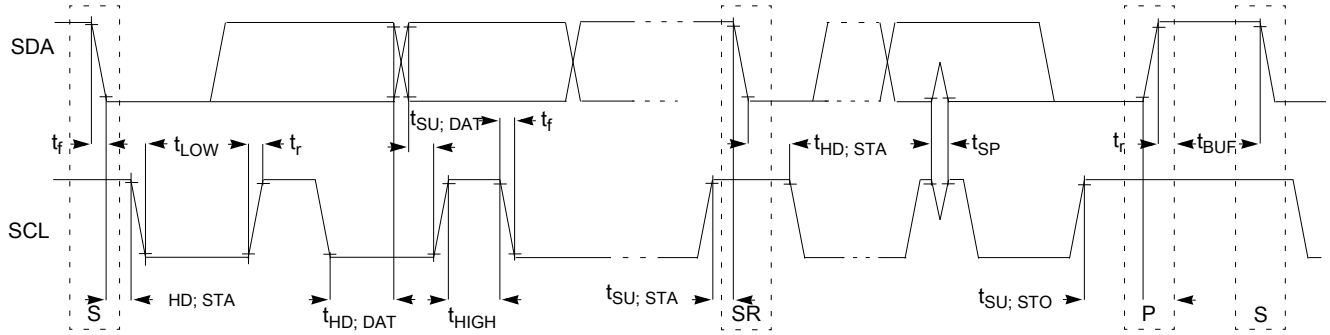


Figure 16. Timing definition for fast and standard mode devices on the I^2C bus

6.5.8.4 UART

See General switching specifications.

6.5.9 Human-machine interfaces (HMI)

6.5.9.1 TSI electrical specifications

Table 35. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	µA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	µA
TSI_EN	Power consumption in enable mode	—	100	—	µA
TSI_DIS	Power consumption in disable mode	—	1.2	—	µA
TSI_TEN	TSI analog enable time	—	66	—	µs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	0.19	—	1.03	V

6.5.9.2 GPIO

The maximum input voltage on PTC0/1/2/3 is VDD+0.3V. For rest of the GPIO specification, see General switching specifications.

7 KW40Z Electrical Characteristics

7.1 DCDC Converter Recommended Electrical Characteristics

Table 36. DCDC Converter Recommended operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Bypass Mode Supply Voltage (RF and Analog)	VDD_{RF1}, VDD_{RF2}, VDD_{XTAL}	1.45	—	3.6	Vdc
Bypass Mode Supply Voltage (Digital)	VDD_X, V_{DCDC_IN}, VDD_A	1.71	—	3.6	Vdc
Boost Mode Supply Voltage	VDD_{DCDC_IN}	0.9	—	1.795	Vdc
Buck Mode Supply Voltage[2, 1]	VDD_{DCDC_IN}	2.1	—	3.6	Vdc

1. In Buck and Boost modes, DCDC converter will generate 1.8V at VDD_1P8OUT and 1.45V at VDD_1P45OUT_PMCIN pins. VDD_1P8OUT should supply to VDD_1, VDD_2 and VDD_A. VDD_1P45OUT_PMCIN should supply to VDD_RF_1 and VDD_RF_2. VDD_{XTAL} can be either supplied by 1.45V or 1.8V
2. In Buck mode, DCDC converter needs 2.1V min to start, the supply can drop to 1.8V after DCDC converter settles

Table 37. DCDC Converter Specifications

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
DCDC Converter Output Power	Total power output of 1p8V and 1p45V	Pdcdc_out	-	-	125[1]	mW
Boost Mode						
DCDC Converter Input Voltage	Operating Voltage Range	VDCDC_IN_boost	0.9	-	1.795	Vdc
	DCDC Startup Voltage Range[2]	VDCDC_IN_boost_startup	1.1	-	-	Vdc
1.8V Output Voltage		VDD_1P8_boost	-	1.8[3]	3	Vdc
1.8V Output Current[5]	VDD_1P8 = 1.8V, VDCDC_IN = 1.7V	IDD_1P8_boost1	-	-	45	mA
	VDD_1P8 = 3.0V, VDCDC_IN = 1.7V	IDD_1P8_boost2	-	-	27	mA
	VDD_1P8 = 1.8V, VDCDC_IN = 0.9V	IDD_1P8_boost3	-	-	20	mA
	VDD_1P8 = 3.0V, VDCDC_IN = 0.9V	IDD_1P8_boost4	-	-	10	mA
1.45V Output Voltage		VDD_1P45_boost	-	1.8[6, 7]	2.0	Vdc
1.45V Output Current[4, 8]		VDD_1P45_boost	-	-	30	mA
Buck Mode						
DCDC Converter Input Voltage	Operating Voltage Range	VDCDC_IN_buck	1.8	-	3.6	Vdc
	DCDC Startup Voltage Range[9]	VDCDC_IN_buck_startup	2.2	-	-	Vdc

Table continues on the next page...

Table 37. DCDC Converter Specifications (continued)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
1.8V Output Voltage		VDD_1P8_buck	1.71	-	min(VDCDC_IN_buck, 3)[10, 3]	Vdc
1.8V Output Current[4, 5]	VDD_1P8 = 1.8V, VDC_1P45 = 1.45V	IDD_1P8_buck1	-	-	45	mA
	VDD_1P8 = 3.0V, VDC_1P45 = 1.45V	IDD_1P8_buck2	-	-	27	mA
1.45V Output Voltage	Radio section requires 1.45V	VDD_1P45_buck	-	1.45[11]	2.0	Vdc
1.45V Output Current[4, 8]		IDD_1P45_buck	-	-	30	mA

1. This is the steady state DC output power. It requires VDCDC_IN >= 1.7V in boost mode. Excessive transient current load from external device will cause 1p8V and 1p45 output voltage unregulated temporary.
2. DCDC converter requires slightly higher input voltage during startup. VDCDC_IN_boost_startup is the minimum startup voltages for the DCDC converter in boost mode. Bit DCDC_STS_DC_OK will be set when the DCDC converter finish the startup sequence. Typical startup time is 50ms and it varies with the loading of the converter.
3. The voltage output level can be controlled by programming DCDC_VDD1P8CTRL_TRG field in DCDC_REG3.
4. The output current specification in both buck and boost modes represents the maximum current the DCDC converter can deliver. The KW40Z radio and MCU blocks current consumption is not excluded. Note that the maxium output power of the DCDC converter is 125mW. The available supply current for external device depends on the energy consumed by the internal peripherals in KW40Z. See application note AN5025 for detail explanation.
5. When using DCDC in low power mode(pulsed mode), current load must be less than 1mA.
6. In Boost mode, the minimum 1.45V output is the maximum of either what is programmed using DCDC_VDD1P45CTRL_TRG_BOOST field in DCDC_REG3 or VDCDC_IN_boost + 0.05V. For example, if VDCDC_IN = 0.9V, minimum VDD_1P45 is as programmed in DCDC_VDD1P45CTRL_ TRG_BOOST. If VDCDC_IN = 1.5V, minimum VDD_1P45 = 1.5 + 0.05V is 1.55V.
7. 1.8V is default value of the DCDC 1.45V output voltage in boost mode. The user can program DCDC_VDD1P45CTRL_TRG_BOOST field in register DCDC_REG3 to control 1.45V output voltage level. For reliable radio operation, a voltage level of 1.425V is required.
8. 1.45V is intended to supply power to KW40Z only. It is not designed to supply power to an external device.
9. DCDC converter requires slightly higher input voltage during startup. VDCDC_IN_buck_startup is the minimum startup voltages for the DCDC converter in buck mode. Bit DCDC_STS_DC_OK will be set when the DCDC converter finish the startup sequence. Typical startup time is 50ms and it varies with the loading of the converter.
10. In Buck mode, the maximum 1.8V output is the minimum of either VDCDC_IN_BUCK or 3V. For example, if VDCDC_IN = 1.8V, maximum VDD_1P8 is 1.8V. If VDCDC_IN = 3.6V, maximum VDD_1P8 is 3V.
11. User needs to program DCDC_VDD1P45CTRL_TRG_BUCK field in DCDC_REG3 register to ensure that a worst case minimum of 1.425V is available as VDD_1P45_buck for radio operation.

7.2 Ratings

7.2.1 Thermal handling ratings

Table 38. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

7.2.2 Moisture handling ratings

Table 39. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

7.2.3 ESD handling ratings

Table 40. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 85 °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

7.2.4 Voltage and current operating ratings

Table 41. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{IO_DCDC}	IO pins in the DCDC voltage domain (DCDC_CFG and PSWITCH)	GND	VDCDC	V

8 Pin Diagrams and Pin Assignments

8.1 Pinouts

Device pinout are shown in figures below.

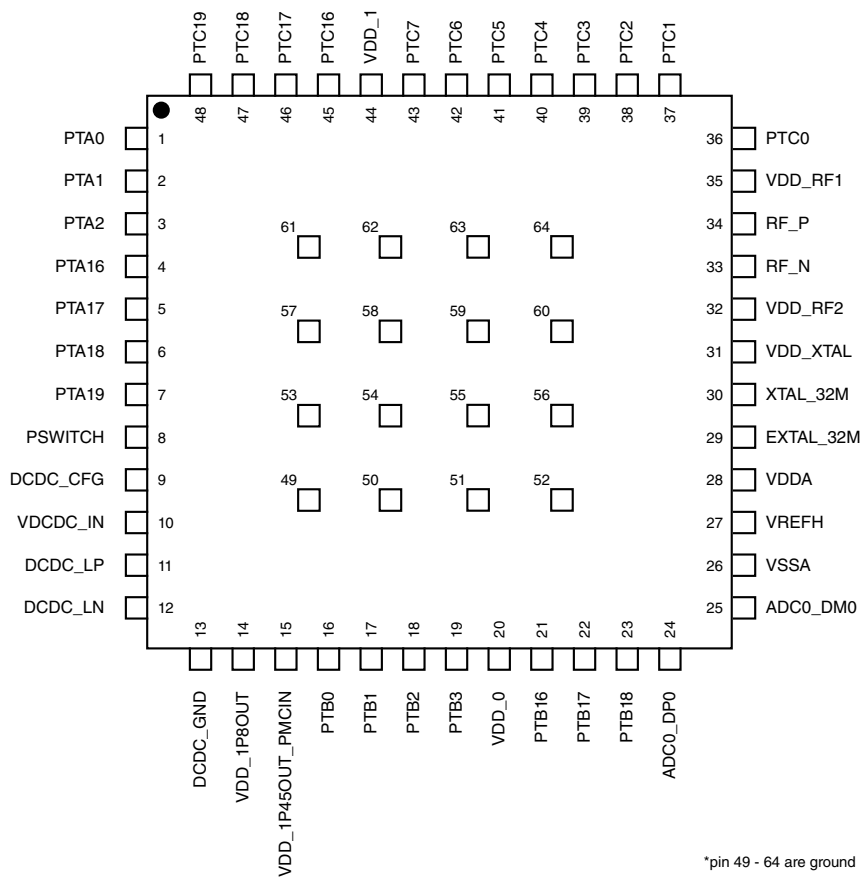


Figure 17. 48-pin Laminate QFN pinout diagram

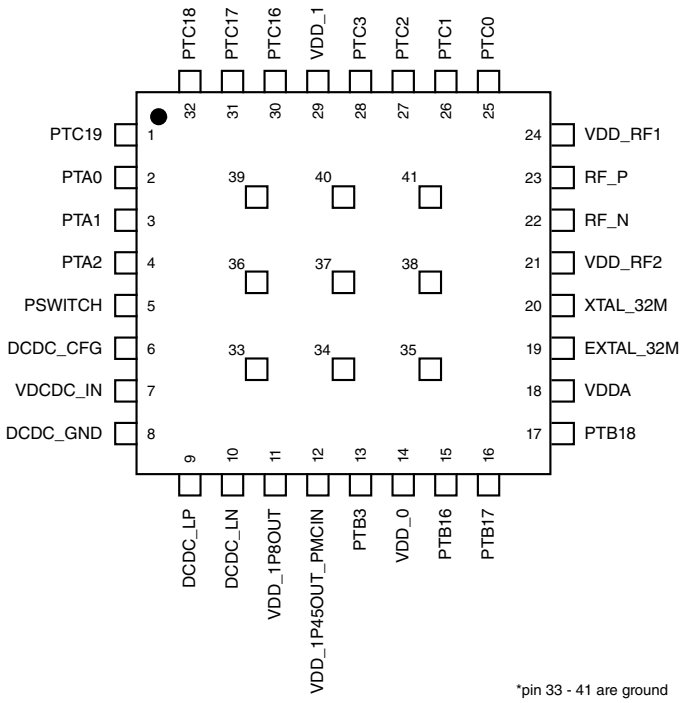


Figure 18. 32-pin Laminate QFN pinout diagram

8.2 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and locations of these pins on the packages supported by this device. The Port Control Module is responsible for selecting which ALT functional is available on each PTxy pin.

Table 42. KW40Z Pin Assignments

48 Laminate QFN	32 Laminate QFN	Pin Name[1]	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	2	PTA0	SWD_DIO	TSI0_CH8	PTA0	SPI0_PCS1	—	—	TPM1_CH0	—	SWD_DIO
2	3	PTA1	SWD_CLK	TSI0_CH9	PTA1	—	—	—	TPM1_CH1	—	SWD_CLK
3	4	PTA2	RESET_b	—	PTA2	—	—	—	TMP0_CH3	—	RESET_b
4	—	PTA16	DISABLED	TSI0_CH10	PTA16/LLWU_P4	SPI1_SOUT	—	—	TPM0_CH0	—	—
5	—	PTA17	DISABLED	TSI0_CH11	PTA17/LLWU_P5	SPI1_SIN	—	—	TPM_CLKIN1	—	—

Table continues on the next page...

Table 42. KW40Z Pin Assignments (continued)

48 Laminate QFN	32 Laminate QFN	Pin Name[1]	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
6	—	PTA18	DISABLED	TSI0_CH12	PTA18/ LLWU_ P6	SPI1_S CK	—	—	TPM2_ CH0	—	—
7	—	PTA19	DISABLED	TSI0_CH13	PTA19/ LLWU_ P7	SPI1_P CS0	—	—	TPM2_ CH1	—	—
8	5	PSWITCH	PSWITCH	PSWITCH	—	—	—	—	—	—	—
9	6	DCDC_CF G	DCDC_CF G	DCDC_CFG	—	—	—	—	—	—	—
10	7	VDCDC_IN	VDCDC_IN	VDCDC_IN	—	—	—	—	—	—	—
11	9	DCDC_LP	DCDC_LP	DCDC_LP	—	—	—	—	—	—	—
13	8	DCDC_GN D	DCDC_GN D	DCDC_GND	—	—	—	—	—	—	—
14	11	VDD_1P8O UT	VDD_1P8O UT	VDD_1P8OUT	—	—	—	—	—	—	—
12	10	DCDC_LN	DCDC_LN	DCDC_LN	—	—	—	—	—	—	—
15	12	VDD_1P45 OUT_PMCI N	VDD_1P45 OUT_PMCI N	VDD_1P45OUT_P MCIN	—	—	—	—	—	—	—
16	—	PTB0	DISABLED	—	PTB0/ LLWU_ P8	—	I2C0_S CL	CMP0_ OUT	TPM0_ CH1	—	CLKOU T
17	—	PTB1	ADC0_SE1 /CMP0_IN5	ADC0_SE1/ CMP0_IN5	PTB1	—	I2C0_S DA	LPTMR 0_ALT 1	TPM0_ CH2	—	CMT_I RO
18	—	PTB2	ADC0_SE3 /CMP0_IN3	ADC0_SE3/ CMP0_IN3	PTB2	—	—	—	TPM1_ CH0	—	—
19	13	PTB3	ADC0_SE2 /CMP0_IN4	ADC0_SE2/ CMP0_IN4	PTB3	—	—	CLKOU T	TPM1_ CH1	—	RTC_C LKOUT
20	14	VDD_0	—	—	—	—	—	—	—	—	—
21	15	PTB16	EXTAL32K	EXTAL32K	PTB16	—	I2C1_S CL	—	TPM2_ CH0	—	—
22	16	PTB17	XTAL32K	XTAL32K	PTB17	—	I2C1_S DA	—	TPM2_ CH1	—	—
23	17	PTB18	NMI_b	DAC0_OUT/ ADC0_SE4/ CMP0_IN2	PTB18	—	I2C1_S CL	TPM_C LKIN0	TPM0_ CH0	—	NMI_b
24	—	ADC0_DP0	ADC0_DP0 /CMP0_IN0	ADC0_DP0/ CMP0_IN0	—	—	—	—	—	—	—
25	—	ADC0_DM 0	—	ADC0_DM0/ CMP0_IN1	—	—	—	—	—	—	—
26	—	VSSA	VSSA	VSSA	—	—	—	—	—	—	—
27	—	VREFH	VREFH	VREFH	—	—	—	—	—	—	—

Table continues on the next page...

Table 42. KW40Z Pin Assignments (continued)

48 Laminate QFN	32 Laminate QFN	Pin Name[1]	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
28	18	VDDA	VDDA	VDDA	—	—	—	—	—	—	—
29	19	EXTAL_32M	EXTAL_32M	EXTAL_32M	—	—	—	—	—	—	—
30	20	XTAL_32M	XTAL_32M	XTAL_32M	—	—	—	—	—	—	—
31	—	VDD_XTAL	VDD_XTAL	VDD_XTAL	—	—	—	—	—	—	—
32	21	VDD_RF2	VDD_RF2	VDD_RF2	—	—	—	—	—	—	—
33	22	RF_N	RF_N	RF_N	—	—	—	—	—	—	—
34	23	RF_P	RF_P	RF_P	—	—	—	—	—	—	—
35	24	VDD_RF1	VDD_RF1	VDD_RF1	—	—	—	—	—	—	—
36	25	PTC0	DISABLED	—	PTC0/LLWU_P9	ANT_A	I2C0_SCL	UART0_CTS_b	TPM0_CH1	—	—
37	26	PTC1	DISABLED	—	PTC1	ANT_B	I2C0_SDA	UART0_RTS_b	TPM0_CH2	—	BLE_ACTIVE
38	27	PTC2	DISABLED	TSI0_CH14	PTC2/LLWU_P10	TX_SWITCH	I2C1_SCL	UART0_RX	CMT_IRO	—	DTM_RX
39	28	PTC3	DISABLED	TSI0_CH15	PTC3/LLWU_P11	RX_SWITCH	I2C1_SDA	UART0_TX	—	—	DTM_TX
40	—	PTC4	DISABLED	TSI0_CH0	PTC4/LLWU_P12	—	EXTRG_IN	UART0_CTS_b	TPM1_CH0	—	—
41	—	PTC5	DISABLED	TSI0_CH1	PTC5/LLWU_P13	—	LPTMR0_ALT2	UART0_RTS_b	TPM1_CH1	—	—
42	—	PTC6	DISABLED	TSI0_CH2	PTC6/LLWU_P14	—	I2C1_SCL	UART0_RX	TPM2_CH0	—	—
43	—	PTC7	DISABLED	TSI0_CH3	PTC7/LLWU_P15	SPI0_PCS2	I2C1_SDA	UART0_TX	TPM2_CH1	—	—
44	29	VDD_1	VDD	—	—	—	—	—	—	—	—
45	30	PTC16	DISABLED	TSI0_CH4	PTC16/LLWU_P0	SPI0_SCK	I2C0_SDA	UART0_RTS_b	TPM0_CH3	—	—
46	31	PTC17	DISABLED	TSI0_CH5	PTC17/LLWU_P1	SPI0_SOUT	—	UART0_RX	—	—	DTM_RX
47	32	PTC18	DISABLED	TSI0_CH6	PTC18/LLWU_P2	SPI0_SIN	—	UART0_TX	—	—	DTM_TX

Table continues on the next page...

Table 42. KW40Z Pin Assignments (continued)

48 Laminate QFN	32 Laminate QFN	Pin Name[1]	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
48	1	PTC19	DISABLED	TSI0_CH7	PTC19/ LLWU_ P3	SPI0_P CS0	I2C0_S CL	UART0 _CTS_ b	—	—	BLE_A CTIVE
49-64	33-41	Ground	NA	NA	NA	NA	NA	NA	NA	NA	NA

1. LLWU_Px signals are active in LLS/VLLSx power modes

9 Package Information

9.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **nxp.com** and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin Laminate QFN (5x5)	98ASA00693D
48-pin Laminate QFN (7x7)	98ASA00694D

10 Revision History

The following table provides a revision history for this document.

Table 43. Revision History

Rev. No.	Date	Substantial Changes
1.2	April 2018	• Updated DCDC Buck mode maximum voltage range to 3.6 V (from 4.2 V) throughout. • Updated Typ., Min., and Max. values of Temp sensor slope in Table 26. • Added V_{IO_DCDC} specifications in Table 41.

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Document Number MKW40Z160
Revision 1.2, 05/2018

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

MKW40Z160VHT4 MKW30Z160VHM4 MKW20Z160VHT4 MKW40Z160VHT4R MKW30Z160VHM4R