# SQ28906

## High Efficiency, 2MHz，6V/6A Synchronous Step Down Regulator

## General Description

The SQ28906 develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 6A current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. It provides accurate regulation for a variety of loads with an accurate ±1% voltage reference ($V_{REF}$) over $T_J$= -40°C to 125°C.

The SQ28906 operates over a wide input voltage range from 2.95V to 6V. Cycle-by-cycle current limit, hiccup over current protection and thermal shutdown protect the device during an over current condition.

The SQ28906 is in a space saving, low profile QFN3×3-16 package.

## Ordering Information

SQ28906 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

| Ordering Number | Package type | Note |
|---|---|---|
| SQ28906QDC | QFN3×3-16 | -- |

## Features

- Input Voltage Range: 2.95V to 6V
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 12mΩ/12mΩ
- 0.6V ±1% Voltage Reference Over Temperature Range ($T_J$: -40°C to 125°C)
- 200kHz to 2MHz Switching Frequency
- CCM Only Operation
- Start-up with Pre-biased Voltage
- Adjustable Input Voltage UVLO by EN
- External Soft-start Limits the Inrush Current
- Power Good Indicator
- Hic-cup Mode Output Short Circuit Protection
- Over Temperature Protection with Auto recovery
- RoHS Compliant and Halogen Free
- Compact Package: QFN3×3-16

## Applications

- Telecom
- Server

## Typical Applications

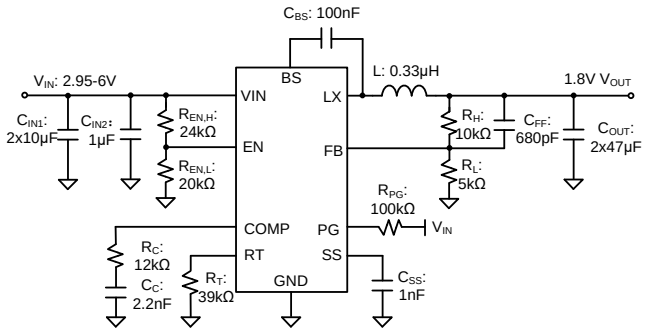



**Figure 1. Schematic Diagram**

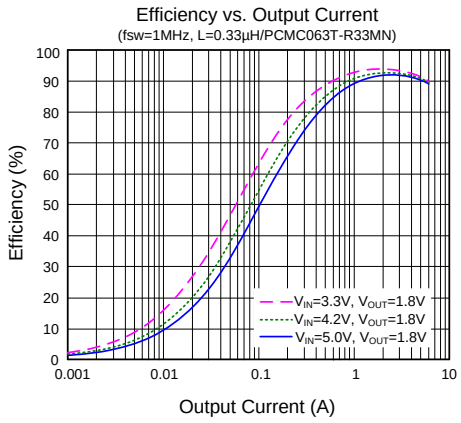
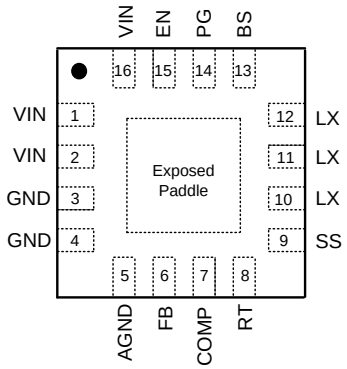



**Figure 2. Efficiency vs Load Current**

## Pin out (Top View)




Top Mark: **mE*xyz*, (**Device code: mE; ***x=year code, y=week code, z= lot number code*****)**

| Pin Name | Pin Number | Pin Description |
|---|---|---|
| VIN | 1, 2, 16 | Input pin. Decouple these pins to GND with at least 2pcs 10μF and 1pcs 1μF ceramic capacitors with low ESR. |
| GND | 3, 4 | Ground pins. |
| AGND | 5 | Analog ground should be electrically connected to GND close to the device. |
| FB | 6 | Output feedback pin. Connect to the center point of resistor divider. |
| COMP | 7 | Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin. |
| RT | 8 | Resistor timing pin. |
| SS | 9 | Soft-start pin. An external capacitor connected to this pin sets the output voltage rise time. |
| LX | 10, 11, 12 | Inductor pin. Connect this pin to the switching node of inductor. |
| BS | 13 | Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin. |
| PG | 14 | Power good Indicator. Open drain output when the output voltage is within 93% to 115% of regulation point. |
| EN | 15 | Enable pin, internal pull up current source. Pulled below 1.2 V to disable; Floating to enable. Can be used for setting the on and off threshold (adjust UVLO) with two additional resistors. |

## Block Diagram

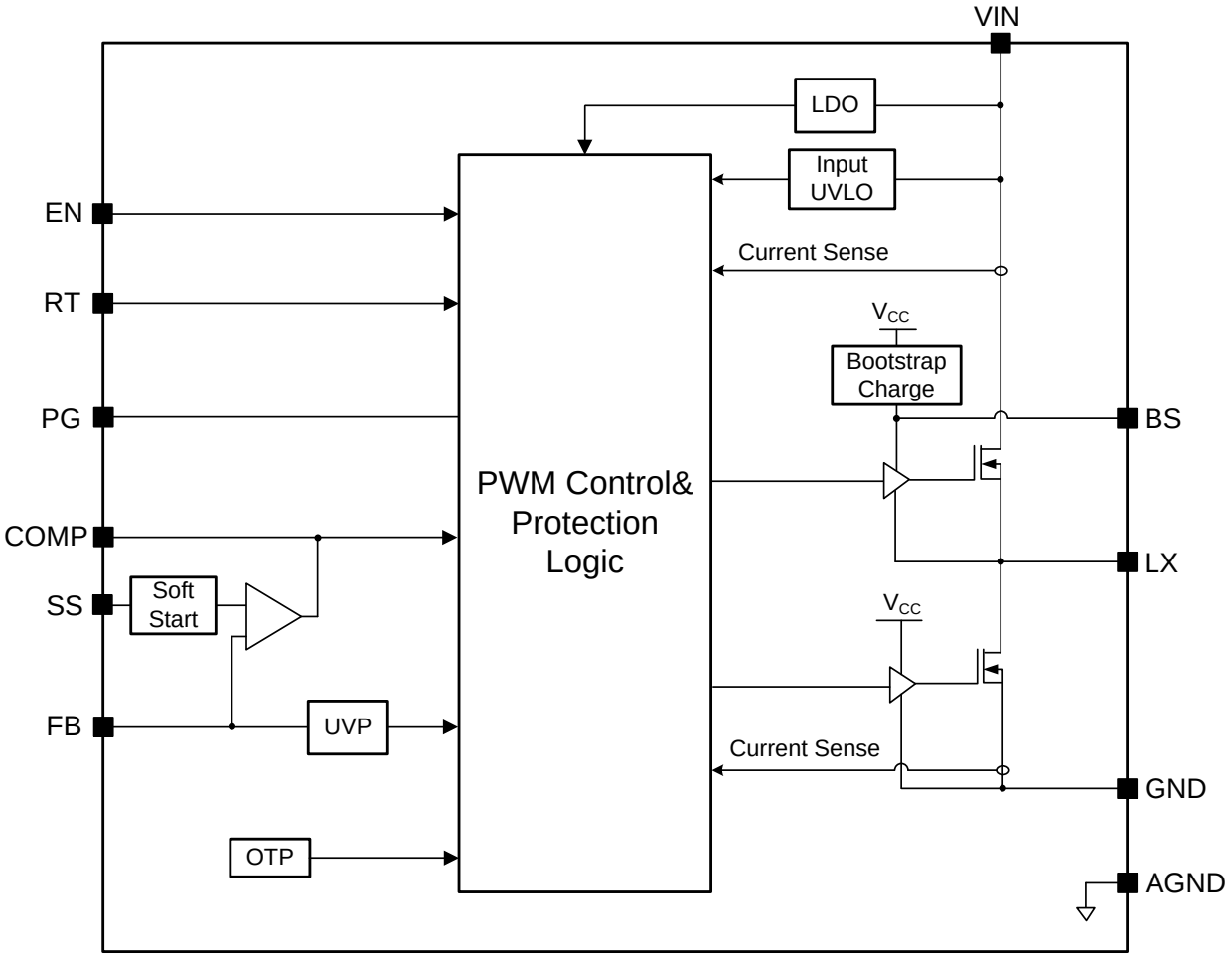



**Figure 3. Block Diagram**

## Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 7.0V
BS-LX, COMP, SS, FB Voltage ---------- -0.3V to 4V
PG, EN, RT Voltage---------- -0.3V to $V_{IN}$ + 0.6V
LX Voltage ---------- -0.3V(*1) to 7V(*2)
Power Dissipation, $P_D$ @ $T_A$ = 25°C, QFN3×3-16----------2.5W
Package Thermal Resistance (Note 2)
$\theta_{JA}$ ---------- 39°C/W
$\theta_{JC\_TOP}$ ---------- 19.5°C/W
$\theta_{JC\_BOT}$ ---------- 2.5°C/W
$\theta_{JB}$ ---------- 13.5°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
(*1) LX Voltage Tested Down to -2V<20ns, -4V<5ns
(*2) LX Voltage Tested Up to +10V<20ns, +12V<5ns

## Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.95V to 6.0V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 105°C

## Electrical Characteristics

($V_{IN}$ = 2.95 to 6V, $T_J$= –40°C to +125°C, unless otherwise specified, the values are guaranteed by design or statistical correlation)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | | 2.95 | | 6 | V |
| Input UVLO Threshold | $V_{UVLO}$ | | | 2.55 | 2.85 | V |
| Quiescent Current | $I_Q$ | $V_{IN}$ = 5V, $V_{FB}$ = 0.6V, $F_{SW}$ = 500kHz, 25°C | | 850 | 1000 | μA |
| Shutdown Current | $I_{SHDN}$ | $V_{EN}$=0V, 25°C | | 1 | 3 | μA |
| Feedback Reference Voltage | $V_{REF}$ | 2.95V ⩽ $V_{IN}$ ⩽ 6V, -40°C <$T_J$< 125°C | 594 | 600 | 606 | mV |
| FB Input Current | $I_{FB}$ | $V_{FB}$=3.3V | -50 | | 50 | nA |
| Top FET $R_{ON}$ | $R_{DS(ON)1}$ | $V_{BS-LX}$ = 3.3V, 25°C | | 12 | 25 | mΩ |
| Bottom FET $R_{ON}$ | $R_{DS(ON)2}$ | $V_{BS-LX}$ = 3.3V, 25°C | | 12 | 25 | mΩ |
| EN Rising Threshold | $V_{EN,R}$ | | 1.24 | 1.3 | 1.37 | V |
| EN Falling Threshold | $V_{EN,F}$ | | 1.12 | 1.18 | 1.24 | V |
| Enable Pull-up Current | $I_{EN}$ | $V_{EN}$>$V_{EN,R}$ | 2.8 | 3.5 | 4.2 | μA |
| | | $V_{EN}$<$V_{EN,F}$ | 0.55 | 0.7 | 0.85 | μA |
| Power Good Threshold | $V_{PG}$ | $V_{FB}$ falling, PG from high to low | 88 | 91 | 94 | %$V_{REF}$ |
| | | $V_{FB}$ rising, PG from low to high | 90 | 93 | 96 | %$V_{REF}$ |
| | | $V_{FB}$ rising, PG from high to low | 112 | 115 | 118 | %$V_{REF}$ |
| | | $V_{FB}$ falling, PG from low to high | 103 | 106 | 109 | %$V_{REF}$ |
| Power Good Delay | $t_{PG,R}$ | $V_{FB}$ falling, PG from low to high | | 10 | | μs |
| | | $V_{FB}$ rising, PG from low to high | | 30 | | μs |
| | $t_{PG,F}$ | $V_{FB}$ rising, PG from high to low | | 5 | | μs |
| | | $V_{FB}$ falling, PG from high to low | | 5 | | μs |
| Power Good Pull Low Resistor | $R_{PG}$ | $V_{IN}$ = 5V | | 20 | | Ω |
| Power Good Output Low | $V_{PG,L}$ | $I_{PG}$=2.5mA | | 0.05 | | V |
| Min ON Time | $t_{ON,MIN}$ | $I_{OUT}$=3A | | 80 | | ns |
| Min OFF Time | $t_{OFF,MIN}$ | $I_{OUT}$=3A | | 70 | | ns |
| Soft-start Charging Current | $I_{SS}$ | | 1.76 | 2.2 | 2.64 | μA |
| SS discharge Resistor | $R_{DIS,SS}$ | UVLO,EN,OTP Shutdown or UVP detected | | | 125 | Ω |
| Switching Frequency Program Range | $f_{SW,RNG}$ | | 200 | | 2000 | kHz |
| Switching Frequency Setting Accuracy | $f_{SW}$ | $R_{RT}$ =82.5kΩ | 400 | 500 | 600 | kHz |
| RT Voltage | | $R_{RT}$ =82.5kΩ | | 0.5 | | V |

## Electrical Characteristics (Continued)

($V_{IN}$ = 2.95 to 6V, $T_J$ = –40°C to +125°C, unless otherwise specified, the values are guaranteed by test design or statistical correlation)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Error Amplifier Trans-conductance | $g_m$ | -2μA <$I_{COMP}$<2μA, $V_{COMP}$=1V | | 245 | | μS |
| Error Amplifier Trans-conductance during soft start | $g_{m\_SS}$ | -2μA <$I_{COMP}$<2μA, $V_{COMP}$=1V, $V_{FB}$=0.4V | | 80 | | μS |
| Error Amplifier Source and Sink | | 100mV Overdrive, $V_{COMP}$=1V | | ±20 | | μA |
| COMP Voltage to Inductor Current | $G_{M,V2I}$ | | | 20 | | A/V |
| Top FET Current Limit | $I_{LMT,TOP}$ | Fsw=500kHz | 9 | 10.5 | 15 | A |
| Bottom FET Current Limit | $I_{LMT,BOT}$ | | 6 | 8.5 | 10 | A |
| Bottom FET Reverse Current Limit | $I_{LMT,RVS}$ | | -6 | -4.5 | -3 | A |
| Output Under Voltage Protection Threshold | $V_{UVP}$ | | | 50 | | %$V_{REF}$ |
| Output UVP Delay | $t_{UVP,DLY}$ | | | 10 | | μs |
| Delay Before Entering Hiccup During Top FET Current Limit | | | | 200 | | μs |
| Thermal Shutdown Temperature | $T_{SD}$ | | | 170 | | ˚C |
| Thermal Shutdown Hysteresis | $T_{HYS}$ | | | 15 | | ˚C |

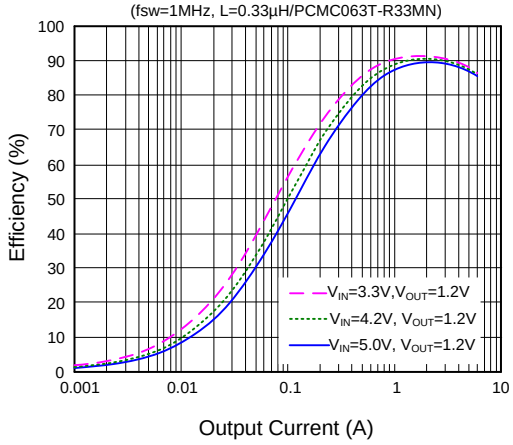
**Note 1**: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2**: $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a high effective 4- layer thermal conductivity test board of JEDEC 51-2 thermal measurement standard.

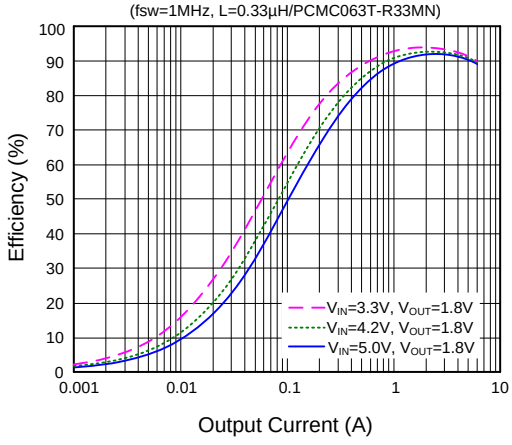
**Note 3:** The device is not guaranteed to function outside its operating conditions.

# Typical Performance Characteristics

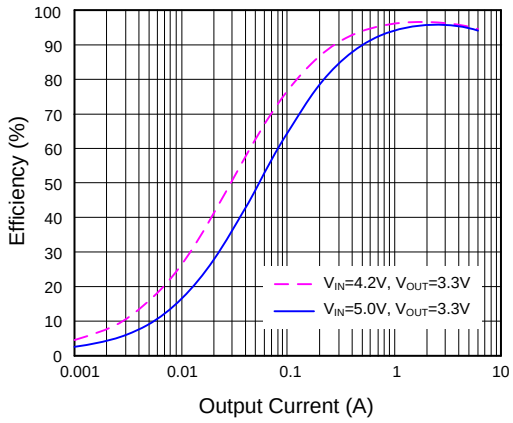
Efficiency vs. Output Current
(fsw=1MHz, L=0.33µH/PCMC063T-R33MN)



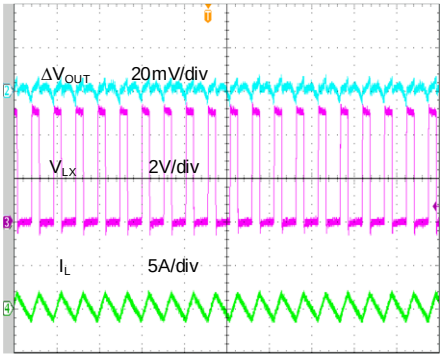

Efficiency vs. Output Current
(fsw=1MHz, L=0.33µH/PCMC063T-R33MN)




Efficiency vs. Output Current
(fsw=1MHz, L=0.33µH/PCMC063T-R33MN)

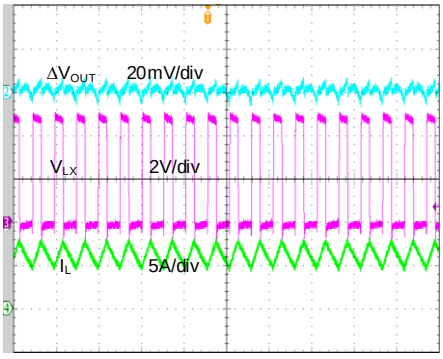



Output Ripple
($V_{IN}$=5.0V, $V_{OUT}$=1.8V, $I_{OUT}$=0A)



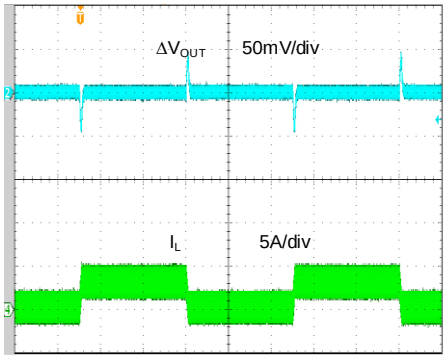

Time (2µs/div)

Output Ripple
($V_{IN}$=5.0V, $V_{OUT}$=1.8V, $I_{OUT}$=6A)




Time (2µs/div)

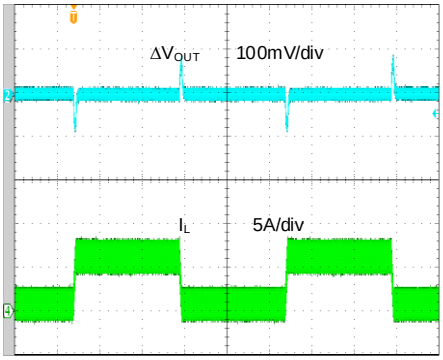
Load Transient
($V_{IN}$=5.0V, $V_{OUT}$=1.8V,$I_{OUT}$=0A~3A~0A)




Time (2ms/div)

Load Transient

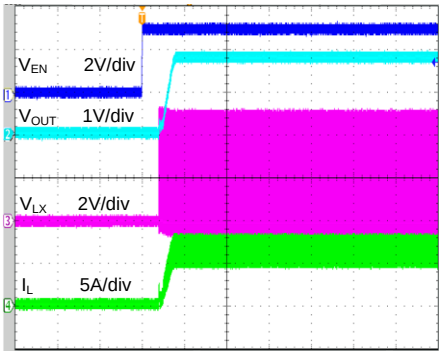
($V_{IN}$=5.0V, $V_{OUT}$=1.8V,$I_{OUT}$=0.6A~6.0A~0.6A)




Time (2ms/div)

Startup from Enable

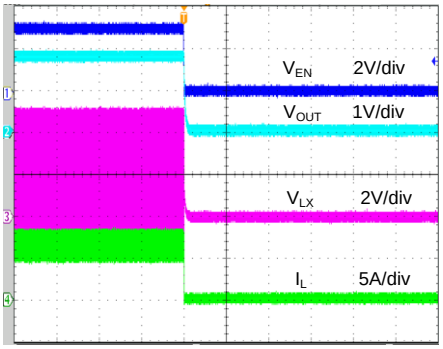
($V_{IN}$=5.0V, $V_{OUT}$=1.8V, $R_{LOAD}$=0.3Ω)




Time (800µs/div)

Shutdown from Enable

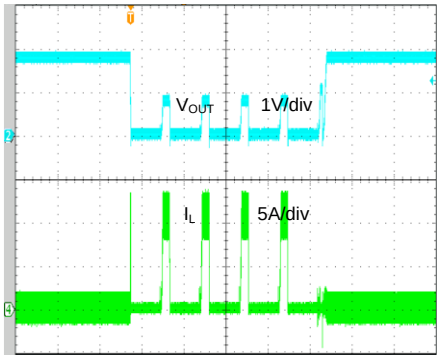
($V_{IN}$=5.0V, $V_{OUT}$=1.8V, $R_{LOAD}$=0.3Ω)




Time (800µs/div)

Short Circuit Protection

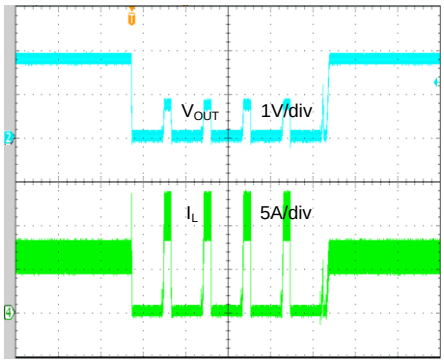
($V_{IN}$=5.0V,$V_{OUT}$=1.8V, $I_{OUT}$=0A~Short~0A)




Time (4ms/div)

Short Circuit Protection

($V_{IN}$=5.0V,$V_{OUT}$=1.8V, $I_{OUT}$=6A~Short~6A)




Time (4ms/div)

# Operation

The SQ28906 develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 6A current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. It provides accurate regulation for a variety of loads with an accurate ±1% voltage reference ($V_{REF}$) over $T_J$= -40°C to 125°C.
The SQ28906 operates over a wide input voltage range from 2.95V to 6V. Cycle-by-cycle current limit, hiccup over current protection and thermal shutdown protect the device during an over current condition.

# Applications Information

Because of the high integration in the SQ28906, the application circuit based on this regulator is rather simple.

**Feedback Resistor Dividers $R_H$ and $R_L$**

Choose $R_H$ and $R_L$ to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both $R_H$ and $R_L$. A value of between 1k and 100k is highly recommended for $R_L$. If $R_L$=10k is chosen, then $R_H$ can be calculated to be:

$$R_H = \frac{(V_{OUT} - 0.6\,V) \times R_L}{0.6V}$$

**Input Capacitor $C_{IN}$**

Two pieces of typical X7R or better grade ceramic capacitors with 10V rating and larger than 10μF capacitance are recommended, another 1μF capacitor with lower ESR should also be needed. These ceramic capacitors need to be placed really close to the IN and GND pins to minimize the potential noise problem. Care should be taken to minimize the loop area formed by $C_{IN}$, and IN/GND pins.

**Output Capacitor $C_{OUT}$**

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use two pieces of X7R or better grade ceramic capacitors with 10V rating and larger than 47μF capacitance.

**Output Inductor L**

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where $f_{SW}$ is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SQ28906 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

**Load Transient Considerations**

The SQ28906 integrates the compensation components to achieve good stability and fast transient responses. In some application, adding a ceramic capacitor (feed-forward capacitor, $C_{ff}$) in parallel with $R_H$ may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements. Typically， for 1.2V/1.8V/3.3V output, the $R_H$, $R_L$, $C_{ff}$ is recommended as below:

**Table1. Recommended Component Selection**

| $V_{OUT}$ | $R_H$ | $R_L$ | $C_{ff}$ |
|---|---|---|---|
| 1.2V | 10kΩ | 10kΩ | 680pF |
| 1.8V | 10kΩ | 5kΩ | 680pF |
| 3.3V | 10kΩ | 2.2kΩ | 680pF |

**Peak Current Limit Protection Method**

With load current increasing, as soon as the high side FET current gets higher than peak current limit threshold, the high side FET will turn off. If the load current continues to increase, the output voltage will drop. When the high side FET triggers peak current limit consecutively for 200μs or the output voltage falls below 50% of the regulation level, the output UVP will be detected and the SQ28906 will operate in hip-cup mode. The hic-cup ON time is 1ms and hic-cup OFF time is 3ms if $C_{SS}$=1nF. If the hard short is removed, the IC will return to normal operation.

**Valley Current Limit Protection Method**

When the low side FET current gets higher than valley current limit threshold, the high side FET is not turned on and skipped during the next clock cycle. Under this condition, the low side FET is kept on until the low side FET current becomes less than valley current limit and then the high side FET is turned on at the beginning of the following clock cycle.

**Reverse Current Limit Method**

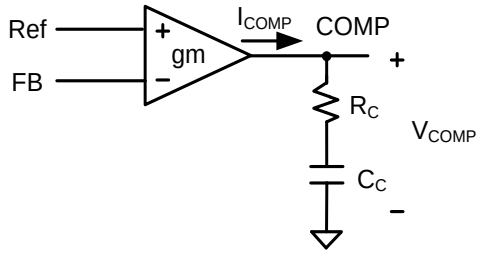
If the low side FET sinking (reverse) current gets higher than reverse current limit threshold, the low side FET is turned off immediately and the high side FET is turned on. The high side FET kept on until high side FET current intersects the COMP voltage.

**Soft Start**

The SQ28906 integrates soft-start function with SS pin. The soft start time can be calculated: $t_{SS}$=0.6Vx$C_{SS}$/2.2μA. If the output capacitor has a pre-biased voltage, the SQ28906 will start with the pre-biased voltage and ramp up to its nominal value.

**Loop Compensation Parameters Selection**

The SQ28906 uses a trans-conductance amplifier for the error amplifier and readily supports a commonly used frequency compensation circuit. The compensation circuit is shown as below. The Type 2 circuit is normally implemented in high bandwidth power supply designs using low ESR output capacitors.




The design guidelines for the SQ28906 loop compensation are as follows:

$$V_{COMP} = I_{COMP} \times \left( R_C + \frac{1}{s \times C_C} \right)$$

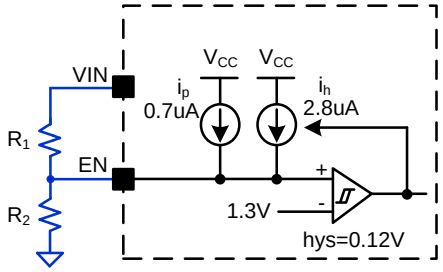
$$\frac{V_{COMP}}{I_{COMP}} = \frac{1}{s \times C_C} \times (1 + s \times R_C \times C_C)$$

$$f_Z = \frac{1}{2\pi \times R_C \times C_C}$$

The $R_C$ and $C_C$ introduce a zero to the loop compensation. Increasing $R_C$ will increase the bandwidth and increasing $C_C$ will decrease the bandwidth. With higher bandwidth, the IC will achieve faster dynamic response speed. However, the higher bandwidth will bring less stability margin. So it is a trade off for dynamic response and stability margin when selecting $R_C$ and $C_C$.

**Input UVLO Programmed by EN Divider Resistor**

For input UVLO, use the EN pin to set up the UVLO by using the two external resistors. Once the EN pin voltage exceeds 1.3 V, an additional 2.8 μA of hysteresis is added. This additional current facilitates input voltage hysteresis. Use equations as below to set the input UVLO rising threshold ($V_{UVLO,R}$) and falling threshold ($V_{UVLO,F}$).




$$R_1 = \frac{V_{UVLO,R} \times \left( \frac{V_{EN,F}}{V_{EN,R}} \right) - V_{UVLO,F}}{i_p \times \left( 1 - \frac{V_{EN,F}}{V_{EN,R}} \right) + i_h}$$

$$R_2 = \frac{R_1 \times V_{EN,F}}{V_{UVLO,F} - V_{EN,F} + R_1 \times (i_p + i_h)}$$

**Switching Frequency Programmed by RT Resistor**

The switching frequency of the SQ28906 is adjustable over a wide range from approximately 200 kHz to 2000 kHz by placing a program resistor on the RT pin. Use equation as below to calculate the RT resistor value for desired switching frequency.

$$R_T(k\Omega) = \frac{56183}{[f_{SW}(kHz)]^{1.052}}$$

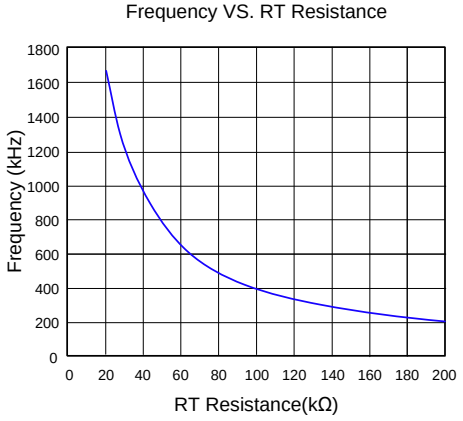



Figure 4. Switching Frequency vs. RT Resistors

**Layout Design**

The layout design of the SQ28906 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: $C_{IN}$, $C_C$, L, $R_{SS}$, $R_T$, $R_C$, $R_H$ and $R_L$.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
2) $C_{IN}$ must be close to the Pins IN and GND. The loop area formed by $C_{IN}$ and GND must be minimized.
3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.
4) The components $R_H$ and $R_L$, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

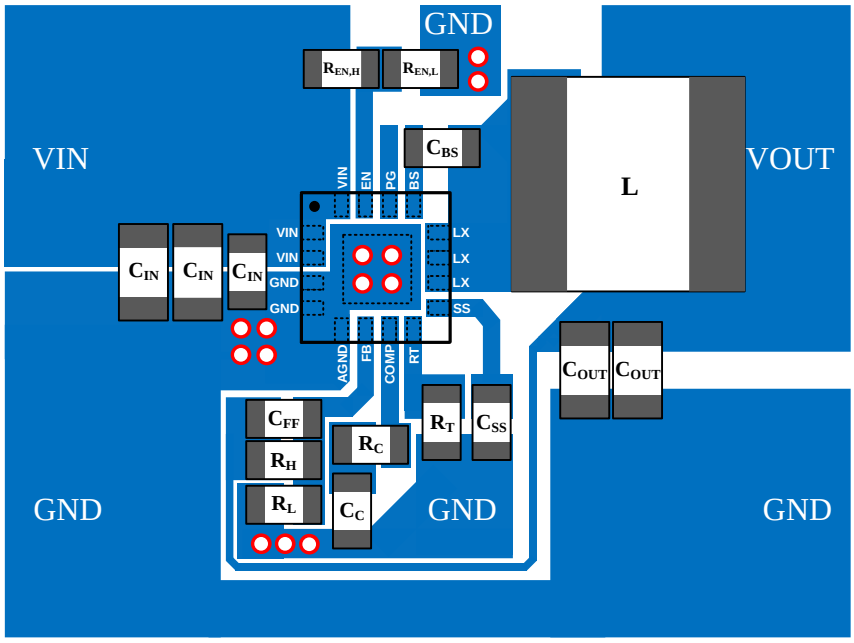
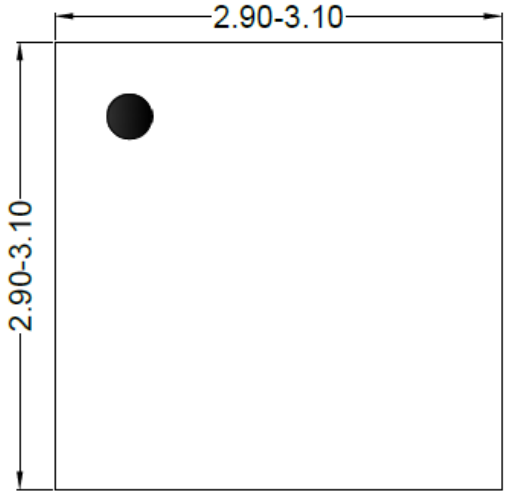
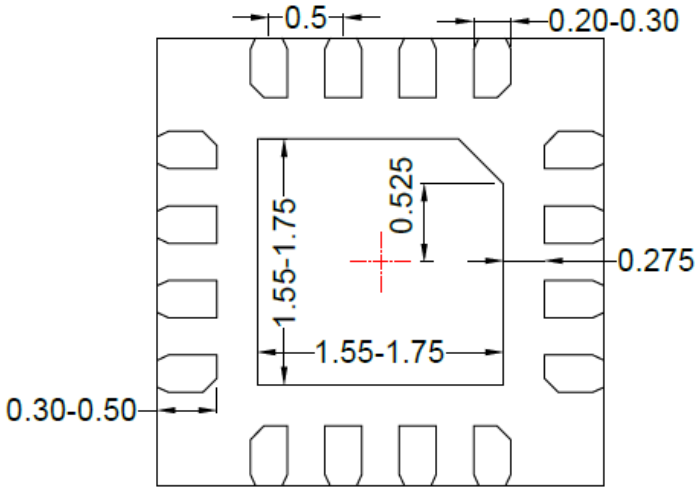



**Figure5. PCB Layout Suggestion**

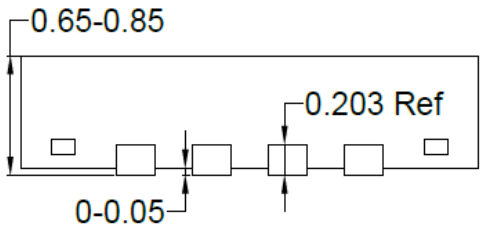
## QFN3×3-16 Package Outline & PCB Layout



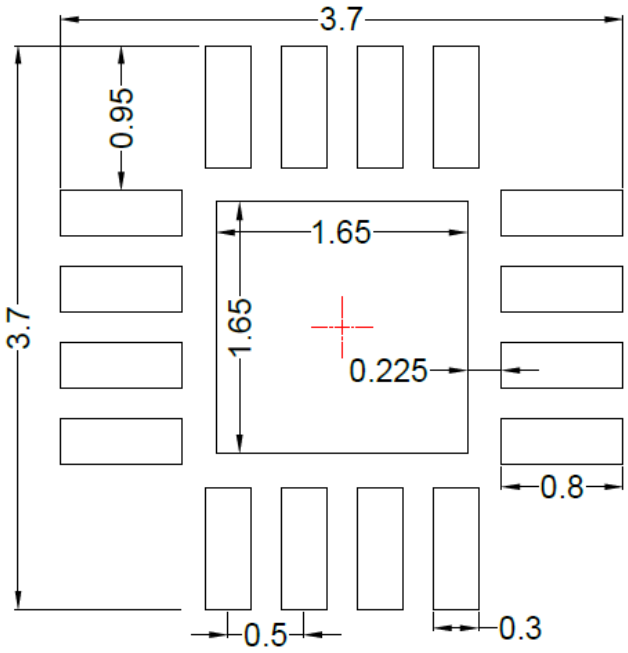

**Top View**




**Bottom View**




**Side View**

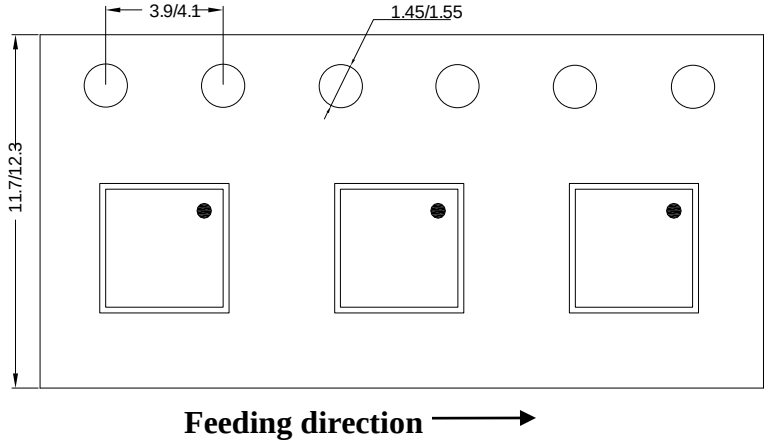



**PCB layout (Recommended)**

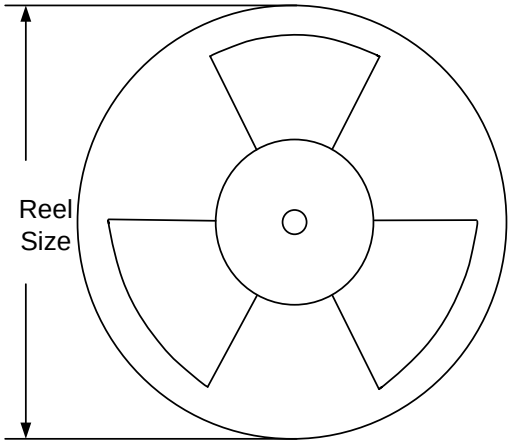
**Notes:** **All dimension in millimeter and exclude mold flash & metal burr.**

# Taping & Reel Specification

## 1. QFN3×3-16 Taping Orientation




## 2. Carrier Tape & Reel Specification for Packages




| Package types | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---|---|---|---|---|---|---|
| QFN3×3 | 12 | 8 | 13" | 400 | 400 | 5000 |

## 3. Others: NA

# Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

| Date | Revision | Change |
|---|---|---|
| Nov.26, 2021 | Revision 0.9C | Update in the taping & reel spec: Pin1 is on the upper right. |
| July 26, 2021 | Revision 0.9B | The recommended ambient temperature range is updated to -40℃ to 105℃ |
| Aug.04, 2020 | Revision 0.9A | Update the package thermal resistance:<br>1. Add $\theta_{JC\_BOT}$ (2.5°C/W);<br>2. $\theta_{JB}$ changes from 22.1°C/W to 13.5°C/W |
| Jul.03, 2020 | Revision 0.9 | Initial Release |

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