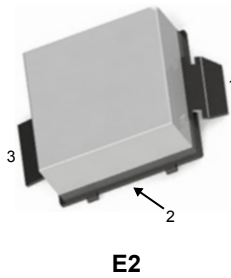


20 W, 28 V, 0.7 to 3.6 GHz RF power LDMOS transistor



Pin connection	
Pin	Connection
1	Drain
2	Source (bottom side)
3	Gate

Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
ST36015	3450 MHz	28 V	20 W	12.4 dB	42%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internal input matching for ease of use
- Large positive and negative gate-source voltage range for improved class C operation
- In compliance with the European directive 2002/95/EC

Applications

- Telecom and wideband communication
- Industrial, scientific and medical (ISM)

Description

The **ST36015** is a 20 W, 28 V, internally matched LDMOS transistor designed for cellular base stations and ISM applications in the frequency range from 0.7 to 3.6 GHz.



Product status link
ST36015

Product summary	
Order code	ST36015
Marking	ST36015
Package	E2
Packing	Tape and reel 13"
Base/bulk quantity	300/300

1 Electrical ratings

Table 1. Absolute maximum ratings ($T_C = 25\text{ °C}$)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	65	V
V_{GS}	Gate-source voltage	-6 to 10	V
V_{DD}	Drain supply voltage	32	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}^{(1)}$	Thermal resistance, junction-to-case	2	°C/W

1. $T_C = 80\text{ °C}$, $T_J = 200\text{ °C}$, DC test.

Table 3. ESD protection

Symbol	Parameter	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	1B
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS002-2014)	C3

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 4. Static

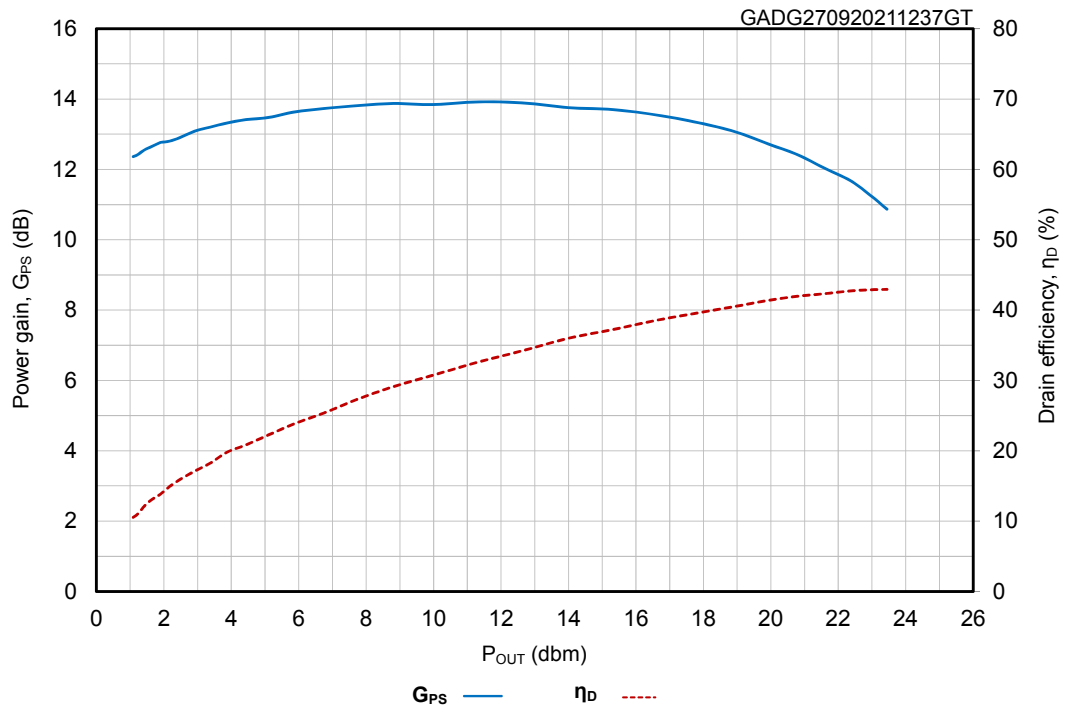
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 100\text{ }\mu\text{A}$	65			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 28\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$			1	
I_{GSS}	Gate-body leakage current	$V_{GS} = -6/10\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 28\text{ V}$, $I_D = 600\text{ }\mu\text{A}$	1.5		2.5	V
$V_{DS(on)}$	Static drain-source on-voltage	$V_{GS} = 10\text{ V}$, $I_D = 200\text{ mA}$			0.25	V
$I_{DS(on)}$	Static drain-source on-current	$V_{GS} = 10\text{ V}$, $V_{DS} = 100\text{ mV}$			2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}$, $I_D = 0.18\text{ A}$			1	Ω
		$V_{GS} = 10\text{ V}$, $I_D = 0.75\text{ A}$			1	
C_{ISS}	Common source input capacitance			37		pF
C_{RSS}	Common source feedback capacitance	$V_{GS} = 0\text{ V}$, $V_{DD} = 28\text{ V}$, $f = 1\text{ MHz}$		0.3		pF
C_{OSS}	Common source output capacitance			8.4		pF

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power		-	20		W
G_{PS}	Power gain	$V_{DD} = 28\text{ V}$, $I_{DQ} = 10\text{ mA}$, $f = 3450\text{ MHz}$, pulse width = $10\text{ }\mu\text{s}$, DC = 10%	-	12.4		dB
η_D	Drain efficiency		-	42		%
VSWR	Load mismatch	$P_{OUT} = 20\text{ W}$, all phases	-		10:1	

3 Typical performance

Figure 1. Power gain and drain efficiency vs output power at 3450 MHz



4 Test circuits

Figure 2. Test circuit photo

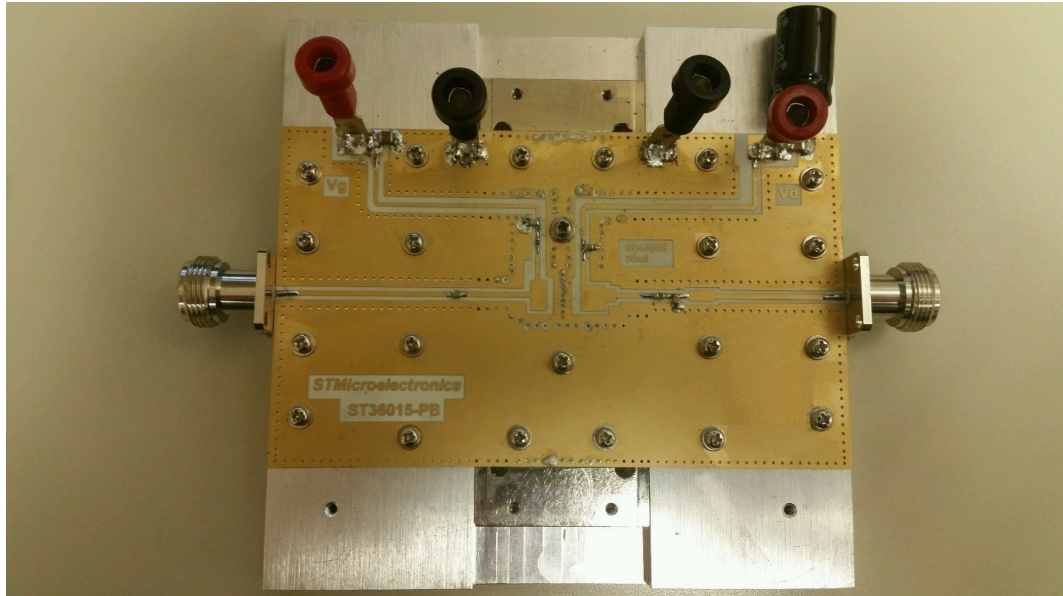
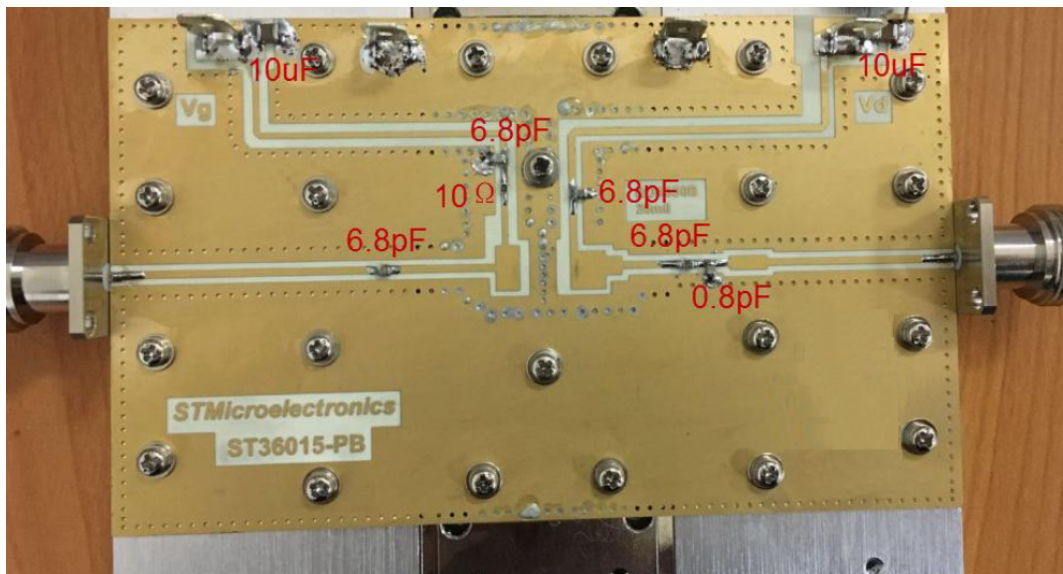


Figure 3. Test circuit components

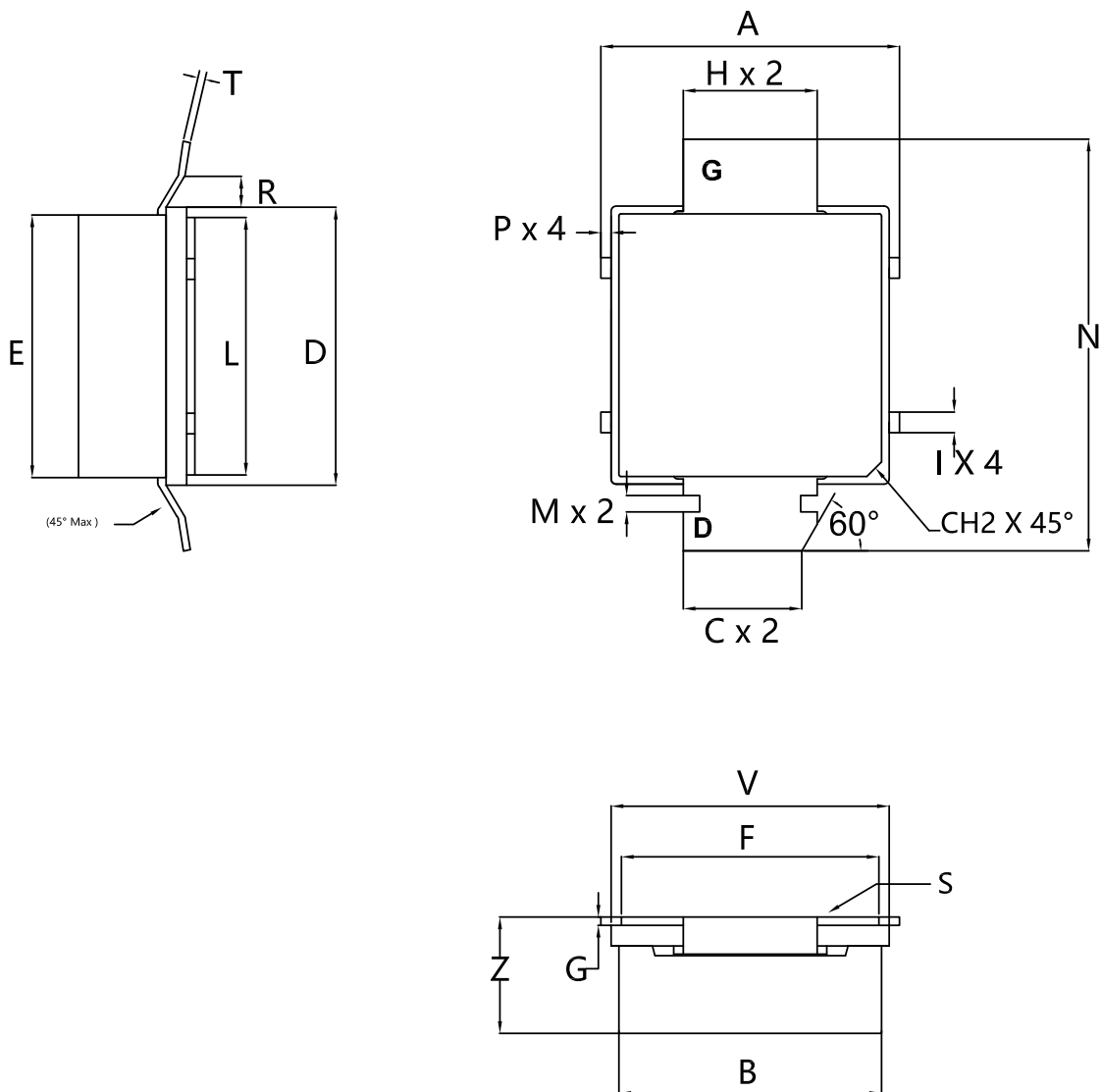


5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 E2 package information

Figure 4. E2 package outline



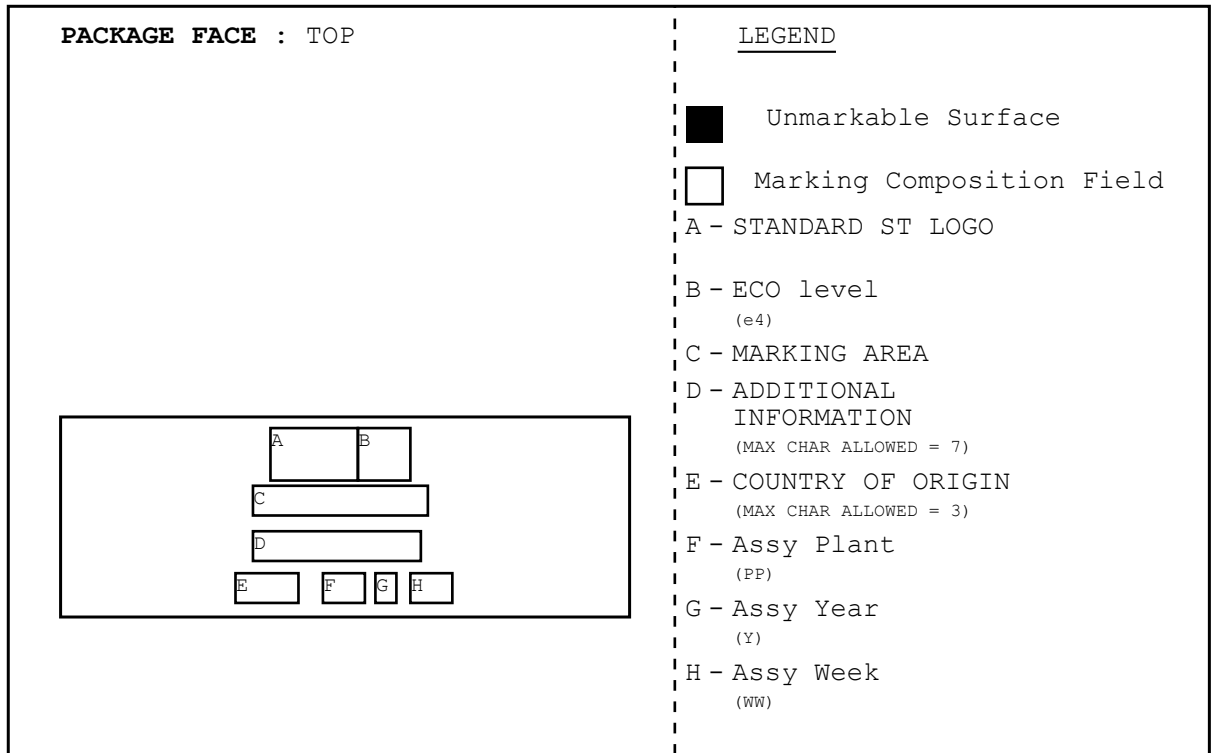
00418523_4

Table 6. E2 mechanical data

Symbol	Millimetres		
	Min.	Typ.	Max.
A			7.37
B	6.35	6.48	6.60
C	2.84	2.92	3.0
D	6.78	6.86	6.94
E	6.35	6.48	6.61
F	6.10	6.35	6.60
G	0.18	0.20	0.23
H	3.23	3.30	3.38
I	0.43	0.51	0.59
L	6.27	6.35	6.43
M	0.33	0.41	0.49
N	10.03	10.16	10.29
P			0.25
R	0.76		1.02
T	0.13	0.18	0.23
V	6.78	6.86	6.94
Z	2.49	2.87	3.25
CH2		0.51	

5.2 Marking information

Figure 5. Marking composition



GADG040220211644GT

Revision history

Table 7. Document revision history

Date	Revision	Changes
12-Sep-2018	1	Initial release
02-Oct-2018	2	Added <i>Section 3 Circuit layout</i> .
08-Sep-2020	3	Updated <i>Section Product status / summary</i> , <i>Table 5</i> and <i>Section 4.1 E2 package information</i> .
27-Sep-2021	4	Updated <i>Description</i> in cover page. Updated <i>Section 1 Electrical ratings</i> . Updated <i>Section 2 Electrical characteristics</i> . Updated <i>Figure 1. Power gain and drain efficiency vs output power at 3450 MHz</i> . Added <i>Section 5.2 Marking information</i> . Minor text changes.

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