MAX11947

4 Channel AISG Integrated Modem

General Description

The MAX11947 is an AISG v2.0 and v3.0-compliant, fully integrated modem with a 4:1 multiplexer facilitating connectivity between a single modem and up to four RF ports. The MAX11947 receiver offers a typical dynamic range of 20dB and integrates a bandpass filter that operates at the 2.176MHz carrier frequency with a narrow 200kHz bandwidth and is fully compliant with the AISG spectral emission profile. It can modulate OOK signals at the required 9.6kbps and up to 115.2kbps for back compatibility with the older AISG standard. The output power can be varied with an internal register setting from under 0dBm to over +6dBm in order to compensate for loss in the external circuitry and cabling. The receiver sensitivity threshold is also adjustable from the default -15dBm down to less than -20dBm to accommodate power loss through an external splitter. The MAX11947 also features a direction output to facilitate the RS-485 bus arbitration in tower-mounted equipment. The MAX11947 is available in a small, 4mm x 4mm 20-pin TQFN and is rated for operation in the -40°C to +105°C temperature range.

Applications

- Base Station Single and Multi-Primary Controllers (SALD and MALD)
- Antenna Line Devices (ALDs)
- Antenna Arrays
- Tower-Mounted Amplifiers (TMAs)
- Smart Bias-Ts
- RS485 Half-Duplex Coaxial Links
- 2MHz OOK Modem Applications

Benefits and Features

- AISG v3.0 Compliant
- Fully Integrated Modem with 4:1 Multiplexer Facilitates Connectivity Between 1 Modem and Up to 4 Ports
- Receiver Wide Input Dynamic Range
  - -23dBm to +5dBm into 50Ω
- Adjustable Receiver Sensitivity Threshold from -20.5dBm to -15dBm
- Adjustable Transmitter Output Level from -0.5dBm to +7.0dBm into 50Ω
- AISG v3.0/v2.0 Compliant Output Emission Profile
- Autodirection Output
- No Need of Microcontrollers to Handle Bus Arbitration in Tower-Mounted Equipment
- Support All AISG v2.0 Data Rates
  - 9.6kbps (default) for AISG v3.0
  - 38.4kbps and 115.2kbps for Backward Compatibility
- Bandpass Filter Compliant with AISG v3.0 Protocol Centered on 2.176MHz
- 3.0V to 5.5V Voltage Supply
- Independent Logic Supply
- Small, 4mm x 4mm 20-Pin TQFN Package

Ordering Information appears at end of data sheet.

19-100411; Rev 0; 2/20

maxim integrated™

Simplified Block Diagram

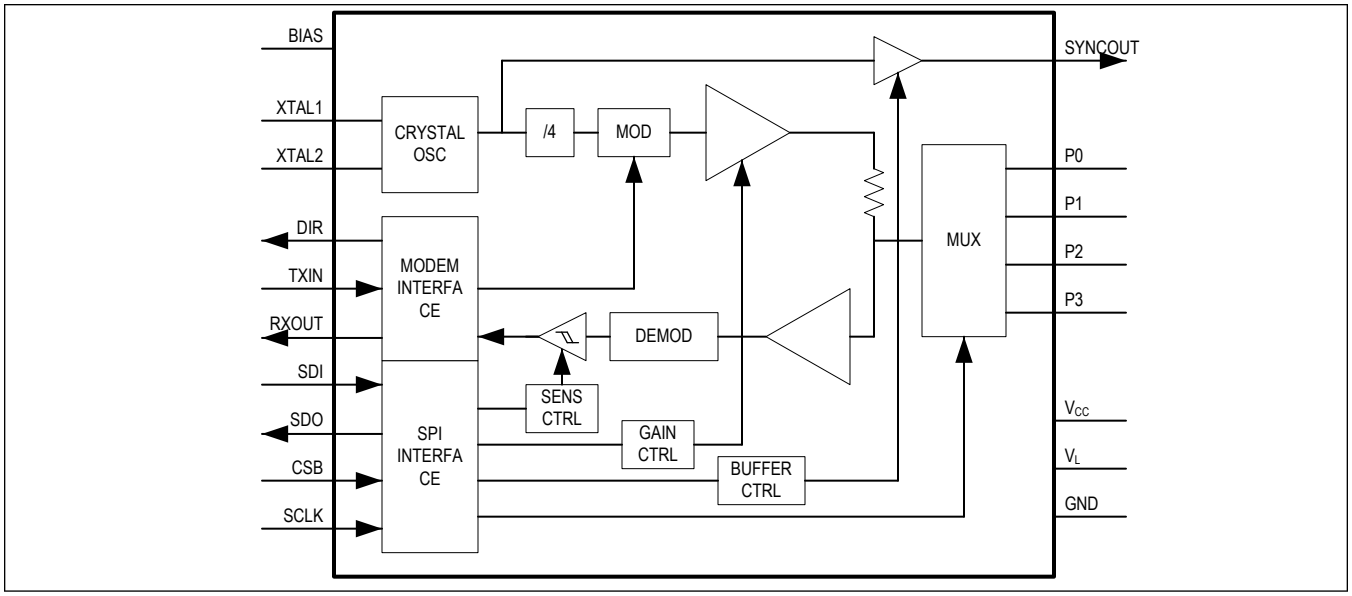


TABLE OF CONTENTS

General Description . . . 1
Applications . . . 1
Benefits and Features . . . 1
Simplified Block Diagram . . . 2
Absolute Maximum Ratings . . . 7
Package Information . . . 7
20-Pin TQFN . . . 7
Electrical Characteristics . . . 7
Typical Operating Characteristics . . . 13
Pin Configuration . . . 16
MAX11947 . . . 16
Pin Description . . . 16
Functional Diagrams . . . 17
Diagram 1 . . . 17
Detailed Description . . . 18
4:1 Multiplexer . . . 18
Internal Termination . . . 21
Receiver . . . 21
Transmitter . . . 22
Carrier Tone . . . 23
Direction Output . . . 23
Serial Peripheral Interface (SPI) . . . 24
Standby and Power-Down . . . 25
Port Scanning . . . 27
Status Bits . . . 30
Register Map . . . 31
Register Map . . . 31
Register Details . . . 31
Applications Information . . . 37
Emission Output Profile . . . 37
RF Filter and Selectivity . . . 37
External Low-Pass Filter and AC-Coupling to Feeder Cable . . . 39
In-Line Attenuation . . . 40
Crystal and External Clock . . . 41
Dwell Time . . . 43
Alternate Modem Interface . . . 43
Typical Application Circuit . . . 44
Circuit 1 . . . 44

TABLE OF CONTENTS (CONTINUED)

Ordering Information 44
Revision History 45

LIST OF FIGURES

Figure 1. SPI Timing 12
Figure 2. MUX Port Diagram 18
Figure 3. Switch Timing 19
Figure 4. RF Isolation 19
Figure 5. AISG Isolation 20
Figure 6. Modem Crosstalk 21
Figure 7. Receiver Timing 22
Figure 8. Transmitter Timing 23
Figure 9. Receiver Communication Flow 24
Figure 10. Transmitter Communication Flow 24
Figure 11. SPI Write Transaction 25
Figure 12. SPI Read Transaction 25
Figure 13. Power Modes 26
Figure 14. Port Scan Flow Chart 28
Figure 15. AISG v3.0 Standard Modem Spectrum Emissions Mask 37
Figure 16. AISG Selectivity No-ON Test Conditions 38
Figure 17. AISG Selectivity Forced-ON Test Conditions 38
Figure 18. AISG Selectivity No-OFF Test Conditions 39
Figure 19. RF Port Filter 39
Figure 20. Transmit and Receive Levels 40
Figure 21. AISG—OOK Bypass 40
Figure 22. Higher Power Transmitter for Splitter 41
Figure 23. Better Sensitivity Threshold for Receiver with Splitter 41
Figure 24. Clock Master/Slave Circuit 42
Figure 25. Cascade Daisy-Chain 42
Figure 26. Star Daisy-Chain 42

LIST OF TABLES

Table 1. RFPORT Register Settings 21
Table 2. DATARATE Register Settings 24
Table 3. SPI Pins 25
Table 4. SCAN_DWELL Time 28
Table 5. User-Programmed Dwell Time 29
Table 6. Alternate Modem Interface 43

Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to +6V
V_L to GND ..... -0.3V to +6V
P0, P1, P2, P3, XTAL1, XTAL2, BIAS, SYNCOUT to GND .-0.3V to +6V
TXIN, RXOUT, DIR, SDI, SDO, SCLK, CSB to GND -0.3V to (V_L +0.3)V
Output Short-Circuit Current P_ While Transmitting, SYNCOUT to V_{CC} or GND ..... Continuous
All Other Pins Max In/Out Current .....±20mA
Continuous Power Dissipation (T_A = +70°C) 20-pin TQFN (derate 30.2mW/°C) 2415mW
Operating Temperature Range .....-40°C to +105°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

20-Pin TQFN

Package Code	T2044+4
Outline Number	21-0139
Land Pattern Number	90-0429
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	48°C/W
Junction to Case (θ_{JC})	2°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	33°C/W
Junction to Case (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{CC} = 5V, V_L = 3.3V, TXPWR = 0x7 (+3dBm), RXSENS = 0xB (-15dBm), DATARATE = 0x0 (9.6kbps), OSCBUF = 0x1, 1kΩ resistor between SYNCOUT and V_{CC}, XTAL frequency 8.704MHz ±30ppm. T_A = -40°C to +105°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Supply Voltage	V_{CC}	Guaranteed by PSRR		3.0		5.5	V
Supply Current	I_{CC}	V_{TXIN} = 0V	$T_A \le 85°C$		24	35	mA
			$T_A > 85°C$ (typ measured at 85°C)		26	37	
Logic Supply Voltage	V_L	Guaranteed by logic supply current		1.6		5.5	V
Logic Supply Current	I_L	V_{TXIN} = V_L (logic-high)			236	380	µA
Standby Current	I_{CC-SB}	V_{TXIN} = V_L, STANDBY = 0x1			13	20	mA
	I_{L-SB}				236	380	µA
Power-Down Current	I_{CC-PD}	V_{TXIN} = V_L, PWRDN = 0x1, XTALOSC = 0x0			0.8	2	mA
	I_{L-PD}				60	120	µA

Electrical Characteristics (continued)

(V_{CC} = 5V, V_L = 3.3V, TXPWR = 0x7 (+3dBm), RXSENS = 0xB (-15dBm), DATARATE = 0x0 (9.6kbps), OSCBUF = 0x1, 1kΩ resistor between SYNCOUT and V_{CC}, XTAL frequency 8.704MHz ±30ppm. T_A = -40°C to +105°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Receiver Power-Supply Rejection Ratio	$PSRR_{RX}$	3.0V ≤ V_{CC} ≤ 5.5V, V_{TXIN} = V_L (Note 2)			54		dB
Transmitter Power-Supply Rejection Ratio	$PSRR_{TX}$	3.0V ≤ V_{CC} ≤ 5.5V, V_{TXIN} = 0V (Note 3)			42		dB
LOGIC INPUTS (TXIN, SDI, CSB, SCLK)							
Logic-Input High Threshold Voltage	V_{IH}			0.7 x V_L			V
Logic Input Low Threshold Voltage	V_{IL}					0.3 x V_L	V
Input Leakage Current	I_{IH}, I_{IL}	Shorted to GND or V_L				±1	µA
LOGIC OUTPUTS (RXOUT, SDO, DIR)							
Logic-Output High Level Voltage	V_{OH}	Sourcing 3.3mA		0.9 x V_L			V
Logic-Output Low Level Voltage	V_{OL}	Sinking 3.3mA				0.1 x V_L	V
SYNC INPUT (XTAL1) AND OUTPUT (SYNCOUT)							
Input High Threshold Voltage	$V_{IH-XTAL1}$			0.7 x V_{CC}			V
Input Low Threshold Voltage	$V_{IL-XTAL1}$					0.3 x V_{CC}	V
Input Leakage Current	$I_{IH-XTAL1}$, $I_{IL-XTAL1}$					±10	µA
Output Low Voltage	$V_{OL-SYNCOUT}$	OSCBUF = 0x1, SYNCOUT sinking 5mA				0.4	V
Output Low Current	$I_{OL-SYNCOUT}$	$V_{SYNCOUT}$ = 0.0V	OSCBUF = 0x0 (disabled), SYNCOUT open	-1		+1	µA
			OSCBUF = 0x1 (default), SYNCOUT 1kΩ resistor to V_{CC}		5		mA
			OSCBUF = 0x2, SYNCOUT 500Ω resistor to V_{CC}		10		
			OSCBUF = 0x3, SYNCOUT 250Ω resistor to V_{CC}		20		
RECEIVER							
Maximum Input Level	P_{IN}	V_{CC} = 3.0V to 5.5V, f_{IN} = 2.176MHz		+5			dBm
	V_{IN}	V_{CC} = 3.0V to 5.5V, f_{IN} = 2.176MHz		1.12			V_{P-P}
AISG Threshold Window	P_{TH}	f_{IN} = 2.176MHz, RXSENS = 0xB (default) (Note 12)		-18	-15	-12	dBm
	V_{TH}			79.6	112.5	158.8	mV_{P-P}

Electrical Characteristics (continued)

(V_{CC} = 5V, V_L = 3.3V, TXPWR = 0x7 (+3dBm), RXSENS = 0xB (-15dBm), DATARATE = 0x0 (9.6kbps), OSCBUF = 0x1, 1kΩ resistor between SYNCOUT and V_{CC}, XTAL frequency 8.704MHz ±30ppm. T_A = -40°C to +105°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Threshold Adjustment Range	P_{TH-ADJ}	f_{IN} = 2.176MHz, RXSENS ≥ 0xB			-15		dBm
		f_{IN} = 2.176MHz, RXSENS = 0x0			-20.5		
Threshold Adjustment Resolution	P_{TH-RES}	Excluding codes ≥ 0xC			0.5		dB
RECEIVER FILTER							
Passband	f_{PB-L}, f_{PB-H}	Input amplitude -12dBm (the input carrier is recognized), RXSENS = 0xF (Note 13)		1.25		3.7	MHz
Selectivity	f_{IML}	2.176MHz carrier amplitude -18dBm, extra carrier amplitude -13dBm, DATARATE = 0x0 (9.6kbps), RXSENS = 0xF (Note 14)	f_{IML} = 9kHz to 1.5MHz	1.25	2.0		MHz
	f_{IMH}		f_{IMH} = 3.0MHz to 10.0MHz		2.7	3.7	
TRANSMITTER							
Output Frequency	f_O				2.176		MHz
Output Frequency Variation	Δf_O	(Note 4)				±100	ppm
AISG Output ON Level	P_{OUT}	TXPWR = 0x7 (default) (Note 5)		+1.0	+3.0	+5.0	dBm
	V_{OUT}			0.709	0.893	1.125	V_{P-P}
Output Power Adjustment Range	$P_{OUT-ADJ}$	TXPWR = 0xF (Note 5)			+7.0		dBm
		TXPWR = 0x0 (Note 5)			-0.5		
Output Power Adjustment Resolution	$P_{OUT-RES}$	(Note 5)			0.5		dB
AISG Output OFF Power	P_{OUT}	OOK off level (Note 5)			-65	-40	dBm
AISG Output Emission Profile		(Note 6)			Conforms to AISG v3.0 Spectrum Emissions Mask 3GPP TS 25.461, See Figure 15		
Amplifier Gain Bandwidth	GBW				54		MHz

Electrical Characteristics (continued)

(V_{CC} = 5V, V_L = 3.3V, TXPWR = 0x7 (+3dBm), RXSENS = 0xB (-15dBm), DATARATE = 0x0 (9.6kbps), OSCBUF = 0x1, 1kΩ resistor between SYNCOUT and V_{CC}, XTAL frequency 8.704MHz ±30ppm. T_A = -40°C to +105°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RF Port Short-Circuit Current	I_{SC}	Short to GND or V_{CC}, guaranteed over V_{CC} range, limited by internal resistor				±100	mA
SWITCHING CHARACTERISTICS							
Receiver Propagation Delay	t_{RX}	Selected RF Port P_ to RXOUT	DATARATE = 0x0 (9.6kbps, default)		6.5	11	µs
			DATARATE = 0x1 (38.4KBPS)		3.1	11	
			DATARATE = 0x2 (115.2kbps)		3.1	11	
Receiver Output Rise and Fall Time	t_R, t_F	10% to 90%, R_L = 1kΩ, C_L = 10pF			20		ns
Transmitter Propagation Delay	t_{TX}	TXIN to selected RF port P_			1.8	5	µs
DIR to RXOUT Delay (Note 7)	$t_{DIR-SKEW}$			270	345		ns
DIR Dwell Time	t_{DWELL}	DATARATE = 0x0 (9.6kbps, default)			1667		µs
		DATARATE = 0x1 (38.4kbps)			417		
		DATARATE = 0x2 (115.2kbps)			137		
Receiver Output Data Duty-Cycle Variation	ΔDC	P_ fed by an OOK 2.176MHz sinusoidal signal with 50% duty cycle (Note 8)	P_ = 0dBm		-7.5	±10	%
			P_ = -10dBm		+2	±10	
			DATARATE = 0x2 (115.2kbps)		+11	±15	
RF PORT MUX							
Input Impedance	Z_{IN}	f = 2.176MHz			50		Ω
Return Loss	S_{11}	f = 2.176MHz, with a 470pF capacitor			16		dB
RF Port Isolation	S_{RFVA}	Scatter parameter P_V measured at victim port, aggressor port P_A = +10dBm, f_A = 500MHz~5.0GHz (Note 9)			-45		dBc
AISG Port Isolation	S_{MVA}	Scatter parameter P_V measured at victim port, aggressor port P_A = +5dBm, f_A = 2.176MHz			-60		dBc
Modem Crosstalk	$XTLK_{RX}$	Aggressor port P_A = +5dBm, f_A = 2.176MHz, Victim port RXSENS = 0x0 (-20.5dBm) (Note 11)			-42		dBc
	$XTLK_{TX}$	TXPWR = 0xF (+7dBm) (Note 11)			-65		
Switch Time	t_{SW}	Carrier P_0 = +3dBm, f_0 = 2.176MHz (Note 10)			345		ns
SERIAL INTERFACE (Figure 1)							
SCLK Frequency	f_{SCLK}	$1/t_{SCLK}$, sensitive to V_L	V_L = ≥ 2.0V		20	10	MHz
			V_L = < 2.0V		8	5	

Electrical Characteristics (continued)

(V_{CC} = 5V, V_L = 3.3V, TXPWR = 0x7 (+3dBm), RXSENS = 0xB (-15dBm), DATARATE = 0x0 (9.6kbps), OSCBUF = 0x1, 1kΩ resistor between SYNCOUT and V_{CC}, XTAL frequency 8.704MHz ±30ppm. T_A = -40°C to +105°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCLK to CSB Setup Time	t_{CSS}				20		ns
SCLK to CSB Hold Time	t_{CSH}				0		ns
SDI to SCLK Hold Time	t_{SDH}	Data-write			0		ns
SDI to SCLK Setup Time	t_{SDS}	Data-write			20		ns
Minimum SCLK to SDO Data Delay	$t_{SDD-MIN}$	Data-read	10pF load from SDO to GND		1.5		ns
			100pF load from SDO to GND		3.5		
Maximum SCLK to SDO Data Delay	$t_{SDD-MAX}$	Data-read	10pF load from SDO to GND		8		ns
			100pF load from SDO to GND		11		

Note 1: All devices are 100% production tested at T_A = +25°C. Specification over temperature limits are guaranteed by design.

Note 2: Defined as $20 \cdot \log(\Delta V_{CC}/\Delta V_{TH})$.

Note 3: Defined as $20 \cdot \log(\Delta V_{CC}/\Delta V_{OUT})$, this value is impacted by the internal resistor voltage and temperature coefficient.

Note 4: Output frequency variation determined by external crystal tolerance. Not production tested, guaranteed by design and characterization.

Note 5: Measured at selected RF port, P_. See **Output Power Control** in the *Transmitter* section for power setting details.

Note 6: Guaranteed by design, with a recommended 470pF capacitor between the RF port (P_) and ground. Results above 150MHz are influenced by setup.

Note 7: See Figure 7.

Note 8: ±2µs envelope rise/fall.

Note 9: Excludes external LPF on the input of the aggressor port, see the *External Lowpass Filter and AC-Coupling to Feeder Cable* section.

Note 10: Switch time is defined from the rising edge of 16th SCLK during a change to the RFPORT register to the settled DC bias on the selected RF port. See Figure 3.

Note 11: Receive modem crosstalk is measured with the most sensitive (lowest dBm level) setting and a high-power aggressor signal applied to any unselected port. Transmit modem crosstalk is measured with a power meter connected to any unslected port with the transmitter set to the highest power level and the TX_ON bit set to 1 in the CFG register (0x00).

Note 12: AISG specifies an input power window with defined thresholds: above -12dBm is a recognized ON state, below -18dBm is a recognized OFF state (-15dBm ±3dB), in between signal power levels are undefined. The MAX11947 nominal threshold is -15dBm.

Note 13: A tighter receiver filter passband provides better receiver performance and improved extra carrier rejection (selectivity) outside of that band. The device meets AISG v3.0.0.10 section 10.3.12.1 Device Selectivity requirements with a typical passband of 2.0MHz to 2.7MHz where AISG requires 1.25MHz to 3.7MHz. See the *RF Filter and Selectivity* section for more information.

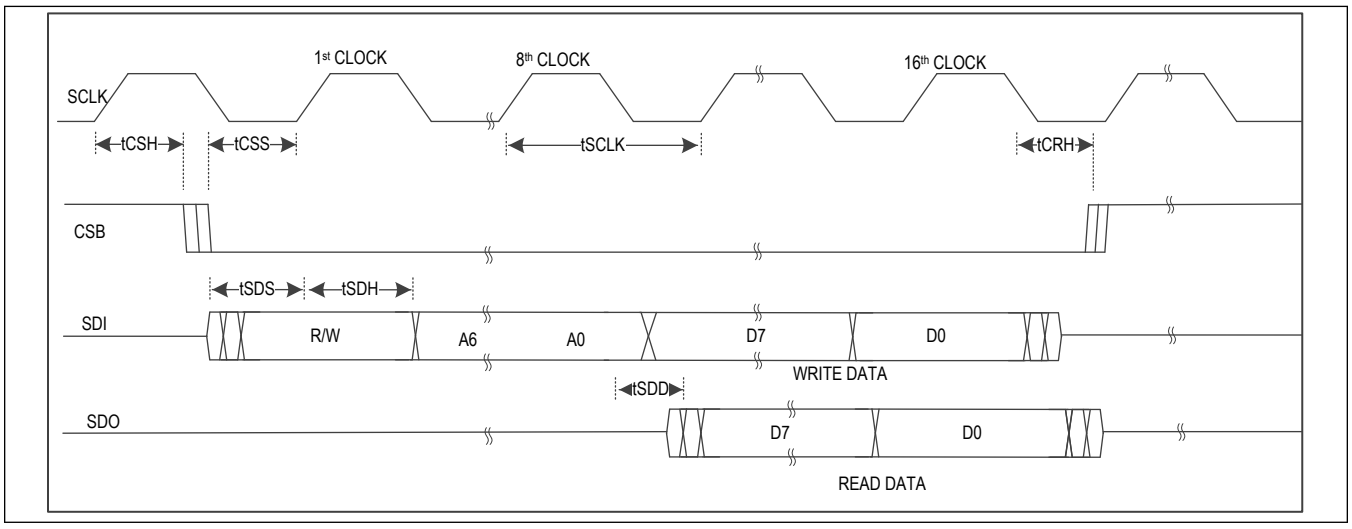
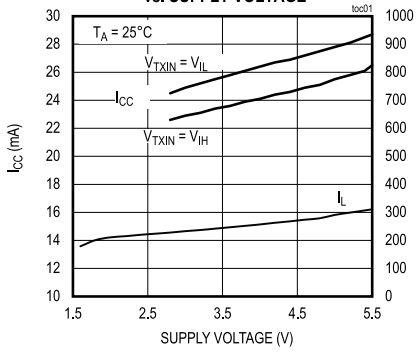


Figure 1. SPI Timing

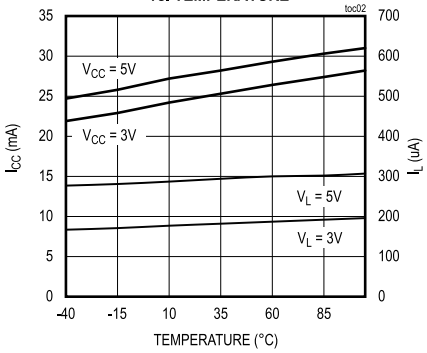
Typical Operating Characteristics

(V_{CC} = 5V, V_L = 3.3V, TXPWR = 0x7 (+3dBm), RXSENS = 0xB (-15dBm), DATARATE = 0x0 (9.6kbps), OSCBUF = 0.0, pullup on SYNCOUT with 1kΩ to V_L, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.)

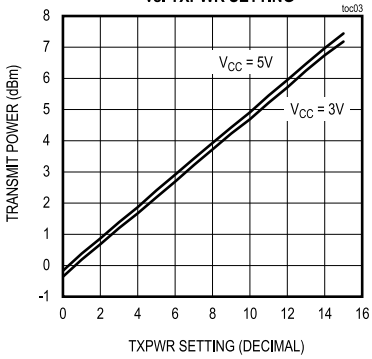
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



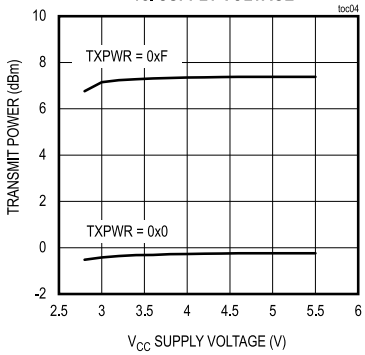
QUIESCENT CURRENT vs. TEMPERATURE



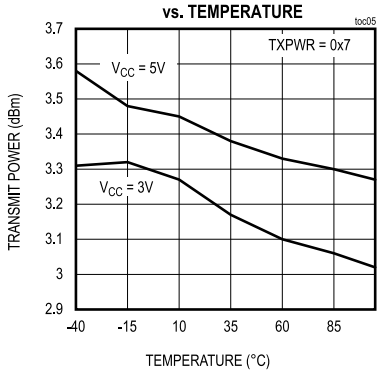
TRANSMIT POWER vs. TXPWR SETTING



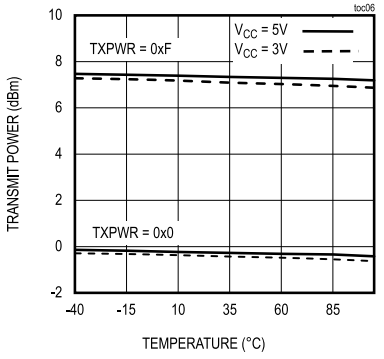
TRANSMIT POWER RANGE vs. SUPPLY VOLTAGE



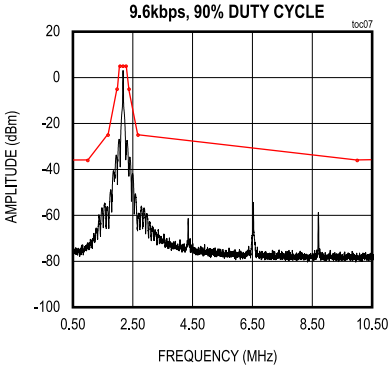
NOMINAL TRANSMIT POWER vs. TEMPERATURE



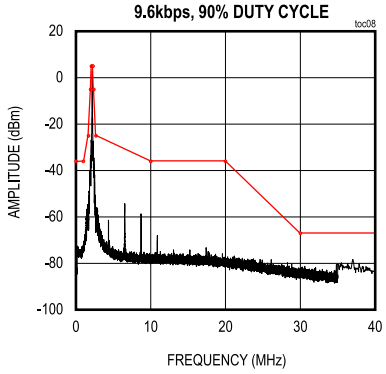
MIN/MAX TRANSMIT POWER vs. TEMPERATURE



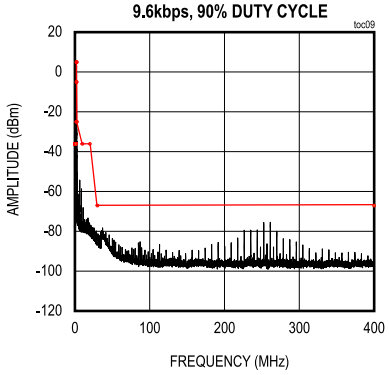
OUTPUT EMISSIONS vs FREQUENCY 9.6kbps, 90% DUTY CYCLE



OUTPUT EMISSIONS vs. FREQUENCY 9.6kbps, 90% DUTY CYCLE



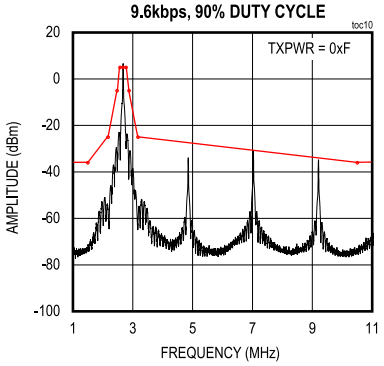
OUTPUT EMISSIONS vs. FREQUENCY 9.6kbps, 90% DUTY CYCLE



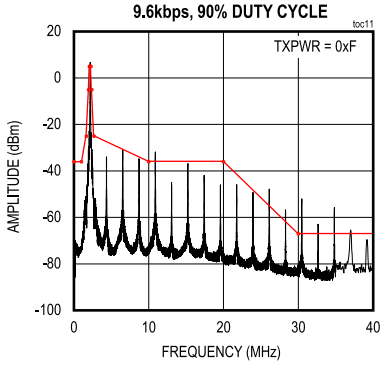
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_L = 3.3V, TXPWR = 0x7 (+3dBm), RXSENS = 0xB (-15dBm), DATARATE = 0x0 (9.6kbps), OSCBUF = 0.0, pullup on SYNCOUT with 1kΩ to V_L, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.)

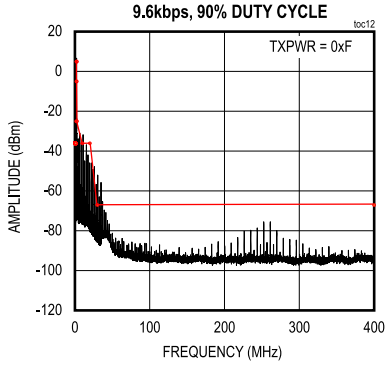
OUTPUT EMISSIONS vs. FREQUENCY
9.6kbps, 90% DUTY CYCLE



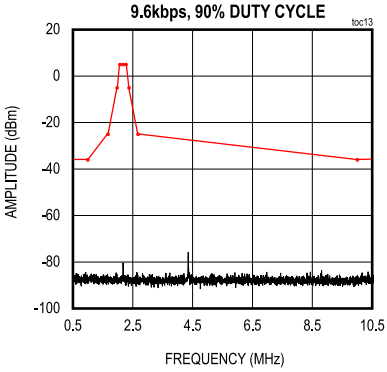
OUTPUT EMISSIONS vs. FREQUENCY
9.6kbps, 90% DUTY CYCLE



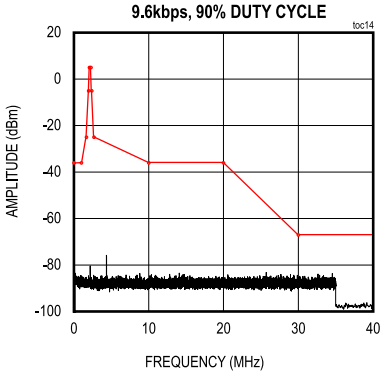
OUTPUT EMISSIONS vs. FREQUENCY
9.6kbps, 90% DUTY CYCLE



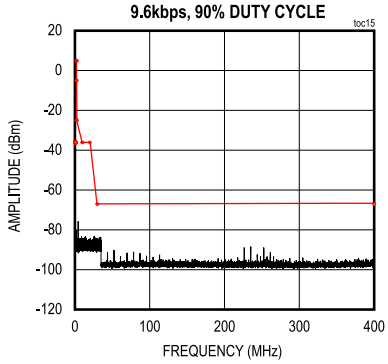
UNSELECTED PORT LEAKAGE
vs. FREQUENCY
9.6kbps, 90% DUTY CYCLE



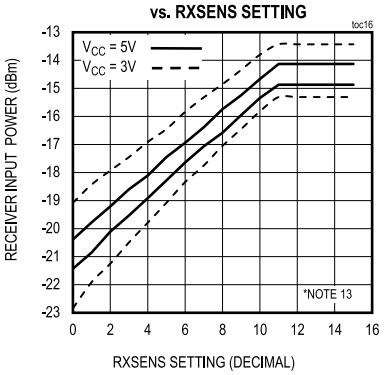
UNSELECTED PORT LEAKAGE
vs. FREQUENCY
9.6kbps, 90% DUTY CYCLE



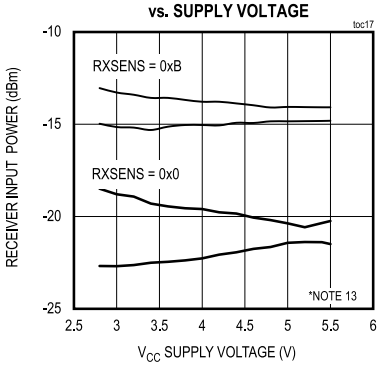
UNSELECTED PORT LEAKAGE
vs. FREQUENCY
9.6kbps, 90% DUTY CYCLE



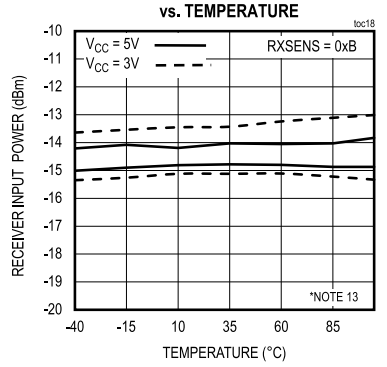
RECEIVER THRESHOLD WINDOW*
vs. RXSENS SETTING



RECEIVER THRESHOLD WINDOW*
vs. SUPPLY VOLTAGE



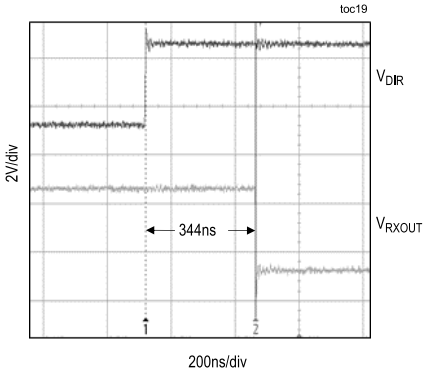
RECEIVER THRESHOLD WINDOW*
vs. TEMPERATURE



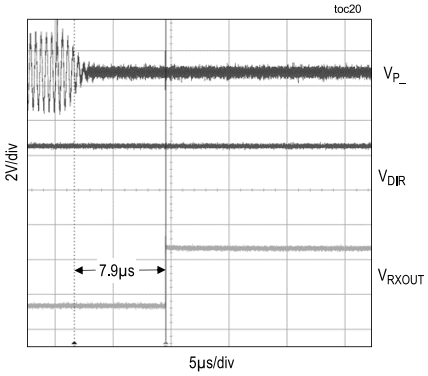
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_L = 3.3V, TXPWR = 0x7 (+3dBm), RXSENS = 0xB (-15dBm), DATARATE = 0x0 (9.6kbps), OSCBUF = 0.0, pullup on SYNCOUT with 1kΩ to V_L, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.)

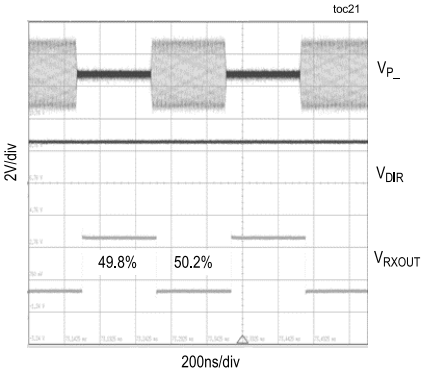
DIR TO RXOUT DELAY



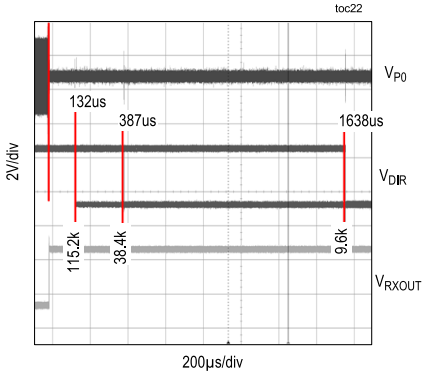
RECEIVER OUTPUT DELAY



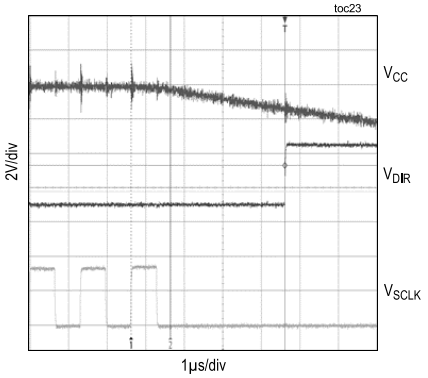
RECEIVER OUTPUT DUTY CYCLE



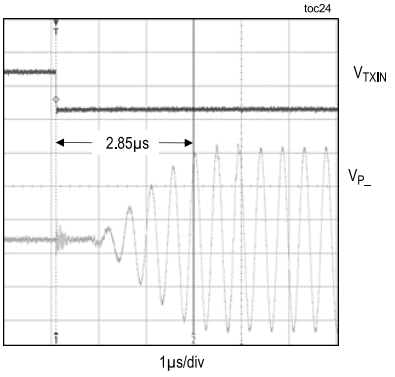
DIR DWELL TIME vs. BAUD RATE



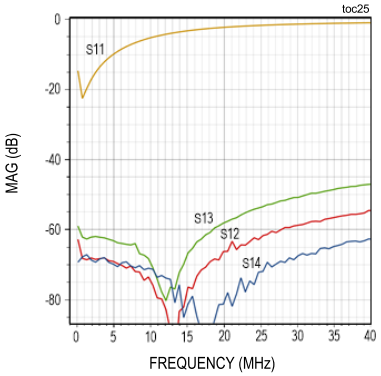
POWER-DOWN TO ACTIVE STATE DELAY



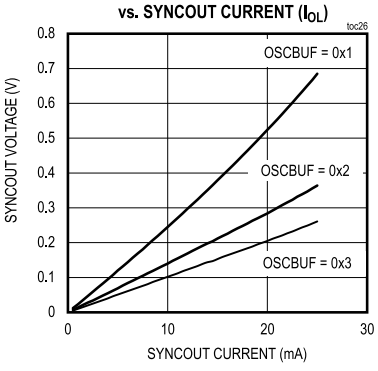
TRANSMIT DATA PROPAGATION DELAY



RF PORT SCATTER PARAMETERS

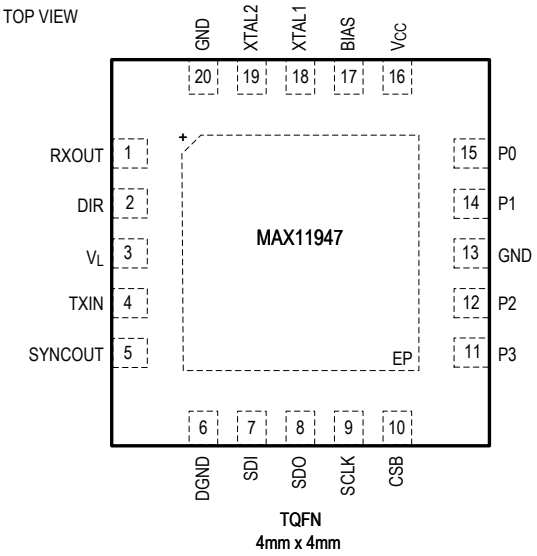


SYNCOUT VOLTAGE LOW (V_{OL}) vs. SYNCOUT CURRENT (I_{OL})



Pin Configuration

MAX11947



Pin Description

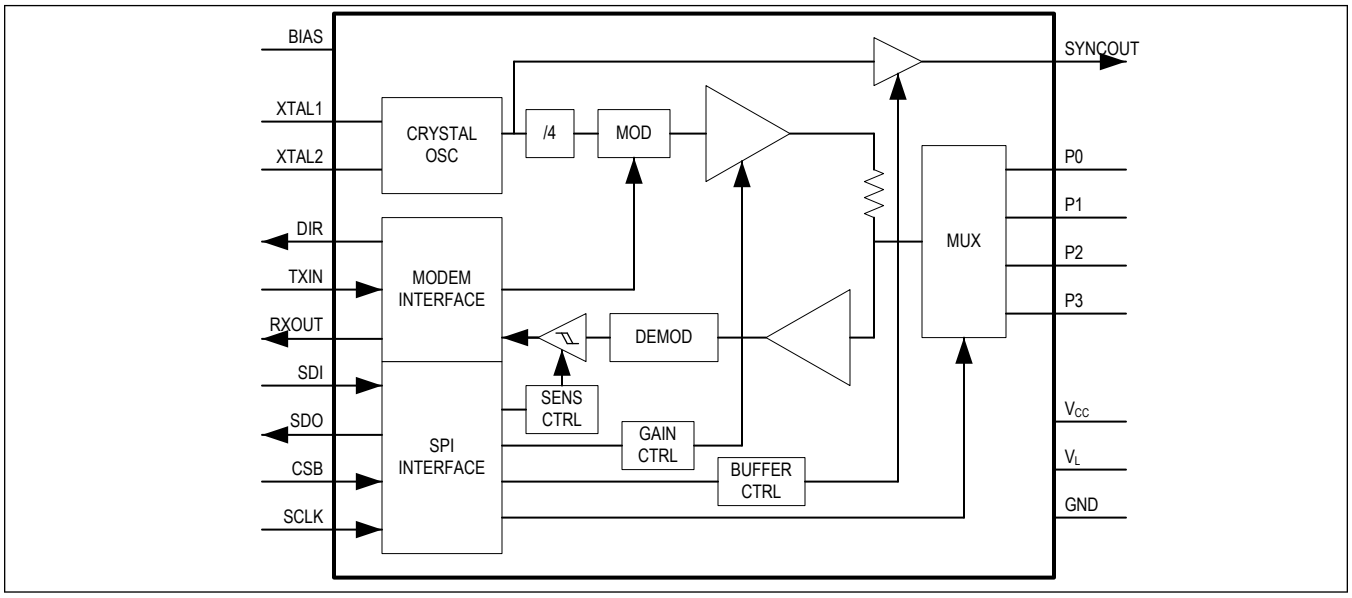
PIN	NAME	FUNCTION	REF SUPPLY
1	RXOUT	Modem Rx Digital Signal Output	V_L
2	DIR	Direction Output. DIR is asserted high when the data stream is seen at the receiver.	V_L
3	V_L	Logic Supply Voltage	
4	TXIN	Modem Tx Digital Signal Input	V_L
5	SYNCOUT	Sync Output. Open-drain output of the 8.704MHz clock to synchronize other devices.	Pullup
6	DGND	Ground	
7	SDI	SPI Bus Serial Data Input	V_L
8	SDO	SPI Bus Serial Data Output	V_L
9	SCLK	SPI Bus Serial Clock Input	V_L
10	CSB	Active-Low, SPI Bus Chip Enable	V_L
11	P3	RF MUX Port 3	V_{CC}
12	P2	RF MUX Port 2	V_{CC}
13	GND	Ground	
14	P1	RF MUX Port 1	V_{CC}
15	P0	RF MUX Port 0	V_{CC}
16	V_{CC}	Analog Supply Voltage	
17	BIAS	Output Bias Reference. Decouple BIAS with 1µF to GND.	VCC

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY
18	XTAL1	External Crystal Input Terminal. Feed with 8.704MHz (±30ppm) input clock for external synchronization.	V_{CC}
19	XTAL2	External Crystal Input Terminal. Connect to GND for external synchronization.	V_{CC}
—	EP	Exposed Pad. Must be left open or connected to GND.	

Functional Diagrams

Diagram 1



Detailed Description

The MAX11947 is an AISG v2.0 and v3.0-compliant, fully integrated modem with a 4:1 multiplexer facilitating connectivity between a single modem and up to four RF ports.

The MAX11947 receiver includes a narrow 200kHz bandwidth bandpass filter centered at the 2.176MHz carrier frequency. It also includes an OOK demodulator and a comparator that reconstructs the digital signal. The typical sensitivity threshold of the receiver is -15dBm (when set to the default value 0xB), in compliance with the AISG standard specifications. This threshold is adjustable through an internal register setting (RXSENS) from a -20.5dBm to -15dBm level.

The MAX11947 transmitter includes an OOK modulator, a bandpass filter that is compliant with the AISG spectral emission profile, and an output amplifier. The output power can be varied with an internal register setting (TXPWR) from under 0dBm to over +6dBm (measured at the MUX-selected RF port) to compensate for loss in the external circuitry and cabling. The OOK carrier is generated from an external crystal at 8.704MHz connected to the XTAL1 and XTAL2 pins. An external clock source at the same frequency can also be applied to XTAL1 from the SYNCOUT pin of another MAX11947.

The MAX11947 also features a DIR output to facilitate the RS-485 bus arbitration in tower-mounted equipment.

4:1 Multiplexer

The integrated 4:1 multiplexer allows the AISG system designer to connect a single modem to as many as four RF ports, simplifying implementation of a multi-primary or ALD PING-capable design. The MUX uses a CMOS analog switch architecture to provide a bidirectional signal, switchable between one common internal modem port and the four RF ports.

The 4:1 MUX provides both isolation and minimal crosstalk, allowing all four ports to be connected to a single modem without impacting the connected RF channels. To address the MUX performance, the port separation is characterized by three forms of isolation or crosstalk, which are primarily related to the frequencies involved: RF isolation, AISG isolation, and modem crosstalk.

Figure 2 shows a simplified block diagram of a single MUX RF port. A 50Ω series resistor is integrated into each RF port and the MUX common node is internally biased to approximately 1.5V DC.

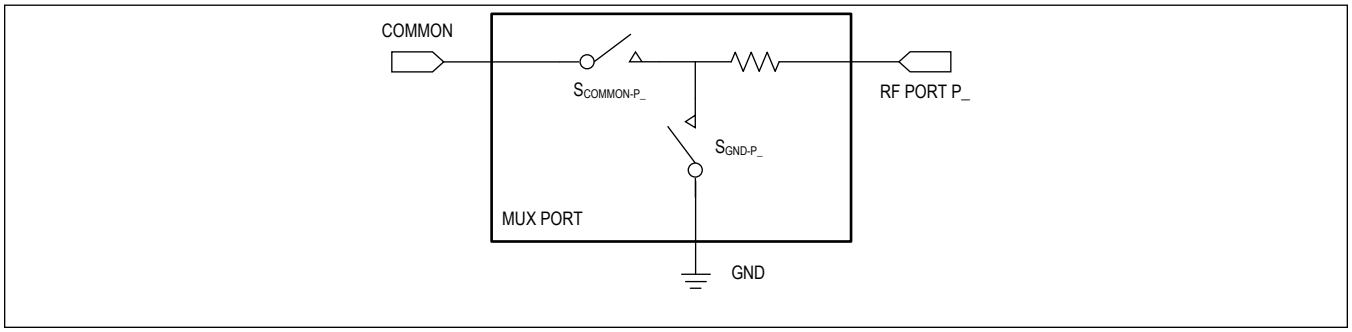


Figure 2. MUX Port Diagram

The 4:1 MUX can be configured to either have all of the P_ RF ports internally terminated and the common node not connected, or any single P_ RF port can be connected to the MUX common node. All switch changes occur in a break-before-make sequence. When an RF port is not connected to the MUX common node, that P_ port is internally terminated through the 50Ω resistor to ground. When a port is selected, any previous selected port is terminated to GND prior to the new port connection being made. The process of connecting a P_ RF port to the common port is measured by the t_{SW} time. This switching time is measured by monitoring the CSB and SCLK signals of the SPI interface and the DC level on the RF port. The time starts when the port change message is programmed into the RFPORT [1:0] bits in the MUX (0x1) register and is triggered by the 16th SCLK rising edge (last register bit is written). The switch time ends when a 1.5V DC bias level is measured on the selected RF port. It should be noted that this timing can vary due to delays with transitioning

between the SPI clock domain and the internal operational clock domain. Figure 3 shows how the MUX switch time is measured from the 16th SCLK transition to the measured 1.5V DC bias on the RF port (t_{SW}), to the DIR output transition (t_{SW-DIR}), and to the first RXOUT bit (t_{SW-RX}).

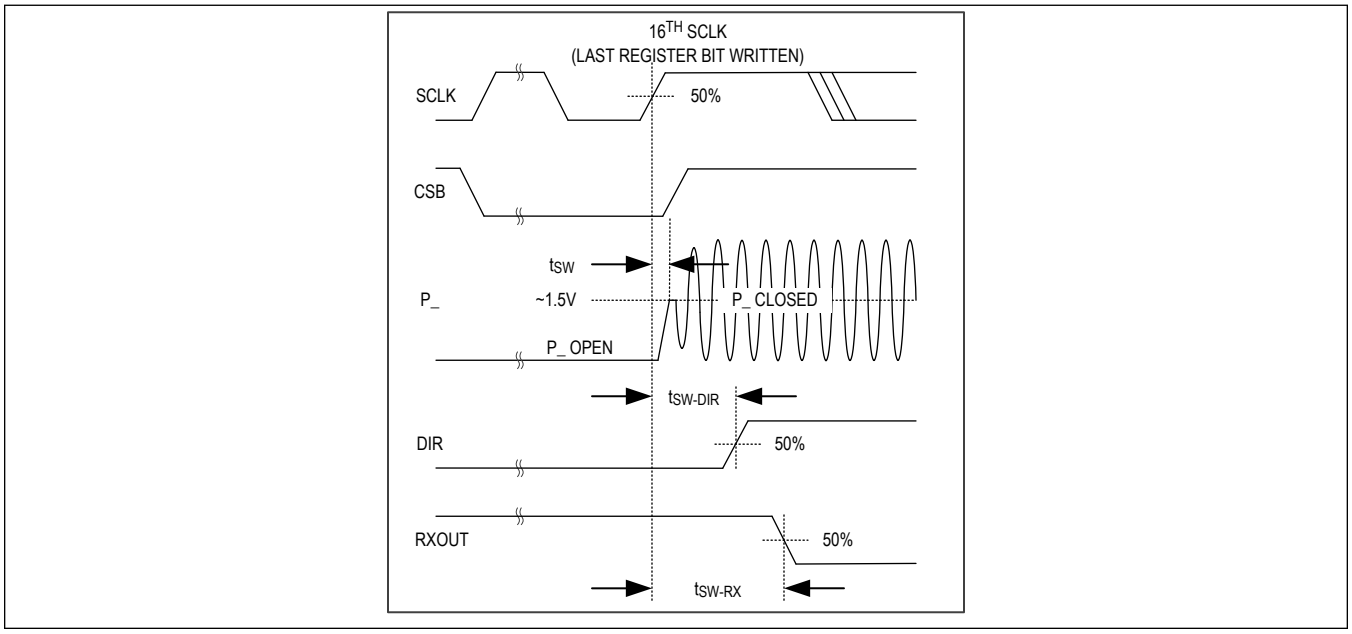


Figure 3. Switch Timing

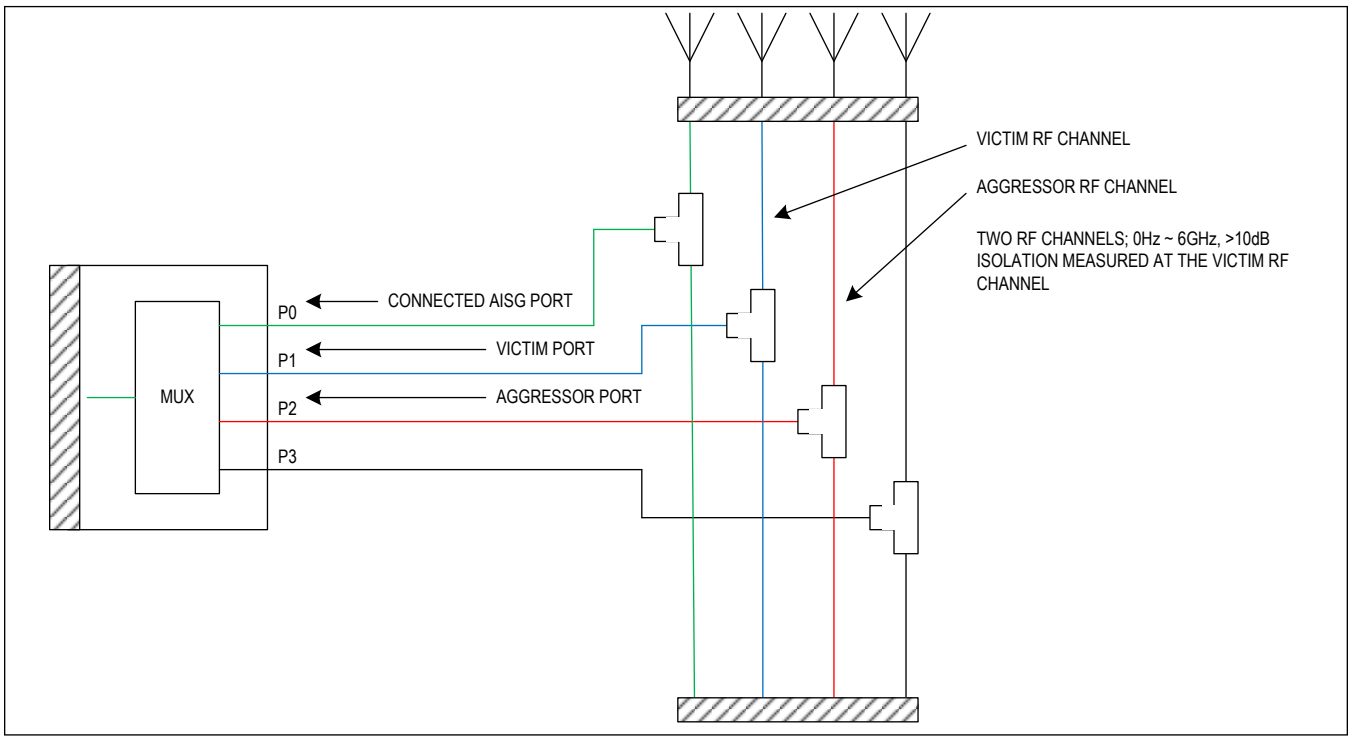


Figure 4. RF Isolation

RF Isolation

The first form of separation to address is radio frequency signal isolation between RF ports. The primary implementation of the MAX11947 in a cellular tower application would have multiple RF frequencies in the cellular bands connected to separate ports on the 4:1 MUX. RF isolation describes how much of a high-frequency (cellular) signal on one RF port is detectable on another RF port. In Figure 4, an aggressor signal is applied to the coax cable tap of the P2 channel and the coax cable tap of P1 is measured for any impact on the victim channel. A majority of this isolation is provided by the lowpass filters on the P2 and P1 connections (LPF2 and LPF1, respectively).

AISG Isolation

The next form of separation to address is AISG carrier signal isolation between RF ports. Implementation of AISG v3.0 allows for the possibility of each RF port to carry either a multi-primary AISG signal or a PING signal. AISG isolation describes how much a 2.176MHz carrier signal on one RF port is detectable on another RF port. In Figure 5, an aggressor AISG signal is applied to the coax cable tap of the P2 channel and the coax cable tap of P1 is measured for any impact on the victim channel. A majority of this isolation is provided by 4:1 MUX switch within the MAX11947.

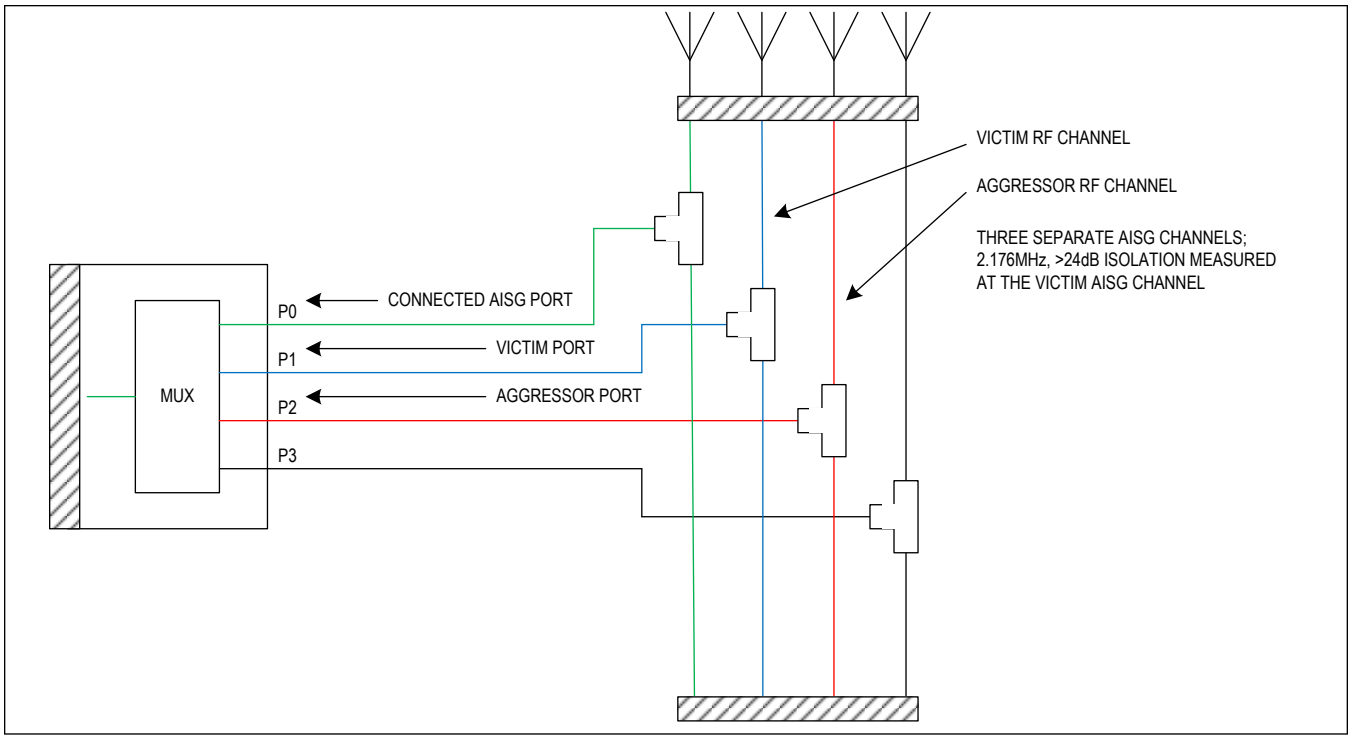


Figure 5. AISG Isolation

Modem Crosstalk

The last form of separation to address is modem crosstalk between RF ports. Again, implementation of AISG v3.0 allows for the possibility of each RF port to carry either a multi-primary AISG signal or a PING signal. Modem crosstalk describes how much a modulated AISG signal on a nonselected RF port is detectable by the MAX11947's internal receiver while connected to a different, selected RF port. In Figure 6, an aggressor AISG signal is applied to the coax cable tap of the P1 channel and the 4:1 MUX is connected to the P0 RF port. The aggressor signal is set to the maximum allowed power of +5dBm and the receiver threshold is set to the minimum programmed level of 0x0 (about -20.5dBm) and is monitored for any indication of a detected signal on the DIR or RXOUT pins. A majority of this isolation is provided by 4:1 MUX switch within the MAX11947.

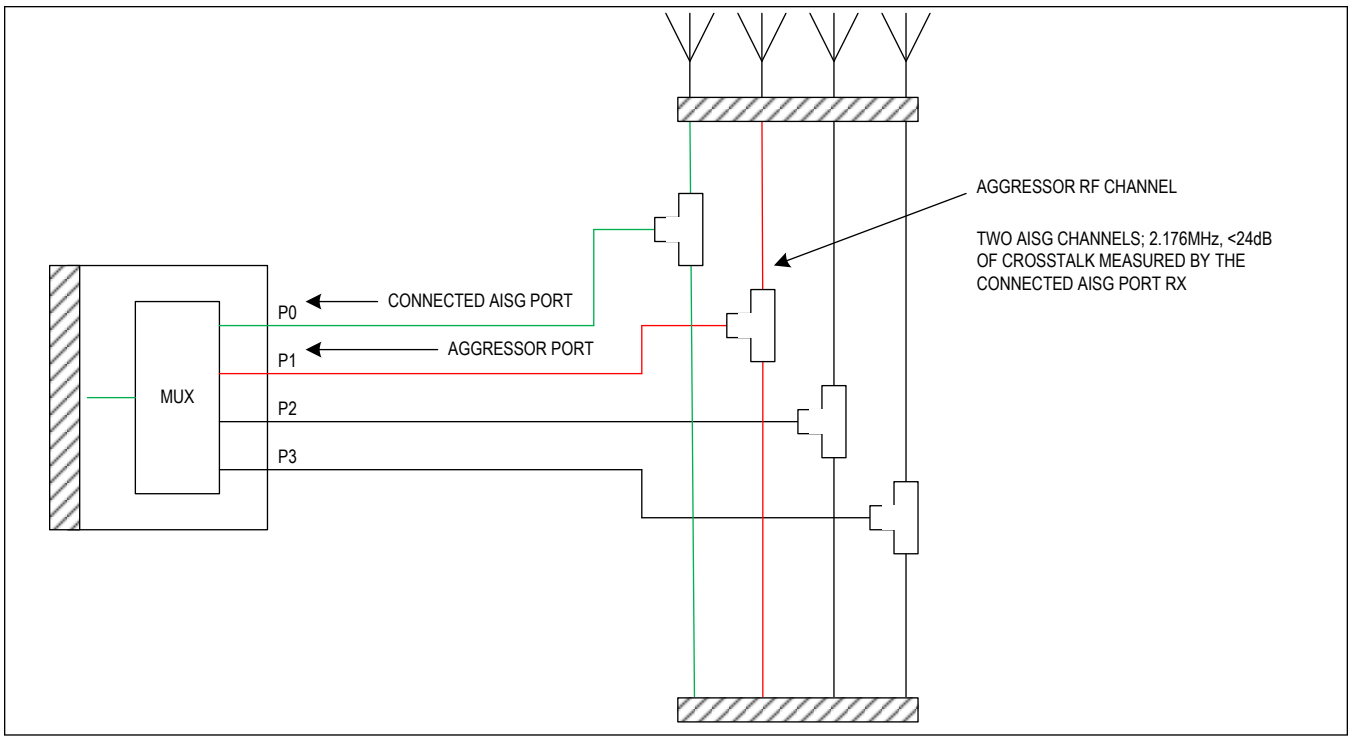


Figure 6. Modem Crosstalk

Register Programming

The multiplexer is programmed through two register settings. In the MUX register (address 0x01), the OPEN bit internally disconnects the modem from the common port of the MUX, and the default condition (0x0) connects. In the same MUX register, the two RFPORT bits are used to select which external RF port the common port is connected to.

Table 1. RFPORT Register Settings

RFPORT VALUE	COMMON CONNECTION
0x0	Connected to port P0
0x1	Connected to port P1
0x2	Connected to port P2
0x3	Connected to port P3

Internal Termination

The MAX11947 modem works in conjunction with a 4:1 multiplexer and an internal 50Ω termination. The termination is connected serially between the internal PA and the common MUX port. This resistor acts as series source for the transmit path (data flowing from TXIN to the selected RF port) and acts as parallel termination when data is being received on the internal receive path. The output of the transmitter is biased at 1.5V to maximize the power-supply rejection ratio and minimize any spurious emissions. It is recommended that the device be AC-coupled to the feeder cable through either an external RF filter or a series 100nF capacitor.

Receiver

The modem receiver consists of an LNA, a demodulator, and a sensitivity threshold adjustment system to convert the 2.176MHz OOK modulated signal into a digital output at RXOUT.

The maximum OOK input power at the internal LNA into the 50Ω internal termination is +5dBm. For a single-tone signal

at 2.176MHz, +5dBm corresponds to 1.12V_{P-P}.

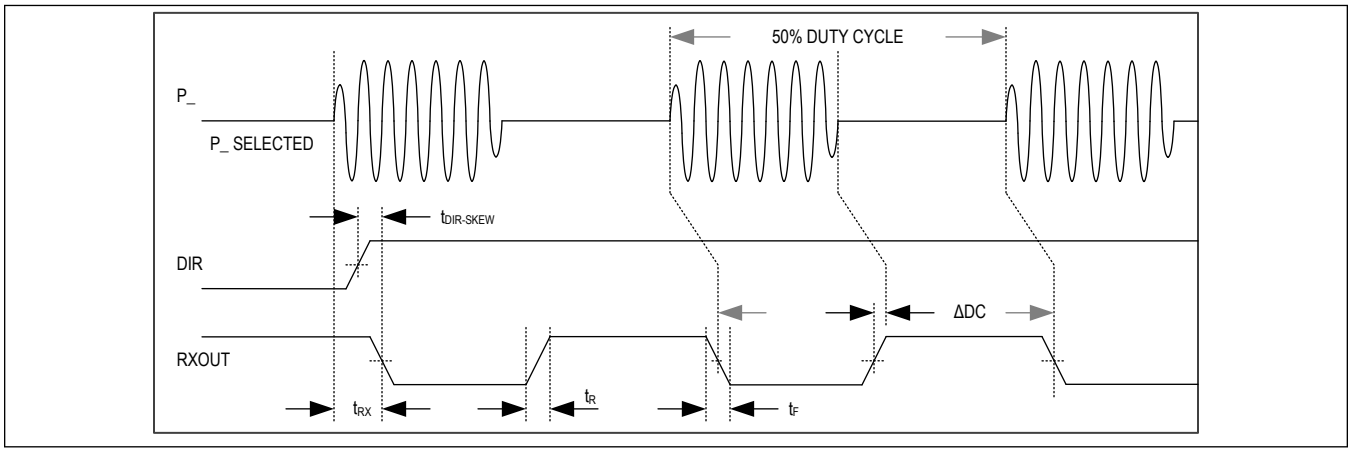


Figure 7. Receiver Timing

Input Range and Sensitivity Threshold Control

The MAX11947 internal threshold is set to -15dBm (112.5mV_{P-P}) by default (RXSENS set to 0xB). This centers the receive sensitivity threshold in the -12dBm to -18dBm undefined window specified by the AISG standard. This threshold sets the minimum input signal power recognized as an OOK ON carrier (asserting DIR level, logic-high and setting the RXOUT bit, logic-low).

Consider a corner case where the OOK signal at 2.176MHz present at the selected RF port, is at the minimum power of -15dBm ±3dB. To avoid saturation of the receiver input stage, any other adjacent carrier with power up-to +5dBm must be at a frequency below 1.25MHz or above 3.7MHz.

Referencing section 10.3.13 of the AISG v3.0 specification, ALD system designers are permitted to include splitters and/or combiners with an insertion loss of 4.5dB for a two-way split or as much as 6.3dB for a three-way split. With an outgoing transmission the MAX11947's adjustable transmitter power allows the designer to increase the modem output up to over +6dBm, which would result in an effective level of +1.7dBm or more after a two-way split (falling within the +3dBm ±2dB window). Similarly, an incoming transmission with a maximum signal power of +5dBm would have no issues being decoded at the modem receiver. However, the potentially minimum receive power of -12dBm may not be properly decoded after the 4.5dB splitter attenuation. The adjustable threshold of the MAX11947 allows the AISG designer to move the target from -15dBm to as low as -20.5dBm, effectively allowing a drop of 5.5dB which can accommodate the 4.5dB attenuation from a two-way splitter. See the *In-Line Attenuation* section for additional information.

The MAX11947 receiver sensitivity threshold can be varied with an internal register setting (RXSENS) from a default level of -15dBm down to -20.5dBm in about 0.5dB steps. To obtain the nominal sensitivity threshold of -15dBm at the RF port as the AISG standard requires, set RXSENS to 0xB (default value). For additional setting values and their equivalent threshold, see the *RXTX* register details.

Transmitter

The modem transmitter consists of a local oscillator (LO) circuit, an on-off-keyed (OOK) modulator, and an adjustable power amplifier (PA).

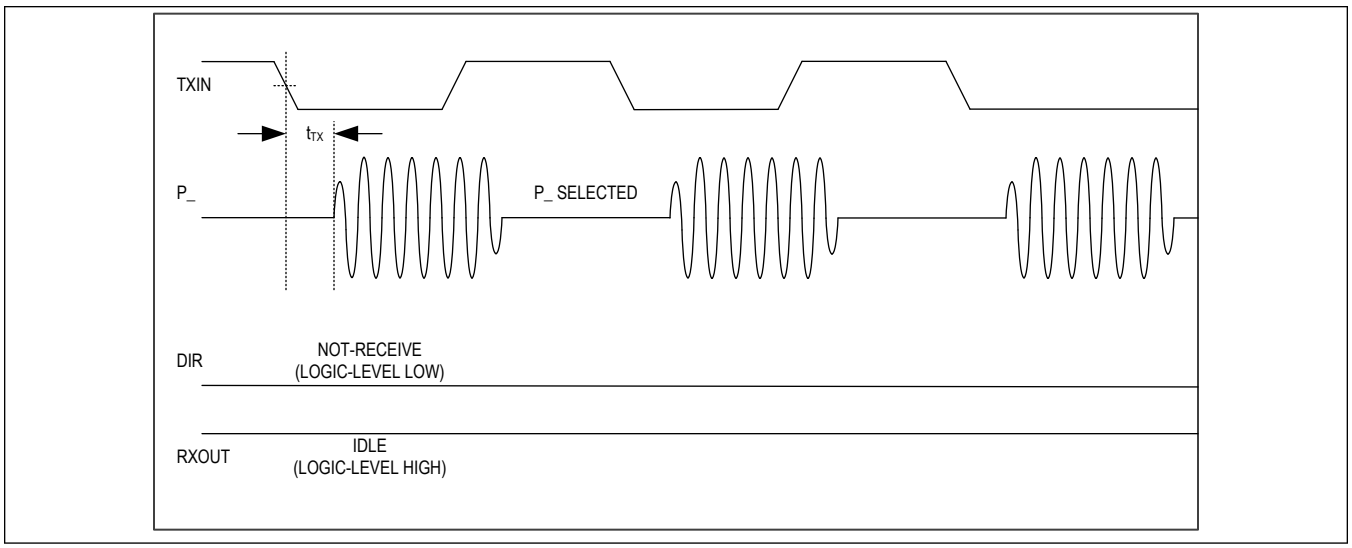


Figure 8. Transmitter Timing

Output Power Control

The MAX11947 output power can be varied with an internal register setting (TXPWR) from < 0dBm to over +6dBm (measured at the MUX selected RF port: P0, P1, P2, or P3) to compensate for loss in the external circuitry and cabling. The maximum voltage available at the MUX selected RF port is about $1.29V_{P-P}$. Assuming that the feeder cable is terminated into a 50Ω impedance, the external filter is lossless at 2.176MHz, where a series 50Ω termination is being used internally, the output level of $1.29V_{P-P}$ corresponds to +6.2dBm at the feeder cable. See the *External Low-Pass Filter and AC-Coupling to Feeder Cable* section for more details.

The P_ voltage level can be varied according to the following equation:

P_{OUT} (at P_ in dBm) = TXPWR (decimal) x 0.5 (dB) - 0.5dBm

The output power has a soft ceiling around +6.0dBm at code 0x0D and rolls off the 0.5dB per code rate with the last two settings of 0x0E and 0x0F. The maximum PA output power is governed by the V_{CC} supply and when using 5.0V the MAX11947 can likely achieve transmitter output power levels up to +7.0dBm.

To obtain the nominal power level of +3dBm at the feeder cable as the AISG standard requires, set TXPWR to 0x7 (default value), which provides about $0.89V_{P-P}$ at the MUX selected RF port P_.

Carrier Tone

For a diagnostic tool, the transmitter can be held in a constant transmit mode by setting an internal register bit. By setting the TX_ON bit to a 1 value in the CFG (0x00) register, the transmitter sends a 2.176MHz carrier without a need to send a data stream through the TXIN pin. This bit is used for various production test and can be used on an AISG system to generate a carrier tone on the RF port selected with the MUX.

Direction Output

The MAX11947 provides a direction output pin (DIR) that indicates the direction of the data flow. This feature is very useful in the tower that acts as a slave in the AISG protocol. In most applications the base is the master and it controls the flow of data by performing bus arbitration. The output DIR allows the equipment in the tower to avoid any involvement in the bus arbitration. The *Typical Application Circuit* shows how the MAX11947 can be used in the tower in conjunction with the RS-485 transceiver such as the MAX13485E or MAX13486E.

Typically, the DIR output drives the DE (driver output enable) and RE_ (receiver output enable) of the RS-485 transceiver.

Whenever the data flows from the selected RF port (P0, P1, P2, or P3) to RXOUT, the DIR output is asserted high. When the MAX11947 is located in the tower, the data flow is being sent from the base (master) to the tower (slave). On the

other side, when the data flows in the opposite direction, from TXIN to the selected RF port, the DIR output is deasserted low. However, the MAX11947 internal state machine is sensing both the TXIN and the status of the internal LNA, it can recognize the correct flow of data and avoid asserting the DIR high.

Figure 9 and Figure 10 show the timing diagrams of the DIR functionality. When the data flows from the selected RF port to RXOUT, DIR remains high for 16 bit times after the last logic-level low bit within the 8-bit protocol data (DIR dwell time). This is compliant with the AISG specification saying that the RS-485 transmitter stops driving the bus within 20 bit-times after the last stop bit is sent.

The DATARATE register value defines the duration of the bit time, as shown in Table 2.

Table 2. DATARATE Register Settings

DATARATE VALUE	DATA RATE (kbps)	BIT TIME (µs)	DIR DWELL TIME (ms)
0x0 (default)	9.6	104.16	1.667
0x1	38.4	26.04	0.416
0x2	115.2	8.68	0.139
0x3	N/A	N/A	N/A

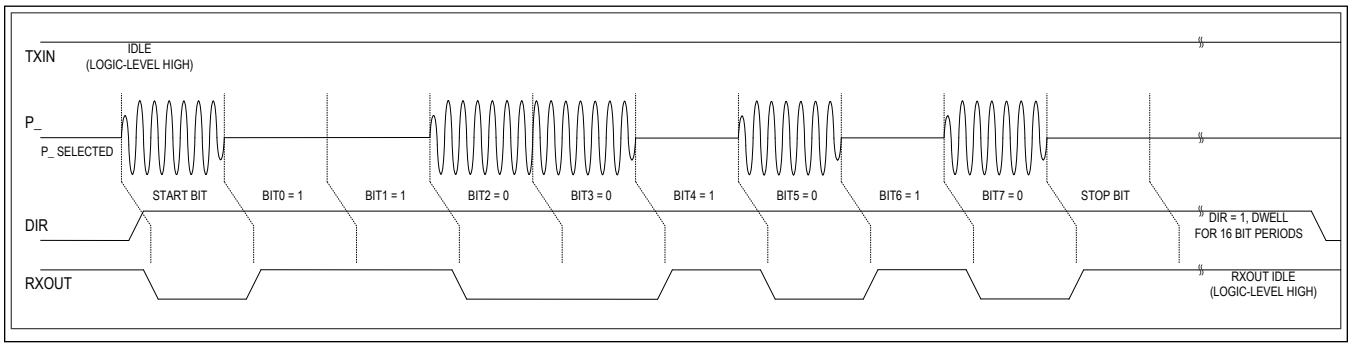


Figure 9. Receiver Communication Flow

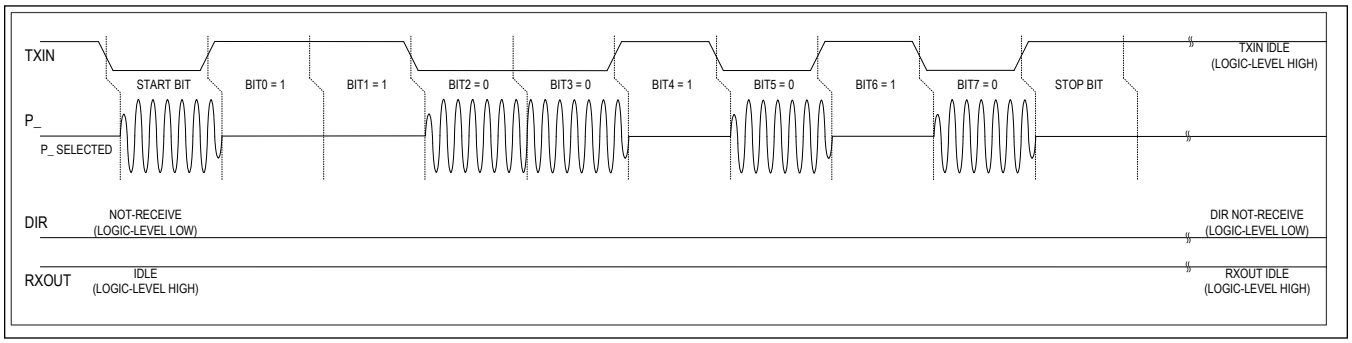


Figure 10. Transmitter Communication Flow

Serial Peripheral Interface (SPI)

The MAX11947 utilizes a 4-wire SPI protocol for programming its registers, configuring and controlling the operation of the modem. The register contents can be read back through the SDO pin. The digital I/Os in Table 3.

control the operation of the SPI.

Table 3. SPI Pins

PIN	DIRECTION	DESCRIPTION
SCLK	Input	Serial Clock
SDI	Input	Serial Data Input (MOSI)
CSB	Input	Chip-Select Bar
SDO	Output	Serial Data Output (MISO)

Figure 11 shows a general SPI write transaction. Figure 12 show the format of a SPI read transaction. As shown in the diagrams, the R/W bit is set to 0 for a write transaction and the R/W bit is set to 1 for a read transaction.

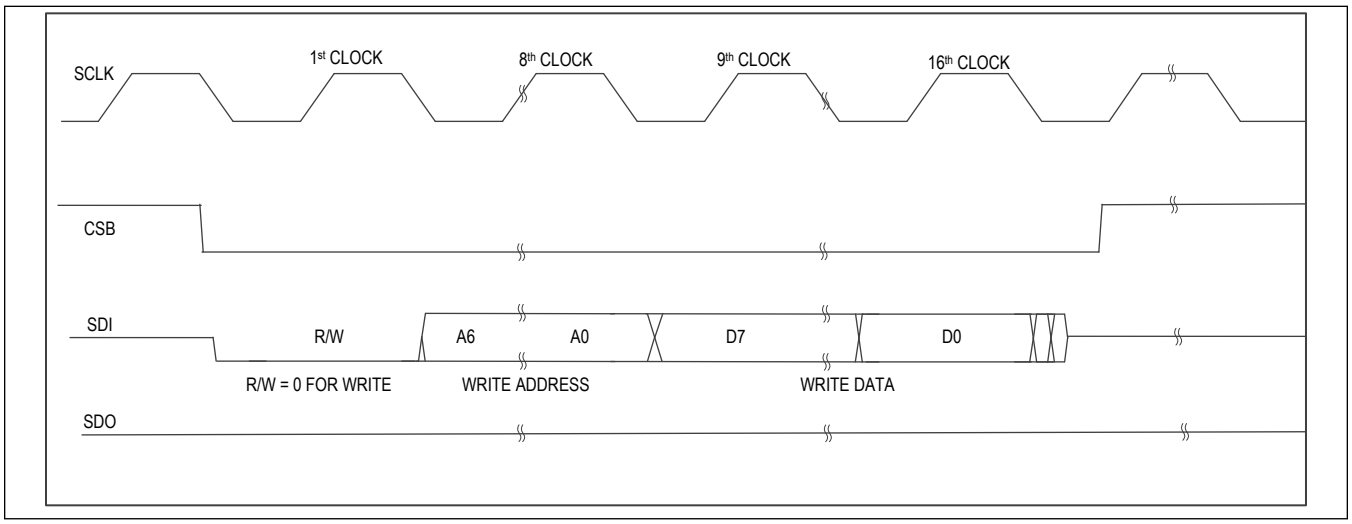


Figure 11. SPI Write Transaction

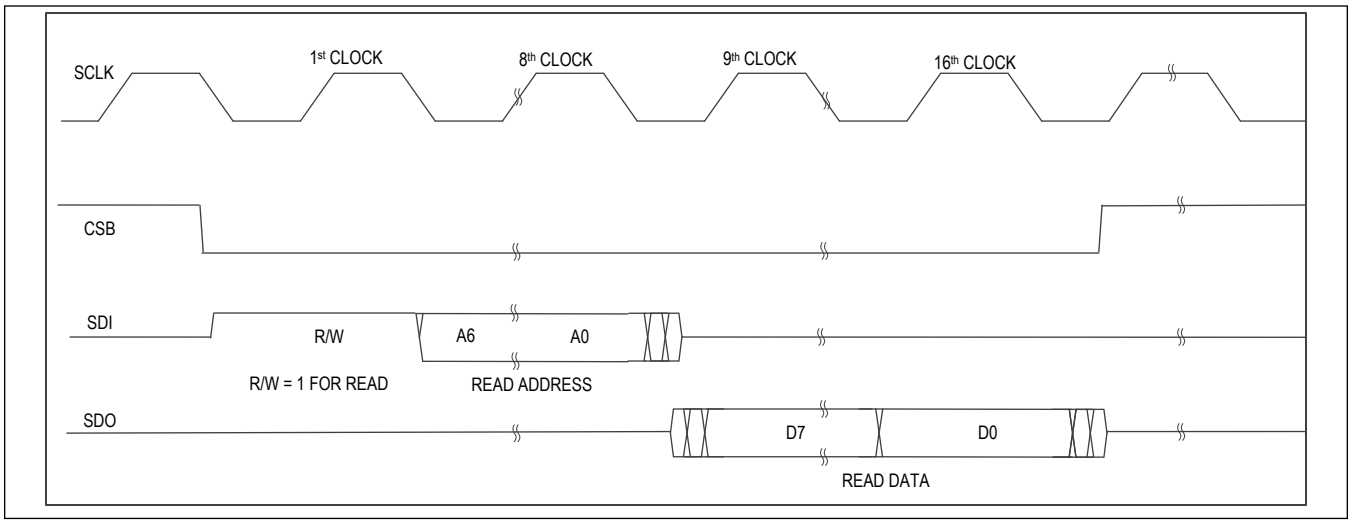


Figure 12. SPI Read Transaction

Standby and Power-Down

Operational Modes

The MAX11947 has three modes of operation that include two power-saving modes. Each power-saving mode shuts

down various internal blocks to save on current and reduce the overall power consumption of the modem. The SPI interface always remains operational, and the internal register values are always retained as long as the V_{CC} and V_L supplies remain within specified voltage limits.

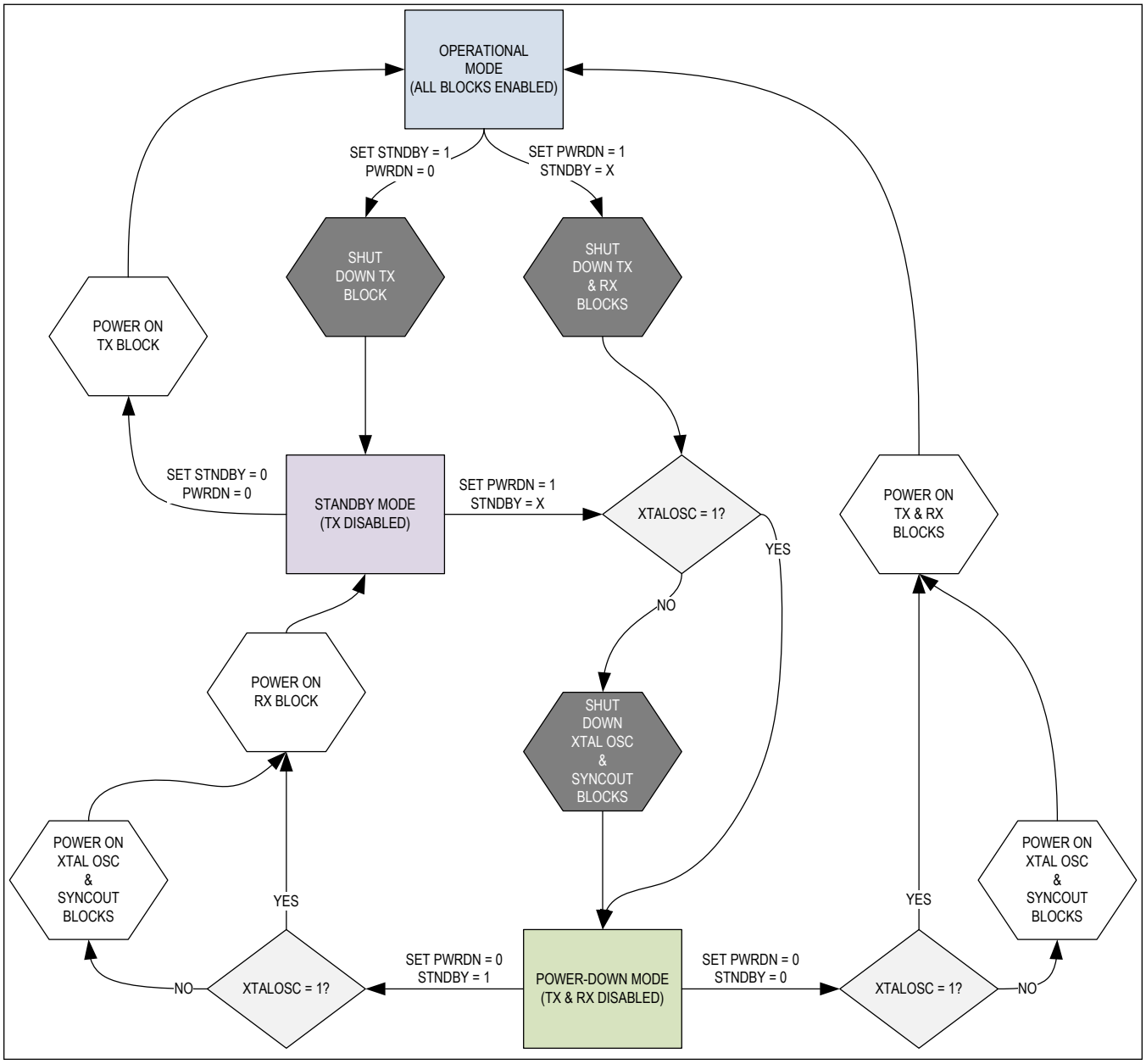


Figure 13. Power Modes

Standby Mode

Setting the STANDBY bit in the CFG (0x00) register places the modem in standby mode. This configuration shuts down the transmitter signal chain including the TXIN interface, the modulator, the power amplifier, and all associated filtering blocks. While in the STANDBY state, the modem consumes less power and thus has a lower supply current. All other modem functions, including the receiver signal chain (RXOUT) and the DIR signal, continue to operate normally.

Power-Down Mode

Setting the PWRDN bit in the CFG (0x00) register places the MAX11947 modem into power-down mode. This configuration shuts down the transmitter signal chain as well as the receiver signal chain including the LNA, the demodulator, the RXOUT interface, and the DIR system.

Depending on the state of the XTALOSC bit in the CFG (0x00) register, the power-down mode maintains the crystal oscillator and SYNCOUT operation or shuts down those blocks as well. By default, the XTALOSC bit is set to 1 and the 8.704MHz system remains operational for cascaded master/slave clocking. See the *Crystal and External Clock* section. If the XTALOSC bit is set to 0 prior to or during the same write command as the PWRDN bit, the crystal oscillator and SYNCOUT blocks are also shut down while in power-down mode.

While in the PWRDN state, the modem consumes minimal power yet still retains values programmed in the registers and keeps the SPI interface operational for further programming and mode selection.

Port Scanning

The SCAN (0x02) register bits are used to configure the port scanning feature of the MAX11947. This state machine allows the modem to automatically listen for a carrier tone and/or the ping message on any of the RF ports sequentially. By setting the MASK_Px bits to 1 or 0, the individual RF ports can be included or excluded from the scan sequence, respectively. The default port scan process includes all RF ports (PINGCFG = 0x0F by default).

The automatic scanning process is initiated by setting the START_SCAN bit to 1; this is a self-clearing bit and reverts back to a 0 if the register is read back. While the modem is actively scanning the RF ports, the SCANNING bit asserts (1) and the LSTN_PORT bits indicate which port is connected to the modem through the 4:1 MUX.

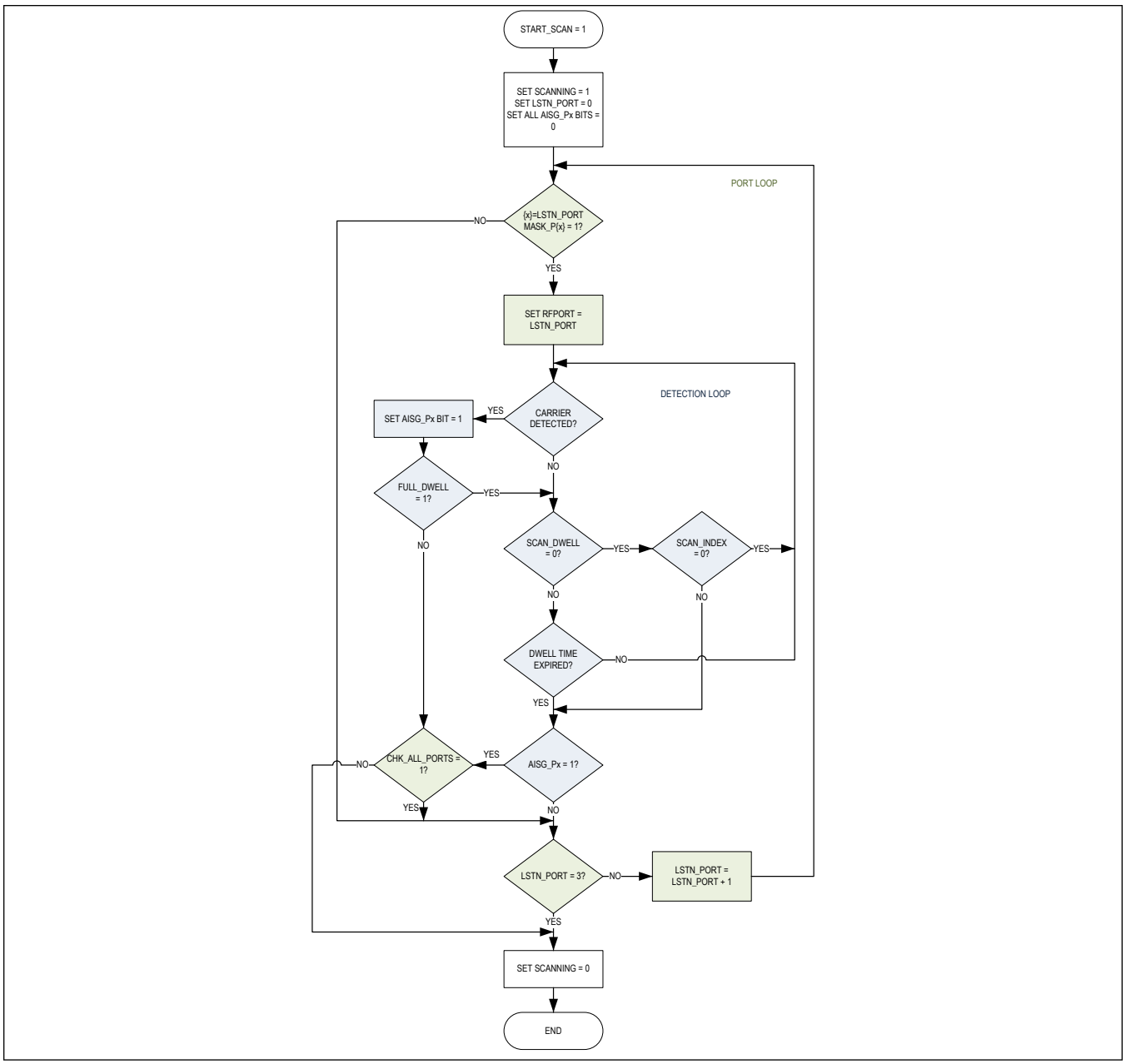


Figure 14. Port Scan Flow Chart

The port scanning dwell time is either a manually controlled delay or is based on a combination of the SCAN_DWELL setting and the programmed DATARATE setting described in the *Direction Output* section. This dwell time defines how long the receiver listens to each RF port in order to detect a 2.176MHz carrier signal.

Table 4. SCAN_DWELL Time

SCAN_DWELL		DWELL TIME		
VALUE	BIT PERIOD MULTIPLIER	DATA RATE = 0x0/9.6kbps	DATA RATE = 0x1/38.4kbps*	DATA RATE = 0x2/115.2kbps*

Table 4. SCAN_DWELL Time (continued)

0x0	NA	Manual mode: Sequenced by SCAN_INDEX Bit		
0x1	1x	0.104ms	0.026ms	0.009ms
0x2	16x (Same as DIR Dwell)	1.667ms	0.416ms	0.139ms
0x3	User programmed	Based on upper-nibble of PORTCFG (0x04) register and the DWELL_MULT (0x05) register		

**Nonstandard setting for AISG v3.0*

When SCAN_DWELL is set to 0x0, the dwell time is controlled by the user and does not increment to the next RF port until the SCAN_INDEX bit is set to 1 or a carrier signal is detected and FULL_DWELL is set to 0. This mode gives the user external, asynchronous control of the port scanning dwell time. When SCAN_DWELL is set to a value of 0x1 or 0x2, the scan dwell time is based on a fixed number of bit periods (1 or 16) based a combination of the SCAN_DWELL multiplier and the programmed data rate of the modem. When SCAN_DWELL is set to 0x3, a user-defined bit period multiplier between 1x to 4096x is used. The user defined DWELL multiplier is a 12-bit value spread across the PINGCFG (0x04) and DWELL_MULT (0x05) registers with the upper-nibble (bits 11:8) being programmed into the PINGCFG register and the remaining eight bits of the DWELL multiplier being programmed into the DWELL_MULT register.

Table 5. User-Programmed Dwell Time

PARAMETER	DWELL VALUE		
REGISTER / BITS	BITS [11:8]	BITS [7:4]	BITS [3:0]
PINGCFG (0x04)	[7:4]	—	—
DWELL_MULT (0x05)	—	[7:4]	[3:0]

The DATARATE value should be set prior to initiating the scan. See Table 4 and Table 5 for the available port scanning dwell times.

The port scanning engine indexes to the next port under three conditions:

- After the dwell time has expired.
- The SCAN_INDEX bit has been asserted by the user (in manual mode, SCAN_DWELL = 0x0).
- An AISG carrier signal has been detected, FULL_DWELL = 0, and the CHK_ALL_PORTS = 1.

After one of the above conditions are met, the next unmasked RF port is selected and programmed into the MUX.

Each port is scanned in sequence from P0, to P1, P2, and P3 based on the mask selection. If the matching MASK_Px bit is set to 1 then that RF port Px is included in the scan sequence. If the MASK_Px bit is cleared 0, then that RF port will not be included in the sequence.

Once all the unmasked ports have been scanned, the SCANNING bit is set to 0 and the port scanning process is complete.

The port scanning process uses the sensitivity threshold programmed into the RXSENS bits of the RXTX (0x03) register. A signal is reported as a valid detection when the power level exceeds the programmed sensitivity threshold (i.e., the DIR pin indicates an AISG signal). See Input Range and Sensitivity Threshold Control in the *Receiver* section for more information. The RXSENS threshold should be set prior to initiating the scan.

When a carrier signal is detected, the port scanning engine continues to listen to that RF port if the FULL_DWELL bit is set to 1. This allows the user to decode a full message received at that port. The Rx channel remains active during port scanning thus the RXOUT pin indicates the received signal as in normal operation. For example, the AISG v3.0 ping packet is expected to have a length of 82 bits, assuming the DWELL time is set to 82x the bit period, the port scan routine remains on the selected RF port for the full time needed to decode such a ping message. See the *Dwell Time* section for for more information.

Results from the automatic port scanning are reported in the PORTSTAT (0x06) register. When an AISG carrier was detected during the scan, each port with a detected signal is marked with a 1 bit in the appropriate location (AISG_Px bit). If no carrier was detected during the dwell time on that port or by the time the SCAN_INDEX bit was asserted, the appropriate PORTSTAT bit has a 0 value.

The AISG_Px bits are only cleared when initiating a new scan. Results from previous scans are held and can be read from the PORTSTAT (0x06) register up until a new scan is started by setting the START_SCAN bit to 1.

Status Bits

The STATUS register (0x07) can be used to determine the state of various internal modem blocks. This read-only register indicates the status of the internal TXACTIVE signal, the RXOUT signal, and the DIR signal through the SPI interface rather than having to sense the three modem pins themselves.

The status of the PA can be determined by reading the TXACTIVE bit in the STATUS register. This bit provides the transmission status of the PA rather than the same logic value of the TXIN pin--effectively inverted from the pin logic.That is, when the TXIN pin is driven to a logic-low or 0 value OR the TX_ON bit of the CFG (0x00) register is set to 1, the transmitter generates a 2.176MHz carrier on the connected RF port and the TXACTIVE bit reads back as a 1.

The DIR bit [1] of the STATUS register provides a duplicate value of the DIR pin. That is, when the DIR pin is being driven to a logic-high or 1 value by the modem, indicating the receiver has detected a 2.176MHz carrier on the connected RF port, the DIR bit reads back as a 1.

The RXOUT bit [0] of the STATUS register also provides a duplicate value of the RXOUT pin. For example, when the receiver is detecting a 2.176MHz carrier on the connected RF port, the RXOUT pin is driven to a logic-low or 0 value by the modem and the RXOUT bit is also read back as a 0.

Register Map

Register Map

ADDRESS	NAME	MSB							LSB
AISG									
0x00	CFG[7:0]	XTALOSC	PWRDN	STANDBY	TX_ON	OSCBUF[1:0]		DATARATE[1:0]	
0x01	MUX[7:0]	–	–	–	–	–	OPEN	RFPORT[1:0]	
0x02	SCAN[7:0]	CHK_ALL_PORTS	FULL_DWELL	SCAN_DWELL[1:0]		–	–	SCAN_INDEX	START_SCAN
0x03	RXTX[7:0]	RXSENS[3:0]				TXPWR[3:0]			
0x04	PINGCFG[7:0]	DWELL[11:8]				MASK_P3	MASK_P2	MASK_P1	MASK_P0
0x05	DWELL_MULT[7:0]	DWELL[7:0]							
0x06	PORTSTAT[7:0]	–	LSTN_PORT[1:0]		SCANNING	AISG_P3	AISG_P2	AISG_P1	AISG_P0
0x07	STATUS[7:0]	–	–	–	–	–	TXACTIVE	RXOUT	DIR
0x08	ID1[7:0]	PARTNUM[7:0]							
0x09	ID2[7:0]	REVNUM[7:0]							

Register Details

CFG (0x0)

BIT	7	6	5	4	3	2	1	0
Field	XTALOSC	PWRDN	STANDBY	TX_ON	OSCBUF[1:0]		DATARATE[1:0]	
Reset	0x1	0x0	0x0	0x0	0x01		0x00	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
XTALOSC	7		0x0: Crystal oscillator shuts down in power-down mode 0x1: Crystal oscillator and SYNCOUT remain on when in power-down mode
PWRDN	6		0x0: Normal operating mode 0x1: PLL, Rx, and Tx are powered down, register content is retained, SPI available
STANDBY	5		0x0: Normal operating mode 0x1: Tx circuit is powered down, PLL on, register content is retained, SPI available
TX_ON	4		0x0: Normal Tx operation w/ internal TXOUT signal = TXIN pin input 0x1: TXOUT signal always on

BITFIELD	BITS	DESCRIPTION	DECODE
OSCBUF	3:2		0x0: SYNCOUT is disabled 0x1: Normal buffer setting for SYNCOUT clock-Level 1 0x2: Increased bias for additional buffer current drive on the SYNCOUT clock-Level 2 0x3: Increased bias for additional buffer current drive on the SYNCOUT clock-Level 3
DATARATE	1:0	XO clock division ratio for digital block	0x0: 9.6kbps data rate (default) 0x1: 38.4kbps data rate 0x2: 115.2kbps data rate 0x3: Not used

MUX (0x1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	OPEN	RFPORT[1:0]	
Reset	–	–	–	–	–	0x0	0x00	
Access Type	–	–	–	–	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
OPEN	2		0x0: The modem (transmitter and receiver) is connected to the common MUX port that is connected to the selected RF port 0x1: The modem is not connected to any RF port
RFPORT	1:0		0x0: MUX common port connnected to RF port P0 0x1: MUX common port connnected to RF port P1 0x2: MUX common port connnected to RF port P2 0x3: MUX common port connnected to RF port P3

SCAN (0x2)

BIT	7	6	5	4	3	2	1	0
Field	CHK_ALL_PORTS	FULL_DWELL	SCAN_DWELL[1:0]		–	–	SCAN_INDEX	START_SCAN
Reset	0x0	0x1	0x01		–	–	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read		–	–	Write, Read, Dual	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION	DECODE
CHK_ALL_PORTS	7		0x0: The port scan routine exits after a carrier has been detected, with dwell time considerations (default) 0x1: Regardless of which port detected the carrier, all unmasked ports are scanned
FULL_DWELL	6		0x0: Index port or exit scan upon carrier detect 0x1: Remain at port until dwell time expires

BITFIELD	BITS	DESCRIPTION	DECODE
SCAN_DWELL	5:4		0x0: Manual Mode holds on RF port during scan until SCAN_INDEX bit is asserted 0x1: 1x bit period dwell time on each RF port during scan 0x2: 16x bit periods dwell time on each RF port during scan, this setting sets scan dwell equal to DIR dwell time 0x3: User-defined multiplier of bit periods for the dwell time on each RF port during scan, reference PINGCFG (0x04) and DWELL_MULT (0x05) registers for the user-programmed value
SCAN_INDEX	1		0x0: Autoincrement of the RF ports based on the SCAN_DWELL time 0x1: When SCAN_DWELL is set to 0x0, a programmed 1 on SCAN_INDEX manually increments the RF port being scanned
START_SCAN	0		0x0: Normal state 0x1: Self-clearing bit, asserting START_SCAN by writing a 1 to this bit begins the port scanning process

RXTX (0x3)

BIT	7	6	5	4	3	2	1	0
Field	RXSENS[3:0]				TXPWR[3:0]			
Reset	0xB				0x7			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
RXSENS	7:4	Adjustable modem receiver threshold	0x0: -20.5dBm, threshold full-scale low 0x1: -20.0dBm 0x2: -19.5dBm 0x3: -19.0dBm 0x4: -18.5dBm 0x5: -18.0dBm 0x6: -17.5dBm 0x7: -17.0dBm 0x8: -16.5dBm 0x9: -16.0dBm 0xA: -15.5dBm 0xB: -15.0dBm, threshold ceiling, default 0xC: -15.0dBm 0xD: -15.0dBm 0xE: -15.0dBm 0xF: -15.0dBm, threshold full-scale high

BITFIELD	BITS	DESCRIPTION	DECODE
TXPWR	3:0	Adjustable modem transmitter output power	0x0: -0.5dBm, output power full-scale low 0x1: 0.0dBm 0x2: 0.5dBm 0x3: 1.0dBm 0x4: 1.5dBm 0x5: 2.0dBm 0x6: 2.5dBm 0x7: 3.0dBm, default output power 0x8: 3.5dBm 0x9: 4.0dBm 0xA: 4.5dBm 0xB: 5.0dBm 0xC: 5.5dBm 0xD: 6.0dBm, output power ceiling 0xE: >6.0dBm, clipping could occur 0xF: >6.0dBm, output power full-scale high

PINGCFG (0x4)

BIT	7	6	5	4	3	2	1	0
Field	DWELL[11:8]				MASK_P3	MASK_P2	MASK_P1	MASK_P0
Reset	0x00				0x1	0x1	0x1	0x1
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DWELL	7:4	User defined dwell time multiplier (upper-nibble)	
MASK_P3	3		0x0: Exclude RF port 3 from the scan sequence 0x1: Include RF port 3 in the scan sequence
MASK_P2	2		0x0: Exclude RF port 2 from the scan sequence 0x1: Include RF port 2 in the scan sequence
MASK_P1	1		0x0: Exclude RF port 1 from the scan sequence 0x1: Include RF port 1 in the scan sequence
MASK_P0	0		0x0: Exclude RF port 0 from the scan sequence 0x1: Include RF port 0 in the scan sequence

DWELL_MULT (0x5)

BIT	7	6	5	4	3	2	1	0
Field	DWELL[7:0]							
Reset	0x52							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DWELL	7:0	User defined dwell time multiplier (middle- and lower-nibble)	0x52: Decimal 82x multiplier of the bit rate, this setting is equal to the length of a PING frame (default)

PORTSTAT (0x6)

BIT	7	6	5	4	3	2	1	0
Field	–	LSTN_PORT[1:0]		SCANNING	AISG_P3	AISG_P2	AISG_P1	AISG_P0
Reset	–	0x00		0x0	0x0	0x0	0x0	0x0
Access Type	–	Read Only		Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LSTN_PORT	6:5		0x0: MUX Scan is on RF port 0 0x1: MUX Scan is on RF port 1 0x2: MUX Scan is on RF port 2 0x3: MUX Scan is on RF port 3
SCANNING	4		0x0: Not scanning 0x1: The MUX port scanning process is active
AISG_P3	3		0x0: No AISG signals were detected on RF Port 3 0x1: AISG carrier detected on RF Port 3
AISG_P2	2		0x0: No AISG signals were detected on RF Port 2 0x1: AISG carrier detected on RF Port 2
AISG_P1	1		0x0: No AISG signals were detected on RF Port 1 0x1: AISG carrier detected on RF Port 1
AISG_P0	0		0x0: No AISG signals were detected on RF Port 0 0x1: AISG carrier detected on RF Port 0

STATUS (0x7)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TXACTIVE	RXOUT	DIR
Reset	–	–	–	–	–	0x1	0x1	0x0
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
TXACTIVE	2		0x0: While DIR is low, TXACTIVE bit is low when TXIN pin is logic-high (1) and there is no OOK carrier signal being transmitted 0x1: While DIR is low, TXACTIVE bit is high when TXIN pin is logic-low (0) and there is an OOK carrier signal being transmitted
RXOUT	1		0x0: While DIR is high, RXOUT bit is low when there is an AISG 0 bit (OOK carrier signal) being received 0x1: While DIR is high, RXOUT bit is high when there is an AISG 1 bit (no OOK carrier signal) being received
DIR	0		0x0: No AISG signal detected at the RXIN 0x1: AISG carrier signal has been detected at the selected RF port

ID1 (0x8)

BIT	7	6	5	4	3	2	1	0
Field	PARTNUM[7:0]							
Reset	0x2F							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PARTNUM	7:0	Part number of the chip

ID2 (0x9)

BIT	7	6	5	4	3	2	1	0
Field	REVNUM[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REVNUM	7:0	Revision number of the chip

Applications Information

Emission Output Profile

The AISG standard defines the maximum spectrum emission that all the OOK modulating devices must be compliant with. Such a spectrum is represented in Figure 15.

The MAX11947 is compliant with the emissions mask as shown in the AISG v3.0.0.10 standard, Figure 10.3.11.3-1.

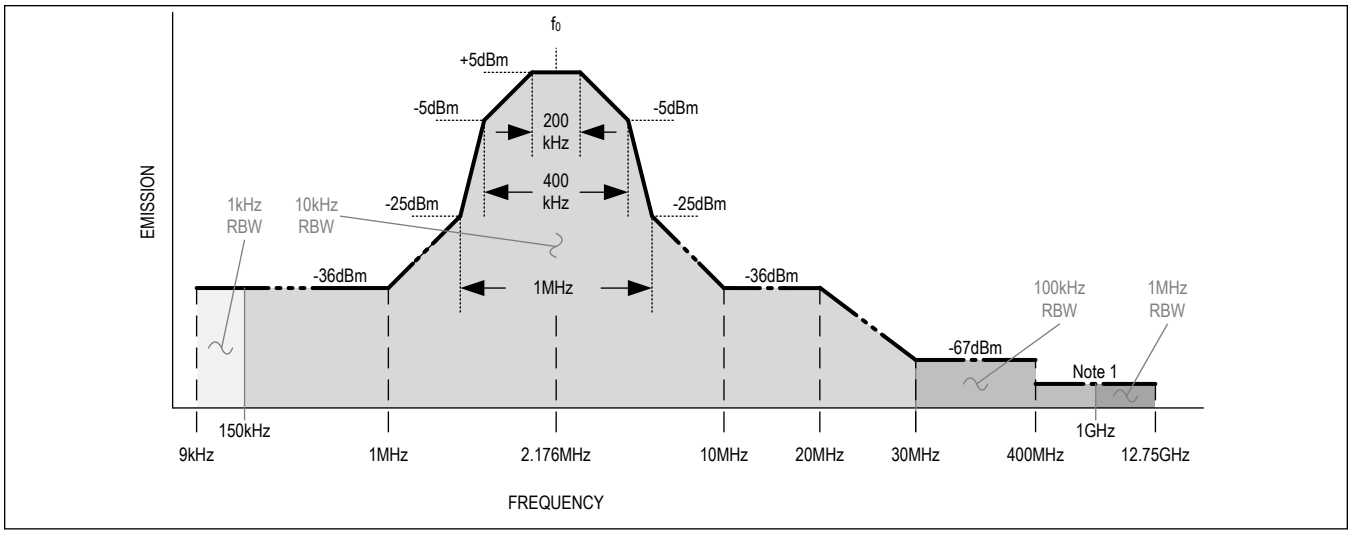


Figure 15. AISG v3.0 Standard Modem Spectrum Emissions Mask

An external 470pF capacitor connected between P_ and ground is recommended for compliance above 25MHz. See the *Typical Application Circuit*.

RF Filter and Selectivity

Description of the receive filter, bandwidth and how the min/max frequency points are tested.

The AISG standard (section 10.3.12) indicates a need for the receiver bandpass filter to remove the influence from any external CW signals. As a minimum, the device has two states it must reject: first, an extra carrier causing an ON signal when the intended carrier at 2.176MHz is at an OFF power level of -18dBm; second, an ON signal (with power ranging from -12dBm to +5dBm) does not indicate an OFF signal because of intermodulation distortion between the two CW signals.

[[AISG Selectivity no-ON Test Conditions]] shows the AISG Test conditions for the first state. The red blocks indicate the power and frequency range of the interfering CW signal: less than or equal to -13dBm power ranging anywhere from 9kHz up to 1.25MHz and 3.7MHz up to 12.75GHz plus the need to reject the Tx carrier signal at the maximum power expected for the ALD system.

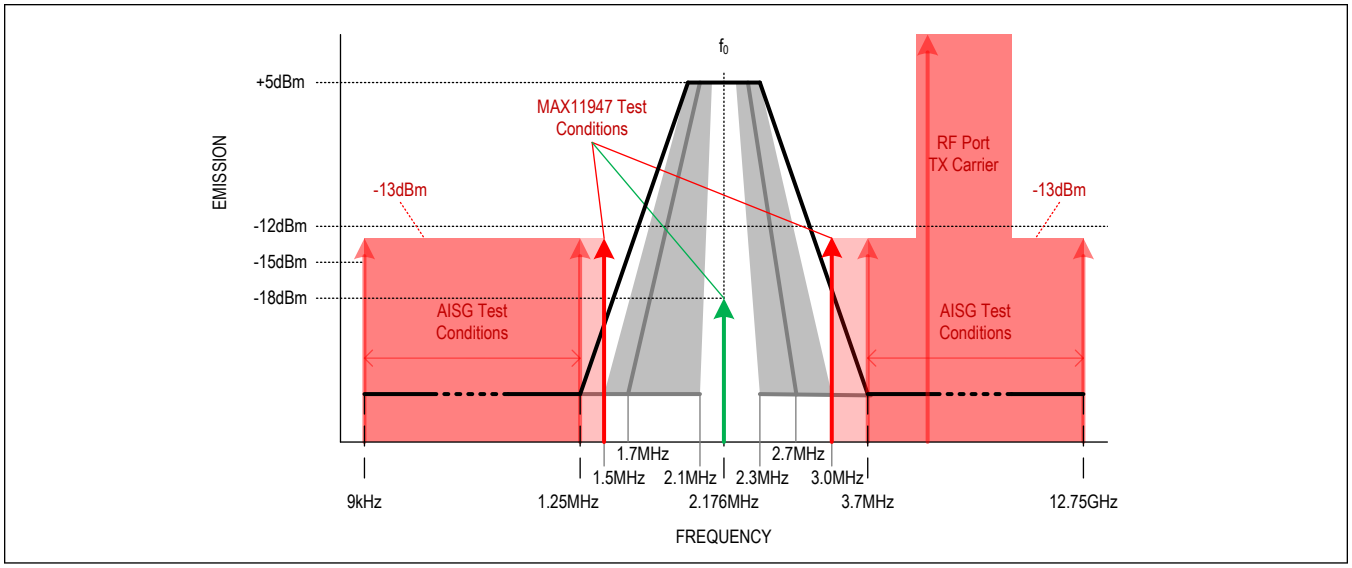


Figure 16. AISG Selectivity No-ON Test Conditions

The MAX11947 is verified at more stringent frequencies by expanding the low-side testing up to 1.5MHz (versus 1.25MHz) and the high-side testing down to 3.0MHz (versus 3.7MHz). These conditions are used to guaranteed the part does not indicate an ON condition (no-ON) when an interfering CW signal is within these bands. This device is tested for a forced-ON state with frequencies of the extra carrier set to 2.1MHz and 2.3MHz as shown in Figure 17. This verifies that the band-pass filter cutoff frequencies fall within the grey area on the plot.

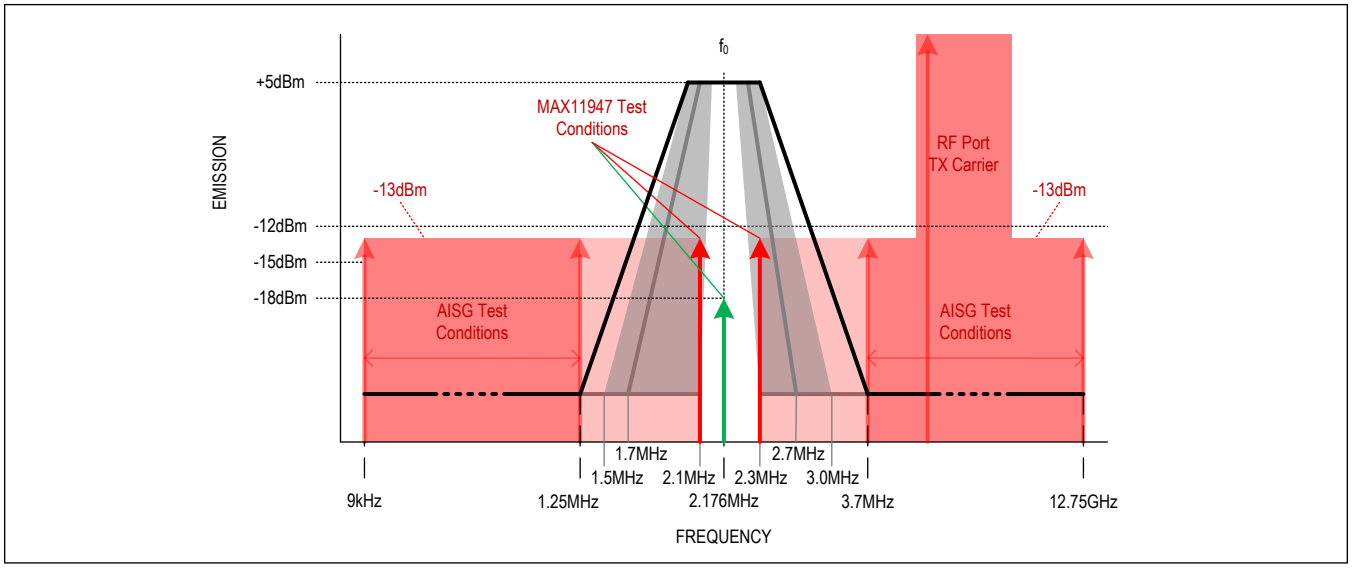


Figure 17. AISG Selectivity Forced-ON Test Conditions

Characterization of the filter shows the receiver only indicates an ON state when a carrier with a power over -12dBm falls between the typical frequencies of 1.7MHz and 2.7MHz.

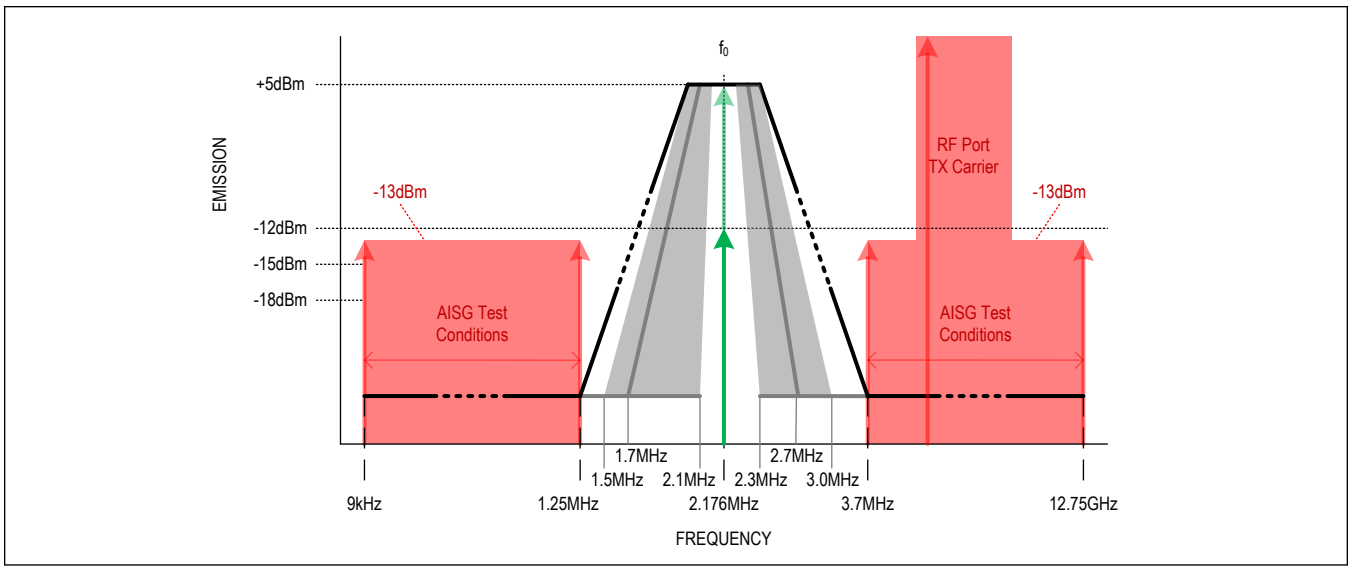


Figure 18. AISG Selectivity No-OFF Test Conditions

Figure 18 depicts the AISG Test conditions for the second state where the receiver should always indicate an ON regardless of the presence of an interfering CW in the red test areas. This condition is not tested on the MAX11947.

External Low-Pass Filter and AC-Coupling to Feeder Cable

The MAX11947 modem specifies several forms of crosstalk and isolation with two simple, required components: a 470pF shunt capacitor for transmitter spectral filtering and a 100nF series capacitor used to block any DC component on the RF feed line (which can range from 10V to 30V). Additional lowpass filtering can be added to each port to increase the port-to-port RF isolation as shown in Figure 19.

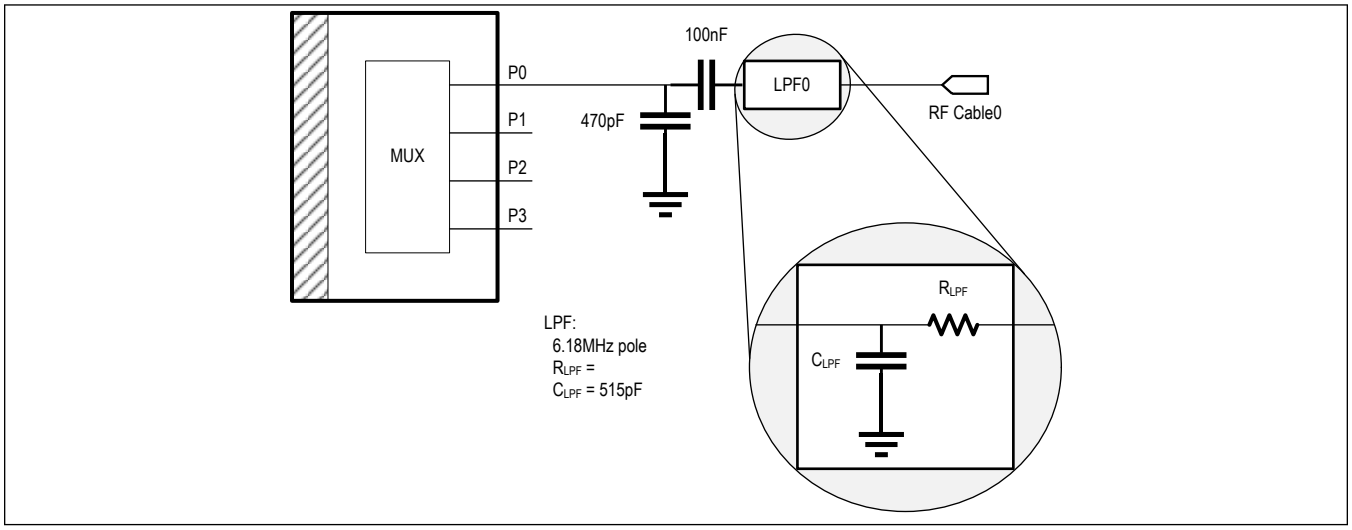


Figure 19. RF Port Filter

A simple RC low-pass filter was implemented in circuit simulation using a 6.18MHz pole with an R_{LPF} = to 50Ω and the C_{LPF} = 515pF. Each port on the MAX11947 evaluation kit has place holders for a three-pole RC filter. By default, the evaluation kit resistors have been shorted (0Ω resistors) and the capacitors are left unpopulated.

In-Line Attenuation

A typical communications channel between a base station master and a tower-mounted antenna line device (ALD) must meet the AISG specified transmitter ON level of +3dBm ±2dB and the OFF level of ≤ -40dBm (section 10.3.11.2 of the AISG v3.0 standard and depicted in Figure 20). Likewise the modem receiver must meet the requirements of definitively indicating a carrier ON level between +5dBm and -12dBm, a carrier OFF level at any power less than -18dBm, and thus the receiver detection threshold must fall in a 6dB window at -15dBm ±3dB (section 10.3.12).

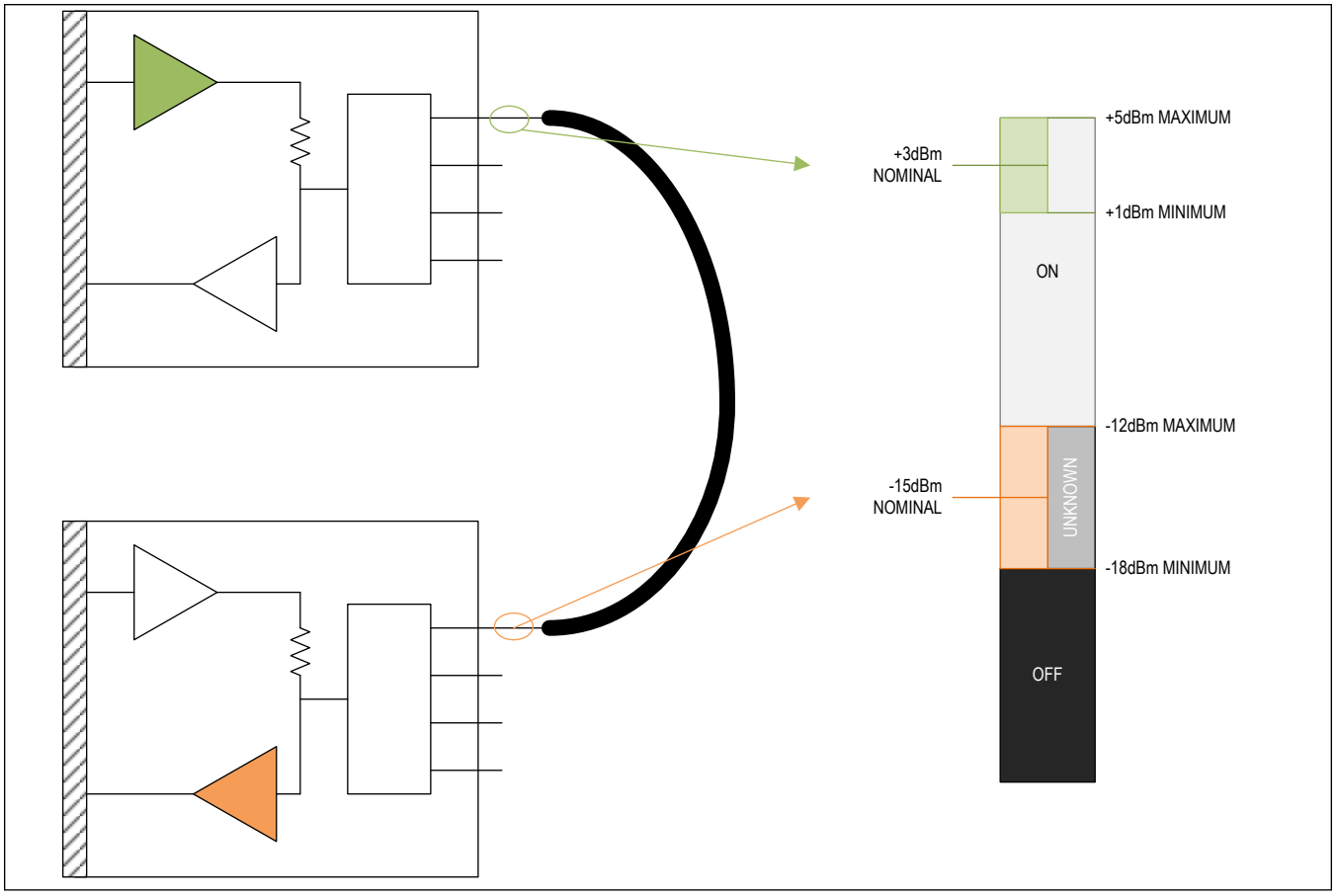


Figure 20. Transmit and Receive Levels

When the modem is used in an ALD system with a line splitter as noted in AISG v3.0 section 10.3.13, both the transmit and receive power levels may need to be adjusted to account for additional signal attenuation through the splitter. Similarly, when an ALD system includes a OOK bypass path, the transmit and receive signals may also be attenuated between the modem and the RF port (section 10.3.15 and depicted in [[AISG - OOK bypass]]).

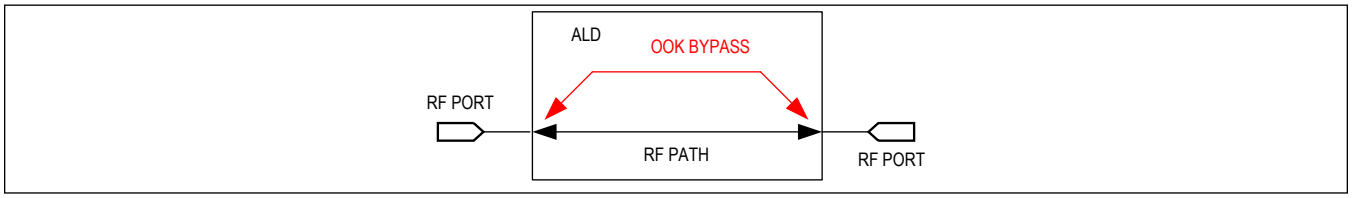


Figure 21. AISG—OOK Bypass

To adjust for the attenuation behind the splitter, the MAX11947 has the ability to increase the transmitter output power as shown in Figure 22.

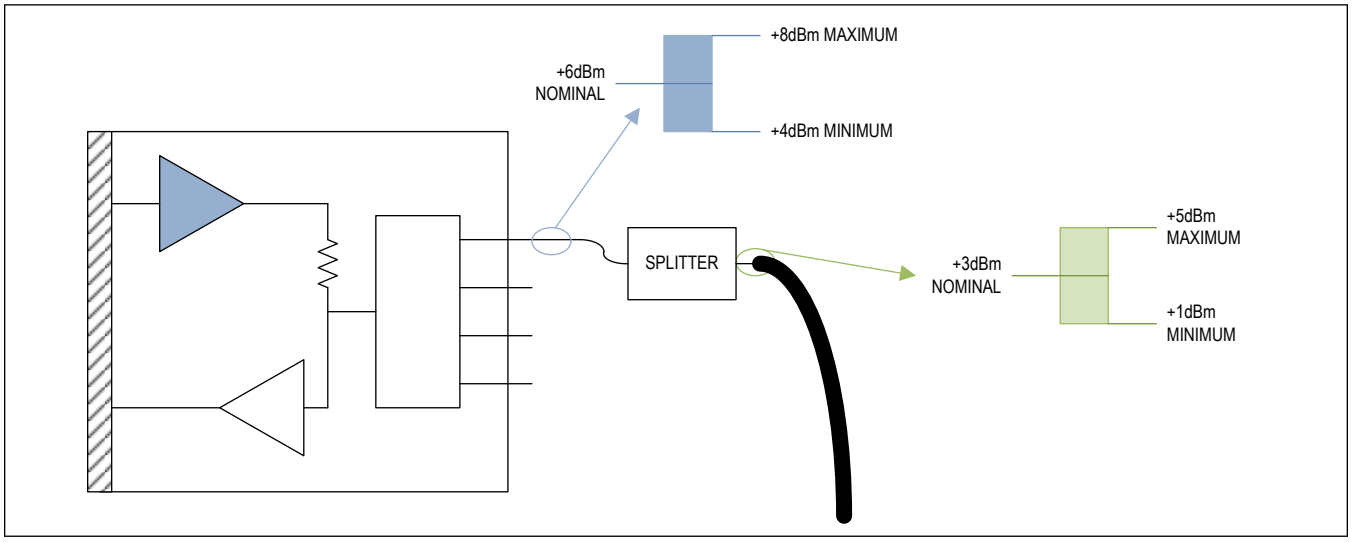


Figure 22. Higher Power Transmitter for Splitter

Similarly, attenuation behind the splitter can effectively shift the sensitivity threshold lower. The MAX11947 has the ability to lower the threshold level to accommodate the power lost through the splitter as shown in Figure 23.

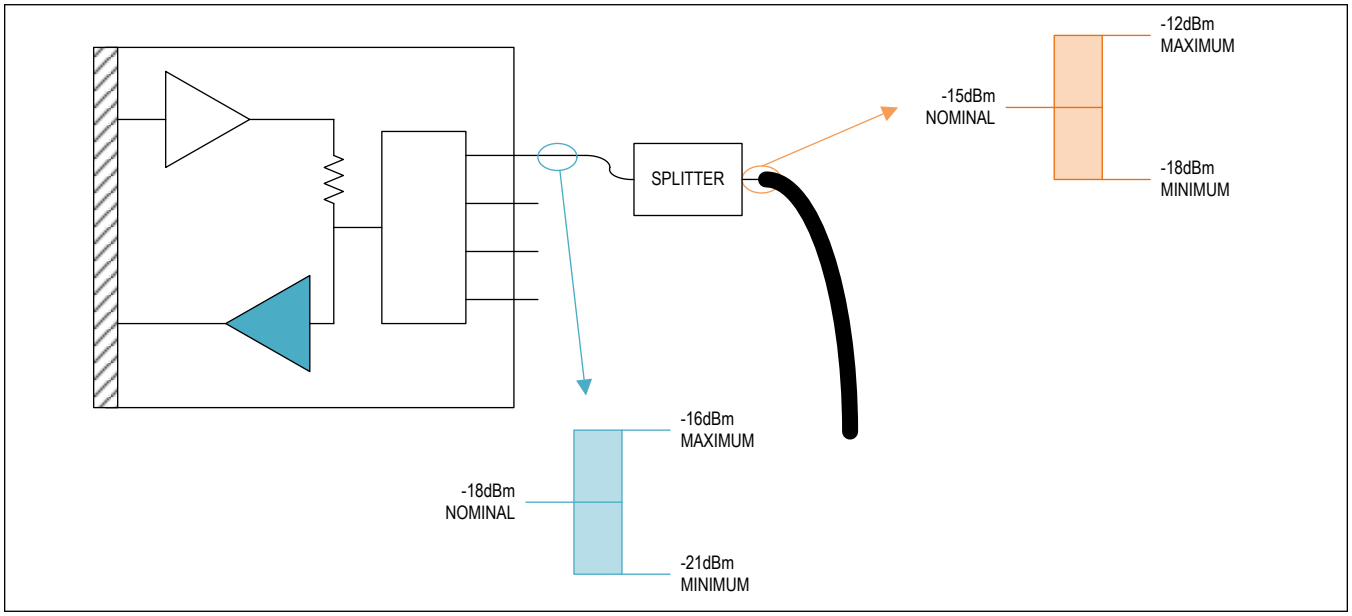


Figure 23. Better Sensitivity Threshold for Receiver with Splitter

Crystal and External Clock

The MAX11947 integrated AISG modem typically operates with an external crystal at 4x the 2.176MHz frequency, or 8.704MHz. The crystal is required to achieve the ±100ppm frequency stability specification of the AISG standard. A crystal with ±30ppm is recommended along with two 40pF (±10% tolerance) capacitors connected to ground as shown

in *Typical Application Circuit*. The capacitors do not affect the oscillation frequency.

The modem can also operate without a crystal, by using a stable external clock source. The external clock should be connected to the XTAL1 pin and the XTAL2 pin on the modem should be connected to ground.

Clock Master/Slave Configuration

Multiple MAX11947 devices can share the same crystal by using the SYNCOUT pin. One device acts as a master and provides the 8.704MHz clock signal to the slave device(s). To configure a device as the clock master, set the OSCBUF bits in the CFG (0x00) register to a value of 0x1 or higher, this turns on the SYNCOUT signal. In the hardware, connect a 1kΩ pullup resistor to V_{CC} from the SYNCOUT pin of the master device. The external clock coming from the master feeds the XTAL1 pin of the slave device and the XTAL2 pin on the slave should be connected to ground. See Figure 24 for an example of the clock master/slave circuit.

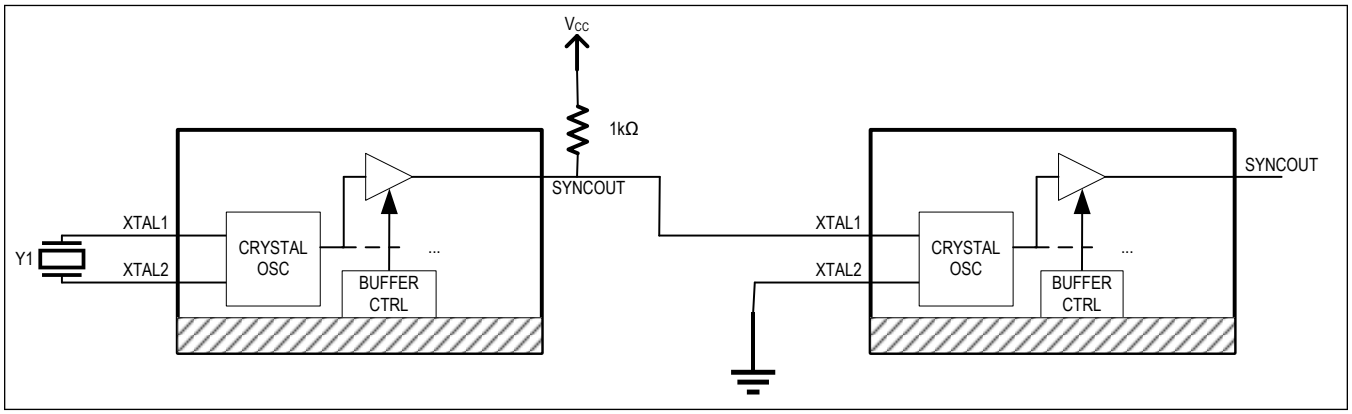


Figure 24. Clock Master/Slave Circuit

If additional drive capability is needed for the SYNCOUT buffer, set the OSCBUF bits to 0x2 or 0x3 as appropriate. Additional daisy-chain configurations can be used if desired.

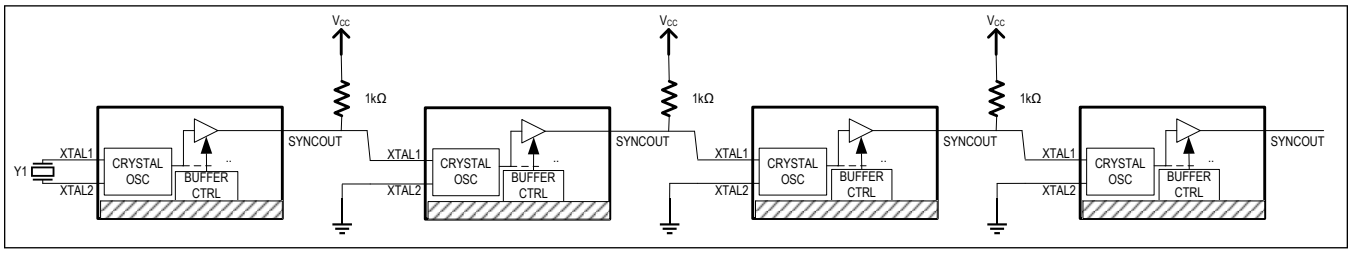


Figure 25. Cascade Daisy-Chain

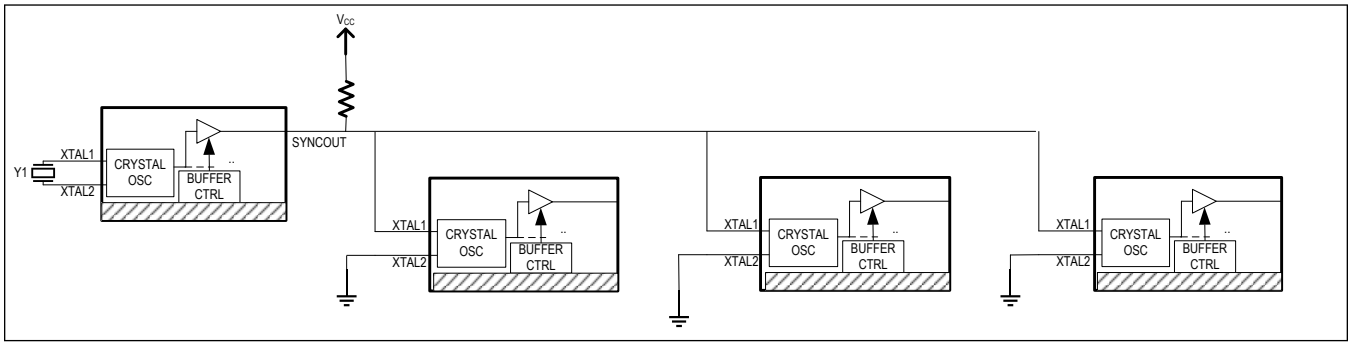


Figure 26. Star Daisy-Chain

Dwell Time

There are effectively two dwell times used in the MAX11947: one is used to maintain the DIR pin in a receive status until an AISG message has timed out and the other is used as part of the automatic port scanning feature. Both times are derived from the data rate (baud rate) that determines the period of a single OOK bit. This bit period is then used to define the fixed DIR pin dwell time as 16-bit periods.

For example, when running at the default 9600kbps NRZ data rate, the bit period is approximately 0.104ms and the DIR dwell time is approximately 1.667ms (approximately 16 x 0.104ms).

The port scanning feature provides the ability to manually index through the MUX ports or to use one of three dwell times (two preset and one custom). These scanning dwell times are 1x a bit period, 16x a bit period, or a user customized count of bit periods. The customized field defaults to a 81x multiplier but can be programmed by the user anywhere from 1x to 4096x the bit period.

The 81-bit period default is an estimate for the length of a ping message. In section 11.11.7 of the AISG v3.0 standard, the ping message is noted to contain a 1-word address, a control word, the FI, GI, and GL words, a 1-octet XID indicating the ping message, and the 4-octet primary ID—summing up to 10 words or 80 bits. Add in the stop and a ping message should be a total of 81 bits in length.

Using the same example of the default 9600kbps data rate above, this custom count of 81x bit periods would equate to 8.438ms, less than the 20ms allocated to receive a Ping message and noticeably less than the 40ms timeout period.

Alternate Modem Interface

Normal modem communication occurs through physical connections to the classic RS-485 modem pins: TXIN, DIR, and RXOUT. However, having all three of these pins represented by four bits in the SPI registers could allow a user to not only configure the MAX11947, but also control of the modem functions through just the serial interface.

Table 6. Alternate Modem Interface

RS-485 PIN	INPUT BIT (REGISTER)	OUTPUT BIT (REGISTER)
TXIN	TX_ON (CFG, 0x0)	TXACTIVE (STATUS, 0x7)
DIR	—	DIR (STATUS, 0x7)
RXOUT	—	RXOUT (STATUS, 0x7)

A typical transmission would occur when the DIR is indicating a transmit-ready state that is represented by a logic-low (0V) level at the DIR pin and a 0 value of the DIR bit in the STATUS register (0x7). The modem begins transmitting the OOK carrier when a logic-low signal (0V) is detected at the TXIN pin or if the TX_ON bit is set to 1 in the CFG register (0x0). The TXACTIVE bit in the STATUS register (0x7) indicates the OOK status of the PA. That is, the TXACTIVE bit is set to 1 if the TX_ON bit is also set to 1 or the TXIN pin is set to logic-low.

When an incoming OOK signal is detected, the MAX11947 asserts the DIR output pin to a logic-high (V_L) level. This same status can be noted by reading a 1 value from the DIR bit in the STATUS register (0x7). After the DIR pin and DIR bit have been set to 1, the RXOUT pin indicates the OOK carrier status by setting the RXOUT pin to logic-low (0V) when the receiver detects an ON carrier or sets the pin to logic-high (V_L) when the carrier is OFF (not detected). The RXOUT field in the STATUS register (0x7) indicates the same: the bit is cleared to 0 when the carrier is detected and set to 1 when the carrier is not detected.

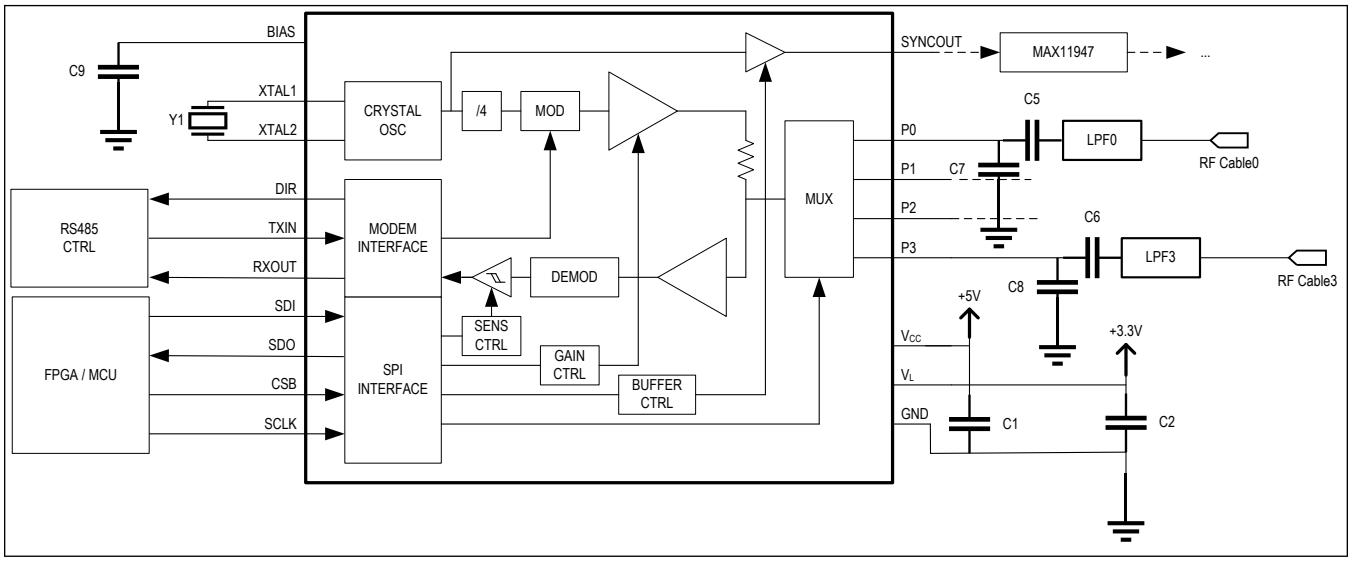
Allowing for the slowest maximum clock rate on the serial interface of 8MHz, plus the requisite 2 words (16 bits) needed to write or read the registers, the fastest SPI interfacing would allow for a maximum of 500k reads per second of the STATUS register. This equates to about 52 samples of the register per each OOK data bit when receiving at a 9600kbps NRZ data rate.

When interfacing the MAX11947 to a microcontroller, the user can trigger an interrupt from the DIR pin rising edge, then initiate a continuous polling sequence of the STATUS register. This allows the user to sample the DIR bit and RXOUT bit values at a rate of 52 readings per OOK bit to allow for an easy decode of the message. After the receive cycle is complete, the SPI interface can then be used to poll the DIR bit for status of the AISG channel. After confirming the

channel is transmit ready (DIR bit is 0), the interface can set and clear the TX_ON bit to send an OOK transmission.

Typical Application Circuit

Circuit 1



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX11947GTP+	-40°C to +105°C	20 TQFN-EP*
MAX11947GTP+T	-40°C to +105°C	20 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed Pad. Connect EP to GND to enhance thermal dissipation.*

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/20	Release for market intro	—