TMS320VC5505
Fixed-Point Digital Signal Processor

Check for Samples: TMS320VC5505

1 Fixed-Point Digital Signal Processor

1.1 TMS320VC5505 Features

- High-Performance, Low-Power, TMS320C55x™ Fixed-Point Digital Signal Processor
  - 16.67-, 10-ns Instruction Cycle Time
  - 60-, 100-MHz Clock Rate
  - One/Two Instruction(s) Executed per Cycle
  - Dual Multipliers [Up to 200 Million Multiply-Accumulates per Second (MMACS)]
  - Two Arithmetic/Logic Units (ALUs)
  - Three Internal Data/Operand Read Buses and Two Internal Data/Operand Write Buses
  - Fully Software-Compatible With C55x Devices
  - Industrial Temperature Devices Available
- 320 K Bytes Zero-Wait State On-Chip RAM, Composed of:
  - 64K Bytes of Dual-Access RAM (DARAM), 8 Blocks of 4K x 16-Bit
  - 256K Bytes of Single-Access RAM (SARAM), 32 Blocks of 4K x 16-Bit
- 128K Bytes of Zero Wait-State On-Chip ROM (4 Blocks of 16K x 16-Bit)
- 16-/8-Bit External Memory Interface (EMIF) with Glueless Interface to:
  - 8-/16-Bit NAND Flash, 1- and 4-Bit ECC
  - 8-/16-Bit NOR Flash
  - Asynchronous Static RAM (SRAM)
- Direct Memory Access (DMA) Controller
  - Four DMA With 4 Channels Each (16-Channels Total)
- Three 32-Bit General-Purpose Timers
  - One Selectable as a Watchdog and/or GP
- Two MultiMedia Card/Secure Digital (MMC/SD) Interfaces
- Universal Asynchronous Receiver/Transmitter (UART)
- Serial-Port Interface (SPI) With Four Chip-Selects
- Master/Slave Inter-Integrated Circuit (I^2C Bus™)
- Four Inter-IC Sound (I^2S Bus™) for Data Transport
- Device USB Port With Integrated 2.0 High-Speed PHY that Supports:
  - USB 2.0 Full- and High-Speed Device
- LCD Bridge With Asynchronous Interface
- Tightly-Coupled FFT Hardware Accelerator
- 10-Bit 4-Input Successive Approximation (SAR) ADC
- Real-Time Clock (RTC) With Crystal Input, With Separate Clock Domain, Separate Power Supply
- Four Core Isolated Power Supply Domains: Analog, RTC, CPU and Peripherals, and USB
- Four I/O Isolated Power Supply Domains: RTC I/O, EMIF I/O, USB PHY, and DV_{DDIO}
- Low-Power S/W Programmable Phase-Locked Loop (PLL) Clock Generator
- On-Chip ROM Bootloader (RBL) to Boot From NAND Flash, NOR Flash, SPI EEPROM, or I2C EEPROM
- IEEE-1149.1 (JTAG™) Boundary-Scan-Compatible
- Up to 26 General-Purpose I/O (GPIO) Pins (Multiplexed With Other Device Functions)
- 196-Terminal Pb-Free Plastic BGA (Ball Grid Array) (ZCH Suffix)
- 1.05-V Core (60 MHz), 1.8-V, 2.5-V, 2.8-V, or 3.3-V I/Os
- 1.3-V Core (100 MHz), 1.8-V, 2.5-V, 2.8-V, or 3.3-V I/Os
- Applications:
  - Wireless Audio Devices (e.g., Headsets, Microphones, Speakerphones, etc.)
  - Echo Cancellation Headphones
  - Portable Medical Devices
  - Voice Applications
  - Industrial Controls
  - Fingerprint Biometrics
  - Software Defined Radio
- Community Resources
  - TI E2E Community
  - TI Embedded Processors Wiki

1.2 Description

The TMS320VC5505 is a member of TI's TMS320C5000™ fixed-point Digital Signal Processor (DSP) product family and is designed for low-power applications.

The TMS320VC5505 fixed-point DSP is based on the TMS320C55x™ DSP generation CPU processor core. The C55x™ DSP architecture achieves high performance and low power through increased parallelism and total focus on power savings. The CPU supports an internal bus structure that is composed of one program bus, one 32-bit data read bus and two 16-bit data read buses, two 16-bit data write buses, and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to four 16-bit data reads and two 16-bit data writes in a single cycle. The TMS320VC5505 also includes four DMA controllers, each with 4 channels, providing data movements for 16-independent channel contexts without CPU intervention. Each DMA controller can perform one 32-bit data transfer per cycle, in parallel and independent of the CPU activity.

The C55x CPU provides two multiply-accumulate (MAC) units, each capable of 17-bit x 17-bit multiplication and a 32-bit add in a single cycle. A central 40-bit arithmetic/logic unit (ALU) is supported by an additional 16-bit ALU. Use of the ALUs is under instruction set control, providing the ability to optimize parallel activity and power consumption. These resources are managed in the Address Unit (AU) and Data Unit (DU) of the C55x CPU.

The C55x CPU supports a variable byte width instruction set for improved code density. The Instruction Unit (IU) performs 32-bit program fetches from internal or external memory and queues instructions for the Program Unit (PU). The Program Unit decodes the instructions, directs tasks to the Address Unit (AU) and Data Unit (DU) resources, and manages the fully protected pipeline. Predictive branching capability avoids pipeline flushes on execution of conditional instructions.

The general-purpose input and output functions along with the 10-bit SAR ADC provide sufficient pins for status, interrupts, and bit I/O for LCD displays, keyboards, and media interfaces. Serial media is supported through two MultiMedia Card/Secure Digital (MMC/SD) peripherals, four Inter-IC Sound (I2S Bus™) modules, one Serial-Port Interface (SPI) with up to 4 chip selects, one I2C multi-master and slave interface, and a Universal Asynchronous Receiver/Transmitter (UART) interface.

The VC5505 peripheral set includes an external memory interface (EMIF) that provides glueless access to asynchronous memories like EPROM, NOR, NAND, and SRAM. Additional peripherals include: a high-speed Universal Serial Bus (USB2.0) device mode only, and a real-time clock (RTC). This device also includes three general-purpose timers with one configurable as a watchdog timer, and a analog phase-locked loop (APLL) clock generator.

In addition, the VC5505 includes a tightly-coupled FFT Hardware Accelerator. The tightly-coupled FFT Hardware Accelerator supports 8 to 1024-point (in power of 2) real and complex-valued FFTs.

The VC5505 is supported by the industry's award-winning eXpressDSP™, Code Composer Studio™ Integrated Development Environment (IDE), DSP/BIOS™, Texas Instruments' algorithm standard, and the industry's largest third-party network. Code Composer Studio IDE features code generation tools including a C Compiler and Linker, RTDX™, XDS100™, XDS510™, XDS560™ emulation device drivers, and evaluation modules. The VC5505 is also supported by the C55x DSP Library which features more than 50 foundational software kernels (FIR filters, IIR filters, FFTs, and various math functions) as well as chip support libraries.

1.3 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the VC5505 device.

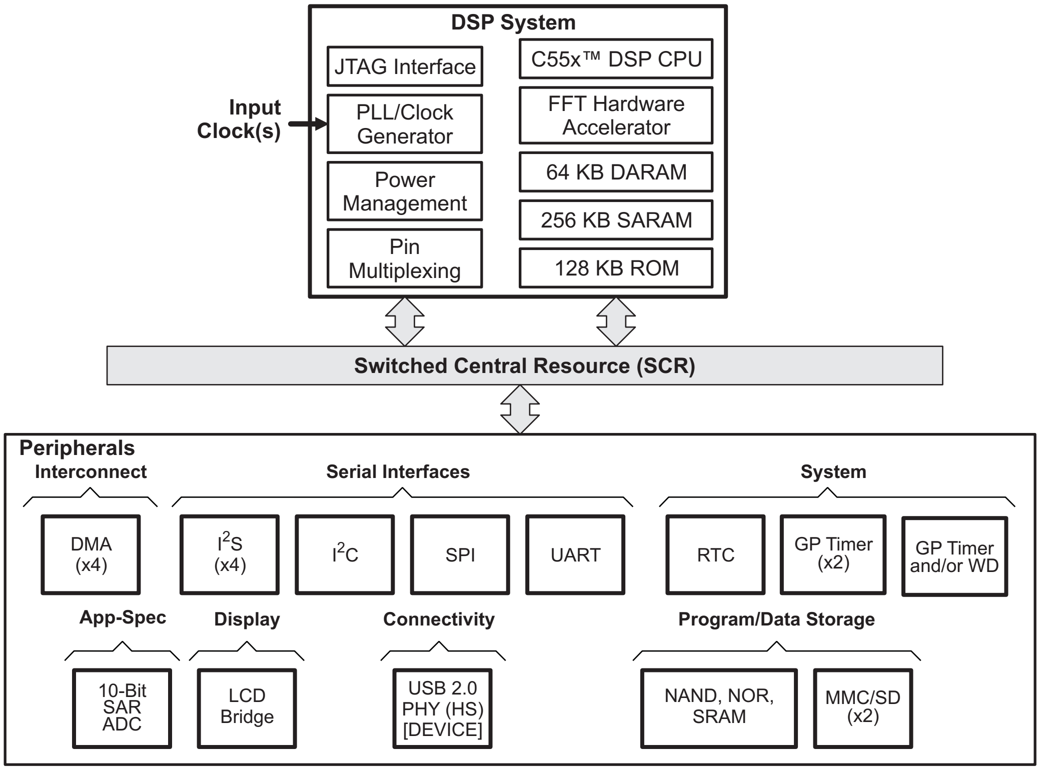


Figure 1-1. TMS320VC5505 Functional Block Diagram

2 Revision History

This data manual revision history highlights the technical changes made to the SPRS503A device-specific data manual to make it an SPRS503B revision.

Scope: Applicable updates to the TMS320C5000 device family, specifically relating to the TMS320VC5505 device (Silicon Revisions 1.4) which is now in the production data (PD) stage of development have been incorporated.

Note: As TMS320VC550x related documentation is released, the ulink references will operate properly. If the related docs are as yet not released, the ulink will appear to be broken.

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 5 Device Operating Conditions	Section 5.2 Recommended Operating Conditions • Updated/Changed USB_V_{DDPLL}, USB_V_{DDOSC}, and USB_V_{DDA3P3} MIN value ***from*** "3.14" ***to*** "2.97" V • Updated/Changed USB_V_{DDPLL}, USB_V_{DDOSC}, and USB_V_{DDA3P3} MAX value ***from*** "3.46" ***to*** "3.63" V
Section 6.8.2 Wake-Up From IDLE Electrical Data/Timing	Table 6-9 Switching Characteristics Over Recommended Operating Conditions For Wake-Up From IDLE • Added footnote that references LDO.

3 Device Overview

3.1 Device Characteristics

Table 3-1, provides an overview of the TMS320VC5505 DSP. The tables show significant features of the VC5505 device, including the capacity of on-chip RAM, the peripherals, the CPU frequency, and the package type with pin count.

Table 3-1. Characteristics of the VC5505 Processor

HARDWARE FEATURES			VC5505
Peripherals Not all peripheral pins are available at the same time (for more detail, see the Device Configurations section).	External Memory Interface (EMIF)		Asynchronous (8/16-bit bus width) SRAM, Flash (NOR, NAND)
	Flash Cards		2 MMC/SD
	DMA		Four DMA controllers each with four channels, for a total of 16 channels
	Timers		2 32-Bit General-Purpose (GP) Timers 1 Additional Configurable as a 32-Bit GP Timer and/or a Watchdog
	UART		1 (with RTS/CTS flow control)
	SPI		1 with 4 chip selects
	I^2C		1 (Master/Slave)
	I^2S		4 (Two Channel, Full Duplex Communication)
	USB 2.0 (Device *only*)		High- and Full-Speed Device
	MMC/SD		256 byte read/write buffer, max 50-MHz clock for SD cards, and signaling for DMA transfers
	LCD Bridge		1 (8-bit or 16-bit asynchronous parallel bus)
	ADC (Successive Approximation [SAR])		1 (10-bit, 4-input, 16-μs conversion time)
	Real-Time Clock (RTC)		1 (Crystal Input, Separate Clock Domain and Power Supply)
	FFT Hardware Accelerator		1 (Supports 8 to 1024-point 16-bit real and complex FFT)
	General-Purpose Input/Output Port (GPIO)		Up to 26 pins (with 1 Additional General-Purpose Output (XF) and 4 Special-Purpose Outputs for Use With SAR)
On-Chip Memory	Size (Bytes)		320 KB RAM, 128KB ROM
	Organization		• 64KB On-Chip Dual-Access RAM (DARAM) • 256 KB On-Chip Single-Access RAM (SARAM) • 128KB On-Chip Single-Access ROM (SAROM)
JTAG BSDL_ID	JTAG ID Register (Value is: 0009_702F)		see Figure 6-40
CPU Frequency	MHz	1.05-V Core	60 MHz
		1.3-V Core	100 MHz
Cycle Time	ns	1.05-V Core	16.67 ns
		1.3-V Core	10 ns
Voltage	Core (V)		1.05 V (60 MHz)
			1.3 V (100 MHz)
	I/O (V)		1.8 V, 2.5 V, 2.8 V, 3.3 V
Power Characterization	Active @ Room Temp 25°C, 75% DMAC + 25% ADD (Typical Sine Wave Data Switching)		0.15 mW/MHz @ 1.05 V, 60 MHz 0.22 mW/MHz @ 1.3 V, 100 MHz
	Active @ Room Temp 25°C, 75% DMAC + 25% NOP (Typical Sine Wave Data Switching)		0.14 mW/MHz @ 1.05 V, 60 MHz 0.22 mW/MHz @ 1.3 V, 100 MHz
	Active @ Room Temp 25°C, Hardware FFT Accelerator 1024-pt FFT, ROM Execution		0.25 mW/MHz @ 1.05 V, 60 MHz 0.31 mW/MHz @ 1.3 V, 100 MHz

Table 3-1. Characteristics of the VC5505 Processor (continued)

HARDWARE FEATURES		VC5505
	Standby (Master Clock Disabled) @ Room Temp 25°C (DARAM and SARAM in Active Mode)	0.26 mW @ 1.05 V 0.44 mW @ 1.3 V
	Standby (Master Clock Disabled) @ Room Temp 25°C (DARAM in Retention and SARAM in Active Mode)	0.23 mW @ 1.05 V 0.40 mW @ 1.3 V
	Standby (Master Clock Disabled) @ Room Temp 25°C (DARAM in Active Mode and SARAM in Retention)	0.15 mW @ 1.05 V 0.28 mW @ 1.3 V
PLL Options	Software Programmable Multiplier	x4 to x4099 multiplier
BGA Package	10 x 10 mm	196-Pin BGA (ZCH)
Process Technology	µm	0.09 µm
Product Status (1)	Product Preview (PP), Advance Information (AI), or Production Data (PD)	PD

(1) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

3.2 C55x CPU

The TMS320VC5505 fixed-point digital signal processor (DSP) is based on the C55x CPU 3.3 generation processor core. The C55x DSP architecture achieves high performance and low power through increased parallelism and total focus on power savings. The CPU supports an internal bus structure that is composed of one program bus, three data read buses (one 32-bit data read bus and two 16-bit data read buses), two 16-bit data write buses, and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to four data reads and two data writes in a single cycle. Each DMA controller can perform one 32-bit data transfer per cycle, in parallel and independent of the CPU activity.

The C55x CPU provides two multiply-accumulate (MAC) units, each capable of 17-bit x 17-bit multiplication in a single cycle. A central 40-bit arithmetic/logic unit (ALU) is supported by an additional 16-bit ALU. Use of the ALUs is under instruction set control, providing the ability to optimize parallel activity and power consumption. These resources are managed in the Address Unit (AU) and Data Unit (DU) of the C55x CPU.

The C55x DSP generation supports a variable byte width instruction set for improved code density. The Instruction Unit (IU) performs 32-bit program fetches from internal or external memory, stores them in a 128-byte Instruction Buffer Queue, and queues instructions for the Program Unit (PU). The Program Unit decodes the instructions, directs tasks to AU and DU resources, and manages the fully protected pipeline. Predictive branching capability avoids pipeline flushes on execution of conditional instructions calls.

For more detailed information on the CPU, see the *TMS320C55x CPU 3.0 CPU* Reference Guide (literature number SWPU073).

The C55x core of the VC5505 can address 16M bytes of unified data and program space. It also addresses 64K words of I/O space. The VC5505 includes three types of on-chip memory: 128 KB read-only memory (ROM), 256 KB single-access random access memory (SARAM), 64 KB dual-access random access memory (DARAM). The memory map is shown in Figure 3-1.

3.2.1 On-Chip Dual-Access RAM (DARAM)

The DARAM is located in the byte address range 000000h − 00FFFFh and is composed of eight blocks of 4K words each (see Table 3-2). Each DARAM block can perform two accesses per cycle (two reads, two writes, or a read and a write). The DARAM can be accessed by the internal program, data, or DMA buses.

Table 3-2. DARAM Blocks

CPU BYTE ADDRESS RANGE	DMA CONTROLLER BYTE ADDRESS RANGE	MEMORY BLOCK
000000h – 001FFFh	0001 0000h – 0001 1FFFh	DARAM 0 (1)
002000h – 003FFFh	0001 2000h – 0001 3FFFh	DARAM 1
004000h – 005FFFh	0001 4000h – 0001 5FFFh	DARAM 2
006000h – 007FFFh	0001 6000h – 0001 7FFFh	DARAM 3
008000h – 009FFFh	0001 8000h – 0001 9FFFh	DARAM 4
00A000h – 00BFFFh	0001 A000h – 0001 BFFFh	DARAM 5
00C000h – 00DFFFh	0001 C000h – 0001 DFFFh	DARAM 6
00E000h – 00FFFFh	0001 E000h – 0001 FFFFh	DARAM 7

(1) The first 192 bytes are reserved for memory-mapped registers (MMRs). See Figure 3-1 , TMS320VC5505 Memory Map Summary.

3.2.2 On-Chip Single-Access RAM (SARAM)

The SARAM is located at the byte address range 010000h – 04FFFF h and is composed of 32 blocks of 4K words each (see Table 3-3). Each SARAM block can perform one access per cycle (one read or one write). SARAM can be accessed by the internal program, data, or DMA buses. SARAM is also accessed by the USB and LCD DMA buses.

Table 3-3. SARAM Blocks

CPU BYTE ADDRESS RANGE	DMA/USB CONTROLLER BYTE ADDRESS RANGE	MEMORY BLOCK
010000h − 011FFFh	0009 0000h – 0009 1FFFh	SARAM 0
012000h − 013FFFh	0009 2000h – 0009 3FFFh	SARAM 1
014000h − 015FFFh	0009 4000h – 0009 5FFFh	SARAM 2
016000h − 017FFFh	0009 6000h – 0009 7FFFh	SARAM 3
018000h − 019FFFh	0009 8000h – 0009 9FFFh	SARAM 4
01A000h − 01BFFFh	0009 A000h – 0009 BFFFh	SARAM 5
01C000h − 01DFFFh	0009 C000h – 0009 DFFFh	SARAM 6
01E000h − 01FFFFh	0009 E000h – 0009 FFFFh	SARAM 7
020000h − 021FFFh	000A 0000h – 000A 1FFFh	SARAM 8
022000h − 023FFFh	000A 2000h – 000A 3FFFh	SARAM 9
024000h − 025FFFh	000A 4000h – 000A 5FFFh	SARAM 10
026000h − 027FFFh	000A 6000h – 000A 7FFFh	SARAM 11
028000h − 029FFFh	000A 8000h – 000A 9FFFh	SARAM 12
02A000h − 02BFFFh	000A A000h – 000A BFFFh	SARAM 13
02C000h − 02DFFFh	000A C000h – 000A DFFFh	SARAM 14
02E000h − 02FFFFh	000A E000h – 000A FFFFh	SARAM 15

Table 3-3. SARAM Blocks (continued)

CPU BYTE ADDRESS RANGE	DMA/USB CONTROLLER BYTE ADDRESS RANGE	MEMORY BLOCK
030000h – 031FFFh	000B 0000h – 000B 1FFFh	SARAM 16
032000h – 033FFFh	000B 2000h – 000B 3FFFh	SARAM 17
034000h – 035FFFh	000B 4000h – 000B 5FFFh	SARAM 18
036000h – 037FFFh	000B 6000h – 000B 7FFFh	SARAM 19
038000h – 039FFFh	000B 8000h – 000B 9FFFh	SARAM 20
03A000h – 03BFFFh	000B A000h – 000B BFFFh	SARAM 21
03C000h – 03DFFFh	000B C000h – 000B DFFFh	SARAM 22
03E000h – 03FFFFh	000B E000h – 000B FFFFh	SARAM 23
040000h – 041FFFh	000C 0000h – 000C 1FFFh	SARAM 24
042000h – 043FFFh	000C 2000h – 000C 3FFFh	SARAM 25
044000h – 045FFFh	000C 4000h – 000C 5FFFh	SARAM 26
046000h – 047FFFh	000C 6000h – 000C 7FFFh	SARAM 27
048000h – 049FFFh	000C 8000h – 000C 9FFFh	SARAM 28
04A000h – 04BFFFh	000C A000h – 000C BFFFh	SARAM 29
04C000h – 04DFFFh	000C C000h – 000C DFFFh	SARAM 30
04E000h – 04FFFFh	000C E000h – 000C FFFFh	SARAM 31 (1)

(1) SARAM31 (byte address range: 0x4E000 – 0x4EFFF) is reserved for the bootloader. After the boot process is complete, this memory space can be used.

3.2.3 On-Chip Read-Only Memory (ROM)

The zero-wait-state ROM is located at the byte address range FE0000h – FFFFFFh. The ROM is composed of four 16K-word blocks, for a total of 128K bytes of ROM. The ROM address space can be mapped by software to the external memory or to the internal ROM.

The standard VC5505 device includes a Bootloader program resident in the ROM.

When the MPNMC bit field of the ST3 status register is cleared (by default), the byte address range FE0000h – FFFFFFh is reserved for the on-chip ROM. When the MPNMC bit field of the ST3 status register is set through software, the on-chip ROM is disabled and not present in the memory map, and byte address range FE0000h – FFFFFFh is directed to external memory space. A hardware reset always clears the MPNMC bit, so it is not possible to disable the ROM at reset. However, the software reset instruction does not affect the MPNMC bit. The ROM can be accessed by the program and data buses. Each on-chip ROM block is a one cycle per word access memory.

3.2.4 External Memory

The external memory space of the device is located at the byte address range 050000h – FFFFFFh. The external memory space is divided into four chip select spaces: EMIF CS2 through CS5 space dedicated to asynchronous devices including flash. Each chip select space has a corresponding chip select pin (called EMIF_CSx) that is activated during an access to the chip select space.

The external memory interface (EMIF) provides the means for the DSP to access external memories and other devices including: NOR Flash, NAND Flash, and SRAM. Before accessing external memory, you must configure the EMIF through its memory-mapped registers.

The EMIF provides a configurable 16- or 8-bit data bus, an address bus width of up to 21-bits, and 4 dedicated chip selects, along with memory control signals. To maximize power savings, the I/O pin of the EMIF can be operated at an independent voltage from the rest of other I/O pins on the device.

3.2.5 I/O Memory

The VC5505 DSP includes a 64K byte I/O space for the memory-mapped registers of the DSP peripherals and system registers used for idle control, status monitoring and system configuration. I/O space is separate from program/memory space and is accessed with separate instruction opcodes or via the DMA's.

Table 3-4 lists the memory-mapped registers of the device. Note that not all addresses in the 64K byte I/O space are used; these addresses should be treated as RESERVED and not accessed by the CPU nor DMA.. For the expanded tables of each peripheral, see Section 6, *Peripheral Information and Electrical Specifications* of this document.

Some DMA controllers have access to the I/O-Space memory-mapped registers of the following peripherals registers: I2C, UART, I2S, MMC/SD, EMIF, USB, and SAR ADC .

Before accessing any peripheral memory-mapped register, make sure the peripheral being accessed is not held in reset via the Peripheral Reset Control Register (PRCR) and its internal clock is enabled via the Peripheral Clock Gating Control Registers (PCGCR1 and PCGCR2).

Table 3-4. Peripheral I/O-Space Control Registers

WORD ADDRESS	PERIPHERAL
0x0000 – 0x0004	Idle Control
0x0005 – 0x000D through 0x0803 – 0x0BFF	Reserved
0x0C00 – 0x0C7F	DMA0
0x0C80 – 0x0CFF	Reserved
0x0D00 – 0x0D7F	DMA1
0x0D80 – 0x0DFF	Reserved
0x0E00 – 0x0E7F	DMA2
0x0E80 – 0x0EFF	Reserved
0x0F00 – 0x0F7F	DMA3
0x0F80 – 0x0FFF	Reserved
0x1000 – 0x10DD	EMIF
0x10EE – 0x10FF through 0x1300 – 0x17FF	Reserved
0x1800 – 0x181F	Timer0
0x1820 – 0x183F	Reserved
0x1840 – 0x185F	Timer1
0x1860 – 0x187F	Reserved
0x1880 – 0x189F	Timer2
0x1900 – 0x197F	RTC
0x1980 – 0x19FF	Reserved
0x1A00 – 0x1A6C	I2C
0x1A6D – 0x1AFF	Reserved
0x1B00 – 0x1B1F	UART
0x1B80 – 0x1BFF	Reserved
0x1C00 – 0x1CFF	System Control
0x1D00 – 0x1FFF through 0x2600 – 0x27FF	Reserved
0x2800 – 0x2840	I2S0
0x2900 – 0x2940	I2S1
0x2A00 – 0x2A40	I2S2
0x2B00 – 0x2B40	I2S3
0x2C41 – 0x2DFF	Reserved
0x2E00 – 0x2E40	LCD

Table 3-4. Peripheral I/O-Space Control Registers (continued)

WORD ADDRESS	PERIPHERAL
0x2E41 – 0x2FFF	Reserved
0x3000 – 0x300F	SPI
0x3010 – 0x39FF	Reserved
0x3A00 – 0x3A1F	MMC/SD0
0x3A20 – 0x3AFF	Reserved
0x3B00 – 0x3B1F	MMC/SD1
0x3B2F – 0x6FFF	Reserved
0x7000 – 0x70FF	SAR and Analog Control Registers
0x7100 – 0x7FFF	Reserved
0x8000 – 0xFFFF	USB

3.3 Memory Map Summary

The VC5505 provides 16M bytes of total memory space composed of on-chip RAM, on-chip ROM, and external memory space supporting a variety of memory types. The on-chip, dual-access RAM allows two accesses to a given block during the same cycle. The VC5505 supports 8 blocks of 4K words of dual-access RAM. The on-chip, single-access RAM allows one access to a given block per cycle. The VC5505 supports 32 blocks of 4K words of single-access RAM.

The remainder of the memory map is divided into reserved areas, four external spaces, and on-chip ROM. Each external space has a chip select decode signal (called CS[2:5]) that indicates an access to the selected space. The external memory interface (EMIF) supports access to asynchronous memories such as SRAM, NAND, or NOR.

The DSP memory is accessible by different master modules within the DSP, including the C55x CPU, the four DMA controllers, LCD, and USB (see Figure 3-1).

CPU BYTE ADDRESS[A]	DMA/USB/LCD BYTE ADDRESS[A]	MEMORY BLOCKS	BLOCK SIZE
000000h	0001 0000h	MMR (Reserved)[B]	
0000C0h	0001 00C0h	DARAM[D]	64K Minus 192 Bytes
010000h	0009 0000h	SARAM	256K Bytes
050000h	0100 0000h	Reserved	8M Minus 320K Bytes
800000h	0200 0000h	External-CS2 Space[C]	4M Bytes Asynchronous
C00000h	0300 0000h	External-CS3 Space[C]	2M Bytes Asynchronous
E00000h	0400 0000h	External-CS4 Space[C]	1M Bytes Asynchronous
F00000h	0500 0000h	External-CS5 Space[C]	1M Minus 128K Bytes Asynchronous
FE0000h	050E 0000h	ROM (if MPNMC=0) / External-CS5 Space[C] (if MPNMC=1)	128K Bytes Asynchronous (if MPNMC=1) 128K Bytes ROM (if MPNMC=0)
FFFFFFh	050F FFFFh		

A. Address shown represents the first byte address in each block.
B. The first 192 bytes are reserved for memory-mapped registers (MMRs).
C. Out of the four DMA controllers, *only* DMA controller 3 has access to the external memory space.
D. The USB and LCD controllers do not have access to DARAM.

Figure 3-1. TMS320VC5505 Memory Map Summary

3.4 Pin Assignments

Extensive use of pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using software programmable register settings. For more information on pin muxing, see Section 4.7, *Multiplexed Pin Configurations* of this document.

3.4.1 Pin Map (Bottom View)

Figure 3-2 shows the bottom view of the package pin assignments.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
P	EM_DQM1	DV_{DDEMIF}	DV_{DDIO}	LCD_ CS0_E0/ SPI_CS0	LCD_ RW_WRB/ SPI_CS2	LCD_D[0]/ SPI_RX	LCD_D[2]/ GP[12]	DV_{DDIO}	LCD_D[5]/ GP[15]	LCD_D[7]/ GP[17]	LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX	LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX
N	EM_A[15]/ GP[21]	RSV13	LCD_ EN_RDB/ SPI_CLK	LCD_ CS1_EN1/ SPI_CS1	LCD_RS/ SPI_CS3	LCD_D[1]/ SPI_TX	LCD_D[3]/ GP[13]	LCD_D[4]/ GP[14]	LCD_D[6]/ GP[16]	LCD_D[8]/ I2S2_CLK/ GP[18]/ SPI_CLK	LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX	LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK	LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	DV_{DDIO}
M	EM_A[14]	EM_D[5]	RSV12	EM_CS3	EMU1	TCK	TDO	XF	TRST	MMC0_D1/ I2S0_RX/ GP[3]	MMC0_CMD/ I2S0_FS/ GP[1]	MMC1_D1/ I2S1_RX/ GP[9]	MMC1_CLK/ I2S1_CLK/ GP[6]	MMC1_D0/ I2S1_DX/ GP[8]
L	EM_A[13]	EM_A[10]	EM_D[12]	EM_D[4]	CV_{DD}	EMU0	TDI	TMS	MMC0_D0/ I2S0_DX/ GP[2]	MMC0_CLK/ I2S0_CLK/ GP[0]	MMC0_D3/ GP[5]	MMC0_D2/ GP[4]	MMC1_D3/ GP[11]	MMC1_CMD/ I2S1_FS/ GP[7]
K	EM_A[12]/ (CLE)	EM_A[11]/ (ALE)	EM_D[14]	EM_D[13]	EM_D[6]	EM_WAIT3	DV_{DDIO}	V_{SS}	V_{SS}	CV_{DD}	V_{SS}	DV_{DDIO}	V_{SS}	MMC1_D2/ GP[10]
J	EM_A[8]	EM_A[9]	EM_A[20]/ GP[26]	EM_D[15]	DV_{DDEMIF}	CV_{DD}	V_{SS}	V_{SS}	V_{SS}	RSV1	RSV2	USB_VBUS	USB_V_{DD1P3}	USB_DM
H	EM_WE	EM_A[7]	EM_D[7]	EM_WAIT5	DV_{DDEMIF}	V_{SS}	DV_{DDEMIF}	CV_{DD}	USB_ V_{SSA1P3}	USB_ V_{DDA1P3}	USB_ V_{SSA3P3}	USB_ V_{DDA3P3}	USB_V_{SS1P3}	USB_DP
G	EM_WAIT4	EM_A[18]/ GP[24]	EM_D[0]	EM_A[19]/ GP[25]	DV_{DDEMIF}	V_{SS}	V_{SS}	USB_V_{DDPLL}	USB_R1	USB_V_{SSREF}	USB_V_{SSPLL}	USB_V_{DDOSC}	USB_M12XI	USB_M12XO
F	EM_A[6]	EM_A[17]/ GP[23]	EM_D[2]	EM_D[9]	DV_{DDEMIF}	CV_{DD}	DV_{DDIO}	DV_{DDRTC}	V_{SS}	V_{SS}	USB_V_{SSOSC}	USB_LDOO	USB_LDOI	DSP_LDOI
E	EM_A[2]	EM_A[16]/ GP[22]	EM_D[8]	EM_OE	EM_D[1]	DV_{DDEMIF}	INT1	WAKEUP	V_{SS}	DSP_LDOO	V_{SS}	V_{SS}	V_{SS}	V_{SS}
D	EM_A[5]	EM_A[3]	EM_D[10]	EM_D[3]	EM_WAIT2	RESET	V_{SS}	RTC_ CLKOUT	V_{SSA_PLL}	GPAIN0	V_{SS}	DSP_ LDO_EN	DSP_LDO_V	RSV3
C	EM_A[4]	EM_A[1]	EM_CS4	EM_D[11]	EM_CS2	INT0	CLK_SEL	CV_{DDRTC}	V_{SSRTC}	V_{DDA_PLL}	GPAIN3	RSV0	RSV5	RSV4
B	EM_BA[1]	EM_A[0]	RSV10	RSV15	EM_DQM0	EM_R/W	SCL	SDA	RTC_XI	V_{SSA_ANA}	GPAIN2	ANA_LDOI	BG_CAP	V_{SSA_ANA}
A	EM_BA[0]	DV_{DDEMIF}	EM_CS5	RSV11	DV_{DDEMIF}	RSV14	CLKOUT	CLKIN	RTC_XO	V_{DDA_ANA}	GPAIN1	ANA_LDOO	V_{SS}	V_{SS}

A. Shading denotes pins not supported on this device. To ensure proper device operation, these pins must be hooked up properly, see Table 3-19, *Regulators and Power Management Terminal Functions*.

Figure 3-2. VC5505 Pin Map (A)

3.5 Terminal Functions

The terminal functions tables (Table 3-5 through Table 3-22) identify the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed/shared pins, and debugging considerations, see the Device Configuration section of this data manual.

For proper device operation, external pullup/pulldown resistors may be required on some pins. Section 4.8.1, *Pullup/Pulldown Resistors* discusses situations where external pullup/pulldown resistors are required.

Table 3-5. Oscillator/PLL Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE (1)	OTHER (2) (3)	DESCRIPTION
CLKOUT	A7	O/Z	– DV_{DDIO}	DSP clock output signal. For debug purposes, the CLKOUT pin can be used to tap different clocks within the DSP clock generator. The SRC bits in the CLKOUT Control Source Register (CCSSR) can be used to specify the CLKOUT pin source. Additionally, the slew rate of the CLKOUT pin can be controlled by the Output Slew Rate Control Register (OSRCR) [0x1C16]. The CLKOUT pin is enabled/disabled through the CLKOFF bit in the CPU ST3_55 register. When disabled, the CLKOUT pin is placed in high-impedance (Hi-Z). At reset the CLKOUT pin is enabled until the beginning of the boot sequence, when the on-chip Bootloader sets CLKOFF = 1 and the CLKOUT pin is disabled (Hi-Z). For more information on the ST3_55 register, see the *TMS320C55x 3.0 CPU* Reference Guide (literature number: SWPU073).
CLKIN	A8	I	– DV_{DDIO}	Input clock. This signal is used to input an external clock when the 32-KHz on-chip oscillator is not used as the DSP clock (pin CLK_SEL = 1). For boot purposes, the CLKIN frequency is assumed to be either 11.2896, 12, or 12.288 MHz. The CLK_SEL pin (C7) selects between the 32-KHz crystal clock or CLKIN. When the CLK_SEL pin is low, this pin should be tied to ground (V_{SS}). When CLK_SEL is high, this pin should be driven by an external clock source. If CLK_SEL is high, this pin is used as the reference clock for the clock generator and during bootup the bootloader bypasses the PLL and assumes the CLKIN frequency is one of the following frequencies: 11.2896-, 12-, or 12.288-MHz. With these frequencies in mind, the bootloader sets the SPI clock rates at 500 KHz, the I2C clock rate at 400 KHz, and UART at 57600 baud.
CLK_SEL	C7	I	– DV_{DDIO}	Clock input select. This pin selects between the 32-KHz crystal clock or CLKIN. 0 = 32-KHz on-chip oscillator drives the RTC timer and the DSP clock generator while CLKIN is ignored. 1 = CLKIN drives the DSP clock generator and the 32-KHz on-chip oscillator drives only the RTC timer. This pin is ***not*** allowed to change during device operation; it ***must*** be tied high or low at the board.
V_{DDA_PLL}	C10	PWR	see Section 5.2, ROC	1.3-V Analog PLL power supply for the system clock generator.
V_{SSA_PLL}	D9	GND	see Section 5.2, ROC	Analog PLL ground for the system clock generator.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-6. Real-Time Clock (RTC) Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	OTHER(2) (3)	DESCRIPTION
RTC_XO	A9	I	– CV_{DDRTC}	Real-time clock oscillator output. This pin operates at the RTC core voltage, CV_{DDRTC}, and supports a 32.768-kHz crystal. If the RTC oscillator is not used, it can be disabled by connecting RTC_XI to CV_{DDRTC} and RTC_XO to ground (V_{SS}). A voltage must still be applied to CV_{DDRTC} (see Section 5.2, *Recommended Operating Conditions*). **Note:** When RTC oscillator is disabled, the RTC registers (I/O address range 1900h – 197Fh) are not accessible.
RTC_XI	B9	I	– CV_{DDRTC}	Real-time clock oscillator input. If the RTC oscillator is not used, it can be disabled by connecting RTC_XI to CV_{DDRTC} and RTC_XO to ground (V_{SS}). A voltage must still be applied to CV_{DDRTC} (see Section 5.2, *Recommended Operating Conditions*). **Note:** When RTC oscillator is disabled, the RTC registers (I/O address range 1900h – 197Fh) are not accessible.
RTC_CLKOUT	D8	O/Z	– DV_{DDRTC}	Real-time clock output pin. This pin operates at DV_{DDRTC} voltage. The RTC_CLKOUT pin is enabled/disabled through the RTCCLKOUTEN bit in the RTC Power Management Register (RTCPMGT). At reset, the RTC_CLKOUT pin is disabled (high-impedance [Hi-Z]).
WAKEUP	E8	I/O/Z	– DV_{DDRTC}	The pin is used to WAKEUP the core from idle condition. This pin defaults to an input at CV_{DDRTC} powerup, but can also be configured as an active-low open-drain output signal to wakeup an external device from an RTC alarm.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-7. RESET, Interrupts, and JTAG Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	OTHER(2) (3)	DESCRIPTION
RESET				
XF	M8	O/Z	– DV_{DDIO}	External Flag Output. XF is used for signaling other processors in multiprocessor configurations or XF can be used as a fast general-purpose output pin. XF is set high by the BSET XF instruction and XF is set low by the BCLR XF instruction or by writing to bit 13 of the ST1_55 register. At reset, the XF pin will be high. For more information on the ST1_55 register, see the *TMS320C55x 3.0 CPU* Reference Guide (literature number: SWPU073).
$\overline{RESET}$	D6	I	IPU DV_{DDIO}	Device reset. $\overline{RESET}$ causes the DSP to terminate execution and loads the program counter with the contents of the reset vector. When $\overline{RESET}$ is brought to a high level, the reset vector in ROM at FFFF00h forces the program execution to branch to the location of the on-chip ROM bootloader. $\overline{RESET}$ affects the various registers and status bits. The IPU resistor on this pin can be enabled or disabled via the PDINHIBR2 register but will be forced ON when $\overline{RESET}$ is asserted.
JTAG				
[For more detailed information on emulation header design guidelines, see the *XDS560 Emulator* Technical Reference (literature number: SPRU589).]				
TMS	L8	I	IPU DV_{DDIO}	IEEE standard 1149.1 test mode select. This serial control input is clocked into the TAP controller on the rising edge of TCK. If the emulation header is located greater than 6 inches from the device, TMS must be buffered. In this case, the input buffer for TMS needs pullup resistors connected to DV_{DDIO} to hold these signals at a known value when the emulator is not connected. A resistor value of 4.7 kΩ or greater is suggested. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference (literature number: SPRU589). The IPU resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
TDO	M7	O/Z	– DV_{DDIO}	IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance (Hi-Z) state except when the scanning of data is in progress. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference (literature number: SPRU589). If the emulation header is located greater than 6 inches from the device, TDO must be buffered.
TDI	L7	I	IPU DV_{DDIO}	IEEE standard 1149.1 test data input. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. If the emulation header is located greater than 6 inches from the device, TDI must be buffered. In this case, the input buffer for TDI need pull-up resistors connected to DV_{DDIO} to hold these signals at a known value when the emulator is not connected. A resistor value of 4.7 kΩ or greater is suggested. The IPU resistor on this pin can be enabled or disabled via the PDINHIBR2 register.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-7. RESET, Interrupts, and JTAG Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1)	OTHER(2) (3)	DESCRIPTION
TCK	M6	I	IPU DV_{DDIO}	IEEE standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on test access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK. If the emulation header is located greater than 6 inches from the device, TCK must be buffered. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference (literature number: SPRU589). The IPU resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
$\overline{\text{TRST}}$	M9	I	IPD DV_{DDIO}	IEEE standard 1149.1 reset signal for test and emulation logic. $\overline{\text{TRST}}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{\text{TRST}}$ is not connected or driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. The VC5505 will ***not*** operate properly if this reset pin is never asserted low. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference (literature number: SPRU589). It is recommended that an external pulldown resistor be used in addition to the IPD -- especially if there is a long trace to an emulation header.
EMU1	M5	I/O/Z	IPU DV_{DDIO}	Emulator 1 pin. EMU1 is used as an interrupt to or from the emulator system and is defined as input/output by way of the emulation logic. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference (literature number: SPRU589). An external pullup to DV_{DDIO} is required to provide a signal rise time of less than 10 μsec. A 4.7-kΩ resistor is suggested for most applications. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference (literature number: SPRU589). The IPU resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EMU0	L6	I/O/Z	IPU DV_{DDIO}	Emulator 0 pin. When $\overline{\text{TRST}}$ is driven low and then high, the state of the EMU0 pin is latched and used to connect the JTAG pins (TCK, TMS, TDI, TDO) to either the IEEE1149.1 Boundary-Scan TAP (when the latched value of EMU0 = 0) or to the DSP Emulation TAP (when the latched value of EMU0 = 1). Once $\overline{\text{TRST}}$ is high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of the emulation logic. An external pullup to DV_{DDIO} is required to provide a signal rise time of less than 10 μsec. A 4.7-kΩ resistor is suggested for most applications. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference (literature number: SPRU589). The IPU resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EXTERNAL INTERRRUPTS				
$\overline{\text{INT1}}$	E7	I	IPU DV_{DDIO}	External interrupt inputs ($\overline{\text{INT1}}$ and $\overline{\text{INT0}}$). These pins are maskable via their specific Interrupt Mask Register (IMR1, IMR0) and the interrupt mode bit. The pins can be polled and reset by their specific Interrupt Flag Register (IFR1, IFR0). The IPU resistor on these pins can be enabled or disabled via the PDINHIBR2 register.
$\overline{\text{INT0}}$	C6	I	IPU DV_{DDIO}	

Table 3-8. External Memory Interface (EMIF) Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	OTHER(2) (3)	DESCRIPTION
EMIF FUNCTIONAL PINS: ASYNC (NOR, SRAM, and NAND)				
				Note: When accessing 8-bit Asynchronous memory, pins EM_A[20:0] should be connected to memory address pins [22:2] and EM_BA[1:0] should be connected to memory addresss pins [1:0]. For 16-bit Asynchronous memory, pins EM_A[20:0] should be connected to memory address pins [20:1] and EM_BA[1] should be connected to memory addresss pin [0].
EM_A[20]/GP[26]	J3	I/O/Z	IPD DV_{DDEMIF}	This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 20. Mux control via the A20_MODE bit in the EBSR (see Figure 4-2). The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[19]/GP[25]	G4	I/O/Z	IPD DV_{DDEMIF}	This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 19. Mux control via the A19_MODE bit in the EBSR (see Figure 4-2). The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[18]/GP[24]	G2	I/O/Z	IPD DV_{DDEMIF}	This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 18. Mux control via the A18_MODE bit in the EBSR (see Figure 4-2). The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[17]/GP[23]	F2	I/O/Z	IPD DV_{DDEMIF}	This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 17. Mux control via the A17_MODE bit in the EBSR (see Figure 4-2). The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[16]/GP[22]	E2	I/O/Z	IPD DV_{DDEMIF}	This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 16. Mux control via the A16_MODE bit in the EBSR (see Figure 4-2). The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[15]/GP[21]	N1	I/O/Z	IPD DV_{DDEMIF}	This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 15. Mux control via the A15_MODE bit in the EBSR (see Figure 4-2). The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[14]	M1	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 14.
EM_A[13]	L1	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 13.
EM_A[12]/(CLE)	K1	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 12. When interfacing with NAND Flash, this pin also acts as Command Latch Enable (CLE).
EM_A[11]/(ALE)	K2	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 11. When interfacing with NAND Flash, this pin also acts as Address Latch Enable (ALE).
EM_A[10]	L2	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 10.
EM_A[9]	J2	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 9.
EM_A[8]	J1	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 8.
EM_A[7]	H2	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 7.
EM_A[6]	F1	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 6.
EM_A[5]	D1	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 5.
EM_A[4]	C1	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 4.
EM_A[3]	D2	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 3.
EM_A[2]	E1	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 2.
EM_A[1]	C2	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 1.
EM_A[0]	B2	I/O/Z	DV_{DDEMIF}	This pin is the EMIF external address pin 0.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-8. External Memory Interface (EMIF) Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1)	OTHER(2) (3)	DESCRIPTION
EM_D[15]	J4	I/O/Z	DV_{DDEMIF}	EMIF 16-bit bi-directional bus.
EM_D[14]	K3			
EM_D[13]	K4			
EM_D[12]	L3			
EM_D[11]	C4			
EM_D[10]	D3			
EM_D[9]	F4			
EM_D[8]	E3			
EM_D[7]	H3			
EM_D[6]	K5			
EM_D[5]	M2			
EM_D[4]	L4			
EM_D[3]	D4			
EM_D[2]	F3			
EM_D[1]	E5			
EM_D[0]	G3			
EM_CS5	A3	O/Z	DV_{DDEMIF}	EMIF chip select 5 output for use with asynchronous memories (i.e., NOR flash, NAND flash, or SRAM).
EM_CS4	C3	O/Z	DV_{DDEMIF}	EMIF chip select 4 output for use with asynchronous memories (i.e., NOR flash, NAND flash, or SRAM).
EM_CS3	M4	O/Z	DV_{DDEMIF}	EMIF NAND chip select 3 output for use with asynchronous memories (i.e., NOR flash, NAND flash, or SRAM).
EM_CS2	C5	O/Z	DV_{DDEMIF}	EMIF NAND chip select 2 output for use with asynchronous memories (i.e., NOR flash, NAND flash, or SRAM).
EM_WE	H1	O/Z	DV_{DDEMIF}	EMIF asynchronous memory write enable output
EM_OE	E4	O/Z	DV_{DDEMIF}	EMIF asynchronous memory read enable output
EM_R/W	B6	O/Z	DV_{DDEMIF}	EMIF asynchronous read/write output
EM_DQM1	P1	O/Z	DV_{DDEMIF}	EMIF asynchronous data write strobes and byte enables.
EM_DQM0	B5	O/Z	DV_{DDEMIF}	
EM_BA[1]	B1	O/Z	DV_{DDEMIF}	EMIF asynchronous bank address 16-bit wide memory: EM_BA[1] forms the device address[0] and BA[0] forms device address [23]. 8-bit wide memory: EM_BA[1] forms the device address[1] and BA[0] forms device address [0].
EM_BA[0]	A1	O/Z	DV_{DDEMIF}	
EM_WAIT5	H4	I	DV_{DDEMIF}	EMIF wait state extension input 5 for EM_CS5
EM_WAIT4	G1	I	DV_{DDEMIF}	EMIF wait state extension input 4 for EM_CS4
EM_WAIT3	K6	I	DV_{DDEMIF}	EMIF wait state extension input 3 for EM_CS3
EM_WAIT2	D5	I	DV_{DDEMIF}	EMIF wait state extension input 2 for EM_CS2

Table 3-9. Inter-Integrated Circuit (I2C) Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE (1)	OTHER (2) (3)	DESCRIPTION
I2C				
SCL	B7	I/O/Z	DV_{DDIO}	This pin is the I2C clock output. Per the I2C standard, an external pullup is required on this pin.
SDA	B8	I/O/Z	DV_{DDIO}	This pin is the I2C bidirectional data signal. Per the I2C standard, an external pullup is required on this pin.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-10. Inter-IC Sound (I2S0 – I2S3) Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE (1)	OTHER (2) (3)	DESCRIPTION
Interface 0 (I2S0)				
MMC0_D0/ I2S0_DX/ GP[2]	L9	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For I2S, it is I2S0 transmit data output I2S0_DX. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_CLK/ I2S0_CLK/ GP[0]	L10	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For I2S, it is I2S0 clock input/output I2S0_CLK. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_D1/ I2S0_RX/ GP[3]	M10	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For I2S, it is I2S0 receive data input I2S0_RX. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_CMD/ I2S0_FS/ GP[1]	M11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For I2S, it is I2S0 frame synchronization input/output I2S0_FS. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
Interface 1 (I2S1)				
MMC1_D0/ I2S1_DX/ GP[8]	M14	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1, I2S1, and GPIO. For I2S, it is I2S1 transmit data output I2S1_DX. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_CLK/ I2S1_CLK/ GP[6]	M13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1, I2S1, and GPIO. For I2S, it is I2S1 clock input/output I2S1_CLK. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_D1/ I2S1_RX/ GP[9]	M12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1, I2S1, and GPIO. For I2S, it is I2S1 receive data input I2S1_RX. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_CMD/ I2S1_FS/ GP[7]	L14	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed betweenn MMC1, I2S2, and GPIO. For I2S, it is I2S1 frame synchronization input/output I2S1_FS. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-10. Inter-IC Sound (I2S0 – I2S3) Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE[(1)]	OTHER[(2)] [(3)]	DESCRIPTION
Interface 2 (I2S2)				
LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX	P12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For I2S, it is I2S2 transmit data output I2S2_DX. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D8]/ I2S2_CLK/ GP[18]/ SPI_CLK	N10	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For I2S, it is I2S2 clock input/output I2S2_CLK. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX	N11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For I2S, it is I2S2 receive data input I2S2_RX. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	P11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, and GPIO. For I2S, it is I2S2 frame synchronization input/output I2S2_FS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
Interface 3 (I2S3)				
LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	P14	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For I2S, it is I2S3 transmit data output I2S3_DX. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK	N12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For I2S, it is I2S3 clock input/output I2S3_CLK. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	N13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For I2S, it is I2S3 receive data input I2S3_RX. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	P13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For I2S, it is I2S3 frame synchronization input/output I2S3_FS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.

Table 3-11. Serial Peripheral Interface (SPI) Terminal Functions

SIGNAL NAME	NO.	TYPE[(1)]	OTHER[(2)] [(3)]	DESCRIPTION
Serial Port Interface (SPI)				
LCD_CS0_E0/ SPI_CS0	P4	I/O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS0.
LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	P11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS0. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_CS1_E1/ SPI_CS1	N4	I/O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS1.
LCD_RW_WRB/ SPI_CS2	P5	I/O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS2.
LCD_RS/ SPI_CS3	N5	I/O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS3.
LCD_EN_RDB/ SPI_CLK	N3	O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is clock output SPI_CLK.
LCD_D8]/ I2S2_CLK/ GP[18]/ SPI_CLK	N10		IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is clock output SPI_CLK. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[1]/ SPI_TX	N6	I/O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI transmit data output.
LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX	P12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI transmit data output. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[0]/ SPI_RX	P6	I/O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI this pin is SPI receive data input.
LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX	N11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. Mux control via the PPMODE bits in the EBSR. For SPI this pin is SPI receive data input. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-12. UART Terminal Functions

SIGNAL NAME	NO.	TYPE (1)	OTHER (2) (3)	DESCRIPTION
UART				
LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	N13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. When used by UART, it is the receive data input UART_RXD. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	P14	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. In UART mode, it is the transmit data output UART_TXD. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	P13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. In UART mode, it is the clear to send input UART_CTS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK	N12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. In UART mode, it is the ready to send output UART_RTS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-13. USB2.0 Terminal Functions

SIGNAL NAME	NO.	TYPE (1)	OTHER (2) (3)	DESCRIPTION
USB 2.0				
USB_MXI	G13	I	USB_V_{DDOSC}	12-MHz crystal oscillator input. When the USB peripheral ***is not*** used, USB_MXI should be connected to ground (V_{SS}).
USB_MXO	G14	O	USB_V_{DDOSC}	12-MHz crystal oscillator output. When the USB peripheral ***is not*** used, USB_MXO should be left unconnected.
USB_V_{DDOSC}	G12	S	see Section 5.2, ROC	3.3-V power supply for USB oscillator. When the USB peripheral ***is not*** used, USB_V_{DDOSC} should be connected to ground (V_{SS}).
USB_V_{SSOSC}	F11	S	see Section 5.2, ROC	Ground for USB oscillator.
USB_VBUS	J12	A I/O	see Section 5.2, ROC	USB power detect. 5-V input that signifies that VBUS is connected. When the USB peripheral ***is not*** used, the USB_VBUS signal should be connected to ground (V_{SS}).
USB_DP	H14	A I/O	USB_V_{DDA3P3}	USB bi-directional Data Differential signal pair [positive/negative]. When the USB peripheral ***is not*** used, the USB_DP and USB_DM signals should both be tied to ground (V_{SS}).
USB_DM	J14	A I/O	USB_V_{DDA3P3}	
USB_R1	G9	A I/O	USB_V_{DDA3P3}	External resistor connect. Reference current output. This must be connected via a 10-kΩ ±1% resistor to USB_V_{SSREF} and be placed as close to the device as possible. When the USB peripheral ***is not*** used, the USB_R1 signal should be connected via a 10-kΩ resistor to USB_V_{SSREF}.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-13. USB2.0 Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE[1]	OTHER[2] [3]	DESCRIPTION
USB_V_{SSREF}	G10	GND	see Section 5.2, ROC	Ground for reference current. This must be connected via a 10-kΩ ±1% resistor to USB_R1. When the USB peripheral ***is not*** used, the USB_V_{SSREF} signal should be connected directly to ground (V_{ss}).
USB_V_{DDA3P3}	H12	S	see Section 5.2, ROC	Analog 3.3 V power supply for USB PHY. When the USB peripheral ***is not*** used, the USB_V_{DDA3P3} signal should be connected to ground (V_{SS}).
USB_V_{SSA3P3}	H11	GND	see Section 5.2, ROC	Analog ground for USB PHY.
USB_V_{DDA1P3}	H10	S	see Section 5.2, ROC	Analog 1.3 V power supply for USB PHY. [For high-speed sensitive analog circuits] When the USB peripheral ***is not*** used, the USB_V_{DDA1P3} signal should be connected to ground (V_{SS}).
USB_V_{SSA1P3}	H9	GND	see Section 5.2, ROC	Analog ground for USB PHY [For high speed sensitive analog circuits].
USB_V_{DD1P3}	J13	S	see Section 5.2, ROC	1.3-V digital core power supply for USB PHY. When the USB peripheral ***is not*** used, the USB_V_{DD1P3} signal should be connected to ground (V_{SS}).
USB_V_{SS1P3}	H13	GND	see Section 5.2, ROC	Digital core ground for USB phy.
USB_V_{DDPLL}	G8	S	see Section 5.2, ROC	3.3 V USB Analog PLL power supply. When the USB peripheral ***is not*** used, the USB_V_{DDPLL} signal should be connected to ground (V_{SS}).
USB_V_{SSPLL}	G11	GND	see Section 5.2, ROC	USB Analog PLL ground.

Table 3-14. LCD Bridge Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	OTHER(2) (3)	DESCRIPTION
LCD_EN_RDB/ SPI_CLK	N3	O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. For LCD Bridge, this pin is either LCD Bridge read/write enable (MPU68 mode) or read strobe (MPU80 mode). Mux control via the PPMODE bits in the EBSR.
LCD_CS0_E0/ SPI_CS0	P4	I/O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. For LCD Bridge, this pin is either LCD Bridge chip select 0 (MPU68 and MPU80 modes) or enable 0 (HD44780 mode). Mux control via the PPMODE bits in the EBSR.
LCD_CS1_E1/ SPI_CS1	N4	I/O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. For LCD Bridge, this pin is either LCD Bridge chip select 1 (MPU68 and MPU80 modes) or enable 1 (HD44780 mode). Mux control via the PPMODE bits in the EBSR.
LCD_RW_WRB/ SPI_CS2	P5	I/O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. For LCD, this pin is either LCD Bridge read/write select (HD44780 and MPU68 modes) or write strobe (MPU80 mode). Mux control via the PPMODE bits in the EBSR,.
LCD_RS/ SPI_CS3	N5	I/O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. For LCD, this pin is the LCD Bridge address set-up. Mux control via the PPMODE bits in the EBSR.
LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	P14	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For LCD Bridge, it is LCD data pin 15. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	N13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For LCD Bridge, it is LCD data pin 14. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	P13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For LCD Bridge, it is LCD data pin 13. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK	N12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, and GPIO. For LCD Bridge, it is LCD data pin 12. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX	P12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For LCD Bridge, it is LCD data pin 11. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX	N11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For LCD Bridge, it is LCD data pin 10. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	P11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For LCD Bridge, it is LCD data pin 9. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[8]/ I2S2_CLK GP[18]/ SPI_CLK	N10	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For LCD Bridge, it is LCD data pin 8. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[7]/ GP[17]	P10	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For LCD Bridge, it is LCD data pin 7. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-14. LCD Bridge Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE[(1)]	OTHER[(2) (3)]	DESCRIPTION
LCD_D[6]/ GP[16]	N9	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For LCD Bridge, it is LCD data pin 6. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[5]/ GP[15]	P9	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For LCD Bridge, it is LCD data pin 5. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[4]/ GP[14]	N8	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For LCD Bridge, it is LCD data pin 4. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[3]/ GP[13]	N7	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For LCD Bridge, it is LCD data pin 3. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[2]/ GP[12]	P7	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For LCD Bridge, it is LCD data pin 2. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[1]/ SPI_TX	N6	I/O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. For LCD Bridge, it is LCD data pin 1. Mux control via the PPMODE bits in the EBSR.
LCD_D[0]/ SPI_RX	P6	I/O/Z	DV_{DDIO}	This pin is multiplexed between LCD Bridge and SPI. For LCD Bridge, it is LCD data pin 0. Mux control via the PPMODE bits in the EBSR.

Table 3-15. MMC1/SD Terminal Functions

SIGNAL NAME	NO.	TYPE(1)	OTHER(2) (3)	DESCRIPTION
MMC/SD				
MMC1_CLK/ I2S1_CLK/ GP[6]	M13	O	IPD DV_{DDIO}	This pin is multiplexed between MMC1, I2S1, and GPIO. For MMC/SD, this is the MMC1 data clock output MMC1_CLK. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_CMD/ I2S1_FS/ GP[7]	L14	O	IPD DV_{DDIO}	This pin is multiplexed between MMC1, I2S1, and GPIO. For MMC/SD, this is the MMC1 command I/O output MMC1_CMD. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_D3/ GP[11]	L13	I/O/Z	IPD DV_{DDIO}	The MMC1_D3 and MMC1_D2 pins are multiplexed between MMC1 and GPIO. The MMC1_D1 and MMC1_D0 pins are multiplexed between MMC1, I2S1, and GPIO. In MMC/SD mode, all these pins are the MMC1 nibble wide bi-directional data bus. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on these pins can be enabled or disabled via the PDINHIBR1 register.
MMC1_D2/ GP[10]	K14	I/O/Z	IPD DV_{DDIO}	
MMC1_D1/ I2S1_RX/ GP[9]	M12	I/O/Z	IPD DV_{DDIO}	
MMC1_D0/ I2S1_DX/ GP[8]	M14	I/O/Z	IPD DV_{DDIO}	

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-16. MMC0/SD Terminal Functions

SIGNAL NAME	NO.	TYPE(1)	OTHER(2) (3)	DESCRIPTION
MMC/SD				
MMC0_CLK/ I2S0_CLK/ GP[0]	L10	O	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For MMC/SD, this is the MMC0 data clock output MMC0_CLK. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_CMD/ I2S0_FS/ GP[1]	M11	O	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For MMC/SD, this is the MMC0 command I/O output MMC0_CMD. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_D3/ GP[5]	L11	I/O/Z	IPD DV_{DDIO}	The MMC0_D3 and MMC0_D2 pins are multiplexed between MMC0 and GPIO. The MMC0_D1 and MMC0_D0 pins are multiplexed between MMC0, I2S0, and GPIO. In MMC/SD mode, these pins are the MMC0 nibble wide bi-directional data bus. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on these pins can be enabled or disabled via the PDINHIBR1 register.
MMC0_D2/ GP[4]	L12	I/O/Z	IPD DV_{DDIO}	
MMC0_D1/ I2S0_RX/ GP[3]	M10	I/O/Z	IPD DV_{DDIO}	
MMC0_D0/ I2S0_DX/ GP[2]	L9	I/O/Z	IPD DV_{DDIO}	

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-17. 10-Bit SAR ADC Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE[(1)]	OTHER[(2) (3)]	DESCRIPTION
SAR ADC				
GPAIN0	D10	I/O	V_{DDA_ANA}	GPAIN0: General -Purpose Output and Analog Input pin 0. This pin is demuxed internally into ADC Channels 0, 1, & 2. GPAIN0 can also be used as a general-purpose open-drain output. This pin is unique among the GPAIN pins in that it is the only pin that is 3.6 V-tolerant to support measuring a battery voltage. GPAIN0 can accommodate input voltages from 0 V to 3.6 V; although, the ADC is unable to accept signals greater than V_{DDA_ANA} without clamping. ADC Channel 1 is capable of switching in an internal resistor divider that has a divide ratio of approximately 1/8.
GPAIN1	A11	I/O	V_{DDA_ANA}	GPAIN1: General -Purpose Output and Analog Input pin 1. This pin is connected to ADC Channel 3. GPAIN1 can be used as a general-purpose output if certain requirements are met (see Note: below). GPAIN1 can accommodate input voltages from 0 V to V_{DDA_ANA}. Note: If the ANA_LDO is used to supply power to V_{DDA_ANA}, this pin must ***not*** be used as a general-purpose output (driving high) since the max current capability (see the I_{SD} parameter in Section 5.3, *Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature*) of the ANA_LDO can be exceeded. Doing so may result in the on-chip power-on reset (POR) resetting the chip.
GPAIN2	B11	I/O	V_{DDA_ANA}	GPAIN2: General -Purpose Output and Analog Input pin 2. This pin is connected to ADC Channel 4. GPAIN2 can be used as a general-purpose output if certain requirements are met (see Note: below). GPAIN2 can accommodate input voltages from 0 V to V_{DDA_ANA}. Note: If the ANA_LDO is used to supply power to V_{DDA_ANA}, this pin must ***not*** be used as a general-purpose output (driving high) since the max current capability (see the I_{SD} parameter in Section 5.3, *Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature*) of the ANA_LDO can be exceeded. Doing so may result in the on-chip POR resetting the chip.
GPAIN3	C11	I/O	V_{DDA_ANA}	GPAIN3: General -Purpose Output and Analog Input pin 3. This pin is connected to ADC Channel 5. GPAIN3 can be used as a general-purpose output if certain requirements are met (see Note: below). GPAIN3 can accommodate input voltages from 0 V to V_{DDA_ANA}. Note: If the ANA_LDO is used to supply power to V_{DDA_ANA}, this pin must ***not*** be used as a general-purpose output (driving high) since the max current capability (see the I_{SD} parameter in Section 5.3, *Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature*) of the ANA_LDO can be exceeded. Doing so may result in the on-chip POR resetting the chip.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-18. GPIO Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	OTHER(2) (3)	DESCRIPTION
General-Purpose Input/Output				
XF	M8	O/Z	– DV_{DDIO}	External Flag Output. XF is used for signalling other processors in multiprocessor configurations or XF can be used as a fast general-purpose output pin. XF is set high by the BSET XF instruction and XF is set low by the BCLR XF instruction or by writing to bit 13 of the ST1_55 register. At reset, the XF pin will be high. For more information on the ST1_55 register, see the *TMS320C55x 3.0 CPU* Reference Guide (literature number: SWPU073).
MMC0_CLK/ I2S0_CLK/ GP[0]	L10	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For GPIO, it is general-purpose input/output pin 0 (GP[0]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_CMD/ I2S0_FS/ GP[1]	M11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For GPIO, it is general-purpose input/output pin 1 (GP[1]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_D0/ I2S0_DX/ GP[2]	L9	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For GPIO, it is general-purpose input/output pin 2 (GP[2]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_D1/ I2S0_RX/ GP[3]	M10	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0, I2S0, and GPIO. For GPIO, it is general-purpose input/output pin 3 (GP[3]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_D2/ GP[4]	L12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0 and GPIO. For GPIO, it is general-purpose input/output pin 4 (GP[4]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC0_D3/ GP[5]	L11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC0 and GPIO. For GPIO, it is general-purpose input/output pin 5 (GP[5]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_CLK/ I2S1_CLK/ GP[6]	M13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1, I2S1, and GPIO. For GPIO, it is general-purpose input/output pin 6 (GP[6]). Mux control via the SP1MODE bits in the EBSR.
MMC1_CMD/ I2S1_FS/ GP[7]	L14	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1, I2S1, and GPIO. For GPIO, it is general-purpose input/output pin 7 (GP[7]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_D0/ I2S1_DX/ GP[8]	M14	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1, I2S1, and GPIO. For GPIO, it is general-purpose input/output pin 8 (GP[8]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_D1/ I2S1_RX/ GP[9]	M12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1, I2S1, and GPIO. For GPIO, it is general-purpose input/output pin 9 (GP[9]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_D2/ GP[10]	K14	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1 and GPIO. For GPIO, it is general-purpose input/output pin 10 (GP[10]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.
MMC1_D3/ GP[11]	L13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between MMC1 and GPIO. For GPIO, it is general-purpose input/output pin 11 (GP[11]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-18. GPIO Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1)	OTHER(2) (3)	DESCRIPTION
LCD_D[2]/ GP[12]	P7	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 12 (GP[12]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[3]/ GP[13]	N7	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 13 (GP[13]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[4]/ GP[14]	N8	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 14 (GP[14]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[5]/ GP[15]	P9	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 15 (GP[15]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[6]/ GP[16]	N9	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 16 (GP[16]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[7]/ GP[17]	P10	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 17 (GP[17]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D8]/ I2S2_CLK/ GP[18]/ SPI_CLK	N10	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 18 (GP[18]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	P11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, and GPIO. For GPIO, it is general-purpose input/output pin 19 (GP[19]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX	N11	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIOand SPI. For GPIO, it is general-purpose input/output pin 20 (GP[20]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
EM_A[15]/GP[21]	N1	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 21 (GP[21]). Mux control via the A15_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[16]/GP[22]	E2	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 22 (GP[22]). Mux control via the A16_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[17]/GP[23]	F2	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 23 (GP[23]). Mux control via the A17_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[18]/GP[24]	G2	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 24 (GP[24]). Mux control via the A18_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[19]/GP[25]	G4	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 25 (GP[25]). Mux control via the A19_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.
EM_A[20]/GP[26]	J3	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 26 (GP[26]). Mux control via the A20_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register.

Table 3-18. GPIO Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1)	OTHER(2) (3)	DESCRIPTION
LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX	P12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For GPIO, it is general-purpose input/output pin 27 (GP[27]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK	N12	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 28 (GP[28]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	P13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 29 (GP[29]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	N13	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 30 (GP[30]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.
LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	P14	I/O/Z	IPD DV_{DDIO}	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 31 (GP[31]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.

Table 3-19. Regulators and Power Management Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE[1]	OTHER[2] [3]	DESCRIPTION
				Regulators
DSP_LDOO	E10	S		[***Not supported on this device. Reserved for compatibility with future devices]***. For proper device operation, this pin ***must*** be connected to an ~ 1.0 µF decoupling capacitor to V_{SS}. For more detailed information, see Section 6.3.3, *Power-Supply Decoupling*.
DSP_LDOI	F14	S		[***Not supported on this device. Reserved for compatibility with future devices]***. For proper device operation, this pin ***must*** be connected to the same supply as the ANA_LDOI pin (B12).
$\overline{\text{DSP\_LDO\_EN}}$	D12	I	– ANA_LDOI	[***Not supported on this device. Reserved for compatibility with future devices]***. For proper device operation, this pin ***must*** be tied to ground (V_{SS}). For future device family pin compatibility, board designs should have this pin layout with a zero-Ω resistor to ANA_LDOI and a zero-Ω resistor to ground. For VC5505 , only the zero-Ω resistor to ground should be populated.
DSP_LDO_V	D13	I	– ANA_LDOI	[***Not supported on this device. Reserved for compatibility with future devices]***. For proper device operation, this pin ***must*** be connected to the same supply as the ANA_LDOI pin (B12). For future device family pin compatibility, board designs should have this pin layout with a zero-Ω resistor to ANA_LDOI and a zero-Ω resistor to ground. For VC5505 , only the zero-Ω resistor to ANA_LDOI should be populated.
USB_LDOO	F12	S		[***Not supported on this device. Reserved for compatibility with future devices]***. For proper device operation, this pin ***must*** be left unconnected.
USB_LDOI	F13	S		[***Not supported on this device. Reserved for compatibility with future devices]***. For proper device operation, this pin ***must*** be connected to the same supply as the ANA_LDOI pin (B12).
ANA_LDOO	A12	S		Analog LDO output. This output provides up to 3 mA of current regulated to 1.3 V (see the I_{SD} parameter in Section 5.3, *Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature*). For proper device operation, this pin ***must*** be connected to an ~ 1.0 µF decoupling capacitor to V_{SS}. For more detailed information, see Section 6.3.3, *Power-Supply Decoupling*.
ANA_LDOI	B12	S		Analog LDO input. This input pin must be connected to a power supply with a voltage range of 1.8 V to 3.6 V. It supplies power for the ANA_LDO, the bandgap reference generator circuits, and is the I/O supply for some input pins.
BG_CAP	B13	O		Bandgap reference filter signal. For proper device operation, this pin needs to be bypassed with a 0.1 µF capacitor to analog ground (V_{SSA_ANA}). This external capacitor provides filtering for stable reference voltages & currents generated by the bandgap circuit. The bandgap produces the references for use by the System PLL, SAR, and POR circuits.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-20. Reserved and No Connects Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	OTHER(2) (3)	DESCRIPTION
Reserved				
RSV0	C12	I	– ANA_LDOI	Reserved. For proper device operation, this pin must be tied directly to V_{SS}.
RSV1	J10	PWR		Reserved. For proper device operation, this pin must be tied directly to CV_{DD}.
RSV2	J11	PWR		Reserved. For proper device operation, this pin must be tied directly to CV_{DD}.
RSV3	D14	I	– ANA_LDOI	Reserved. For proper device operation, this pin must be tied directly to V_{SS}.
RSV4	C14	I	– ANA_LDOI	Reserved. For proper device operation, this pin must be tied directly to V_{SS}.
RSV5	C13	I	– ANA_LDOI	Reserved. For proper device operation, this pin must be tied directly to V_{SS}.
RSV10	B3	O/Z	DV_{DDEMIF}	Reserved. (Leave unconnected, do not connect to power or ground).
RSV11	A4	O/Z	DV_{DDEMIF}	Reserved. (Leave unconnected, do not connect to power or ground).
RSV12	M3	O/Z	DV_{DDEMIF}	Reserved. (Leave unconnected, do not connect to power or ground).
RSV13	N2	O/Z	DV_{DDEMIF}	Reseverd. (Leave unconnected, do not connect to power or ground).
RSV14	A6	O/Z	DV_{DDEMIF}	Reserved. (Leave unconnected, do not connect to power or ground).
RSV15	B4	O/Z	DV_{DDEMIF}	Reseverd. (Leave unconnected, do not connect to power or ground).

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-21. Supply Voltage Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	OTHER(2) (3)	DESCRIPTION
SUPPLY VOLTAGES				
CV_{DD}	F6, H8, J6, K10, L5	PWR		1.05-V Digital Core supply voltage (60 MHz) 1.3-V Digital Core supply voltage (100 MHz)
DV_{DDIO}	F7, K7, K12, N14, P3, P8	PWR		1.8-V, 2.5-V, 2.8-V, or 3.3-V I/O power supply for non-EMIF and non-RTC I/Os

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

Table 3-21. Supply Voltage Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE[1]	OTHER[2] [3]	DESCRIPTION
DV_{DDEMIF}	A2, A5, E6, F5, G5, H5, H7, J5, P2	PWR		1.8-V, 2.5-V, 2.8-V, or 3.3-V EMIF I/O power supply
CV_{DDRTC}	C8	PWR		1.05-V thru 1.3-V RTC digital core and RTC oscillator power supply.
DV_{DDRTC}	F8	PWR		1.8-V, 2.5-V, 2.8-V, or 3.3-V I/O power supply for RTC_CLOCKOUT and WAKEUP pins.
V_{DDA_ANA}	A10	PWR		1.3-V supply for power management and 10-bit SAR ADC

Table 3-22. Ground Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE[1]	OTHER[2] [3]	DESCRIPTION
V_{SS}	A13, A14, D7, D11, E9, E11, E12, E13, E14, F9, F10, G6, G7, H6, J7, J8, J9, K8, K9, K11, K13	GND		Ground pins
V_{SS_RTC}	C9	GND		Ground pin for RTC digital core and RTC oscillator power supply.
V_{SSA_ANA}	B10	GND		Ground pins for power management (POR & Bandgap circuits) and 10-bit SAR ADC
V_{SSA_ANA}	B14	GND		Ground pins for power management (POR & Bandgap circuits) and 10-bit SAR ADC

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1 , *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

3.6 Device Support

3.6.1 Development Support

TI offers an extensive line of development tools for the TMS320C55x DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of TMS320C55x fixed-point DSP-based applications:

Software Development Tools:

Code Composer Studio™ Integrated Development Environment (IDE): Version 3.3 or later

C/C++/Assembly Code Generation, and Debug plus additional development tools

Scalable, Real-Time Foundation Software (DSP/BIOS™ Version 5.32.03 or later), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools:

Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the TMS320C55x DSP platform, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

3.6.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g.,TMX320VC5505ZCH). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully-qualified production device.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZCH), and the temperature range (for example, "Blank" is the commercial temperature range).

Figure 3-3 provides a legend for reading the complete device name for any DSP platform member.

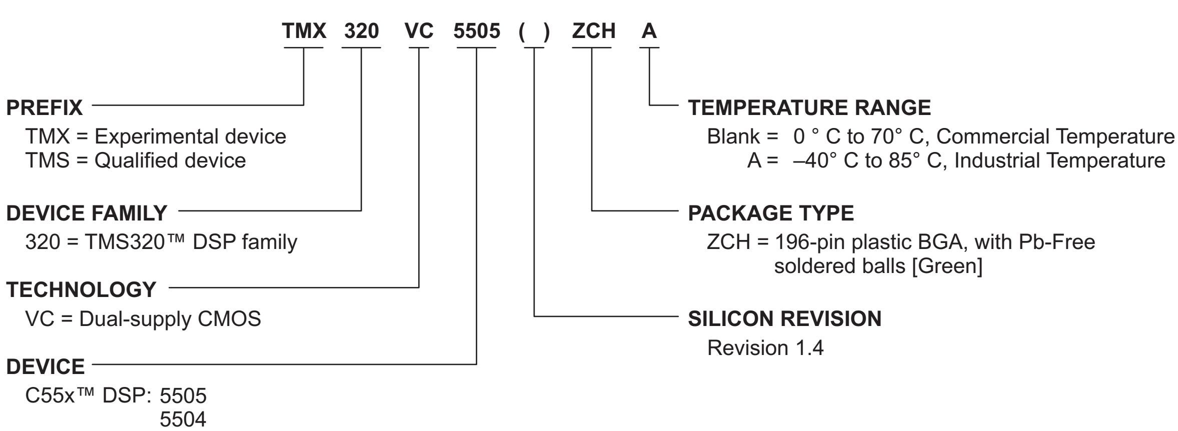


Figure 3-3. TMS320VC5505 Device Nomenclature

4 Device Configuration

4.1 System Registers

The system registers are used to configure the device and monitor its status. Brief descriptions of the various system registers are shown in Table 4-1.

Table 4-1. Idle Control, Status, and System Registers

CPU WORD ADDRESS	ACRONYM	Register Description	COMMENTS
0001h	ICR	Idle Control Register	
0002h	ISTR	Idle Status Register	
1C00h	EBSR	External Bus Selection Register	see Section 4.6.1 of this document.
1C02h	PCGCR1	Peripheral Clock Gating Control Register 1	
1C03h	PCGCR2	Peripheral Clock Gating Control Register 2	
1C04h	PSRCR	Peripheral Software Reset Counter Register	
1C05h	PRCR	Peripheral Reset Control Register	
1C14h	TIAFR	Timer Interrupt Aggregation Flag Register	
1C16h	ODSCR	Output Drive Strength Control Register	
1C17h	PDINHIBR1	Pull-Down Inhibit Register 1	
1C18h	PDINHIBR2	Pull-Down Inhibit Register 2	
1C19h	PDINHIBR3	Pull-Down Inhibit Register 3	
1C1Ah	DMA0CESR1	DMA0 Channel Event Source Register 1	
1C1Bh	DMA0CESR2	DMA0 Channel Event Source Register 2	
1C1Ch	DMA1CESR1	DMA1 Channel Event Source Register 1	
1C1Dh	DMA1CESR2	DMA1 Channel Event Source Register 2	
1C26h	ECDR	EMIF Clock Divider Register	
1C28h	RAMSLPMDCNTLR1	RAM Sleep Mode Control Register 1	
1C2Eh	RAMSLPMDCNTLR2	RAM Sleep Mode Control Register 2	
1C30h	DMAIFR	DMA Interrupt Flag Register	
1C31h	DMAIER	DMA Interrupt Enable Register	
1C32h	USBSCR	USB System Control Register	
1C33h	ESCR	EMIF System Control Register	
1C36h	DMA2CESR1	DMA2 Channel Event Source Register 1	
1C37h	DMA2CESR2	DMA2 Channel Event Source Register 2	
1C38h	DMA3CESR1	DMA3 Channel Event Source Register 1	
1C39h	DMA3CESR2	DMA3 Channel Event Source Register 2	
1C3Ah	CLKSTOP	Peripheral Clock Stop Request/Acknowledge Register	
7004h	USBLDOCNTL	USB LDO Control Register	[***Not Supported***]

4.2 Power Considerations

The VC5505 provides several means of managing power consumption.

To minimize power consumption, the VC5505 divides its circuits into eight main isolated supply domains:

- ANA_LDOI (LDO and Bandgap Power Supply)
- Analog POR and PLL (V_{DDA_ANA} and V_{DDA_PLL})
- RTC (CV_{DD_RTC})
- Digital Core (CV_{DD})
- USB Core (USB_ V_{DD1P3} and USB_V_{DDA1P3})
- USB PHY and USB PLL (USB_V_{DDOSC}, USB_V_{DDA3P3}, and USB_V_{DDPLL})
- EMIF I/O (DV_{DDEMIF})
- RTC I/O (DV_{DDRTC})
- Rest of the I/O (DV_{DDIO})

4.2.1 LDO Configuration

The VC5505 includes one Low-Dropout Regulator (LDO) which can be used to regulate the supplies of the analog PLL and SAR ADC.

4.2.1.1 Analog LDO

The ANA_LDOI pin (B12) provides the power to the Analog LDO, the bandgap reference generator, and some I/O input pins and can range from 1.8 V to 3.6 V. The Bandgap provides accurate voltage and current references to the POR, LDO, PLL, and SAR; therefore, for proper device operation, power **must** always be applied to the ANA_LDOI pin. ANA_LDOO is regulated to 1.3 V and can optionally be used to provide up to 3 mA to the V_{DDA_ANA} (Power Management Voltage Supervisor and SAR V_{DD} power inputs) and V_{DDA_PLL} (System PLL power input).

4.3 Clock Considerations

The system clock, which is used by the CPU and most of the DSP peripherals, is controlled by the system clock generator. The system clock generator features a software-programmable PLL multiplier and several dividers. The clock generator accepts an input reference clock from the CLKIN pin or the output clock of the 32.768-KHz real-time clock (RTC) oscillator. The selection of the input reference clock is based on the state of the CLK_SEL pin. The CLK_SEL pins is required to be statically tied high or low and cannot change dynamically after reset.

In addition, the DSP requires a reference clock for USB applications. The USB reference clock is generated using a dedicated on-chip oscillator with a 12-MHz external crystal connected to the USB_MXI and USB_MXO pins.

The USB reference clock is not required if the USB peripheral is not being used. To completely disable the USB oscillator, connect the USB_MXI pin to ground (V_{SS}) and leave the USB_MXO pin unconnected. The USB oscillator power pins (USB_V_{DDOSC} and USB_V_{SSOSC}) should also be connected to ground.

The RTC oscillator generates a clock when a 32.768-KHz crystal is connected to the RTC_XI and RTC_XO pins. The 32.768-KHz crystal can be disabled if CLKIN is used as the clock source for the DSP. However, when the RTC oscillator is disabled, the RTC peripheral will not operate and the RTC registers (I/O address range 1900h – 197Fh) will not be accessible. This includes the RTC power management register (RTCPMGT) which controls the RTCLKOUT and WAKEUP pins. To disable the RTC oscillator, connect the RTC_XI pin to CV_{DDRTC} and the RTC_XO pin to ground.

For more information on crystal specifications for the RTC oscillator and the USB oscillator, see Section 6.4, *External Clock Input From RTC_XI, CLKIN, and USB_MXI Pins*.

4.3.1 Clock Configurations After Device Reset

After reset, the on-chip Bootloader programs the system clock generator based on the input clock selected via the CLK_SEL pin. If CLK_SEL = 0, the Bootloader programs the system clock generator and sets the system clock to 12.288 MHz (multiply the 32.768-kHz RTC oscillator clock by 375). If CLK_SEL = 1, the Bootloader bypasses the system clock generator altogether and the system clock is driven by the CLKIN pin. In this case, the CLKIN frequency is expected to be 11.2896 MHz, 12.0 MHz, or 12.288 MHz. While the bootloader tries to boot from the USB (*currently not supported*), the clock generator will be programmed to output approximately 36 MHz.

4.3.1.1 Device Clock Frequency

After the boot process is complete, the user is allowed to re-program the system clock generator to bring the device up to the desired clock frequency and the desired peripheral clock state (clock gating or not). The user must adhere to various clock requirements when programming the system clock generator. For more information, see Section 6.5, *Clock PLLs*.

Note: The on-chip Bootloader allows for DSP registers to be configured during the boot process. However, this feature ***must not*** be used to change the output frequency of the system clock generator during the boot process. Timer0 is also used by the bootloader to allow for 200 ms of BG_CAP settling time. The bootloader register modification feature ***must not*** modify the Timer0 registers.

4.3.1.2 Peripheral Clock State

The clock and reset state of each of peripheral is controlled through a set of system registers. The peripheral clock gating control registers (PCGCR1 and PCGCR2) are used to enable and disable peripheral clocks. The peripheral software reset counter register (PSRCR) and the peripheral reset control register (PRCR) are used to assert and deassert peripheral reset signals.

At hardware reset, all of the peripheral clocks are off to conserve power. After hardware reset, the DSP boots via the bootloader code in ROM. During the boot process, the bootloader queries each peripheral to determine if it can boot from that peripheral. At that time, the individual peripheral clocks will be enabled for the query and then disabled again when the bootloader is finished with the peripheral. By the time the bootloader releases control to the user code, all peripheral clocks will be off and all domains in the ICR, except the CPU domain, will be idled.

4.3.1.3 USB Oscillator Control

The USB oscillator is controlled through the USB system control register (USBSCR). To enable the oscillator, the USBOSCDIS and USBOSCBIASDIS bits must be cleared to 0. The user must wait until the USB oscillator stabilizes before proceeding with the USB configuration. The USB oscillator stabilization time is 100 μs, typically with a 10 ms maximum (**Note:** the startup time is highly dependent on the ESR and capacitive load on the crystal).

4.4 Boot Sequence

The boot sequence is a process by which the device's memory is loaded with program and data sections from external flash memory, and by which some of the device's internal registers are programmed with predetermined values. The boot sequence is started automatically after each device reset. For more details on device reset, see Section 6.7, *Reset.*

There are several methods by which the memory and register initialization can take place. Each of these methods is referred to as a boot mode. At reset, the device cycles through different boot modes until a valid boot signature is found (see Figure 4-1). For more information on the boot modes supported, see Section 4.4.1, *Boot Modes*.

The VC5505 Bootloader follows the following steps as shown in Figure 4-1

1. Immediately after reset, the CPU fetches the reset vector from 0xFFFF00. MP/$\overline{\text{MC}}$ is 0 by default, so 0xFFFF00 is mapped to internal ROM. The PLL is in bypass mode.
2. Set CLKOUT slew rate control to slow slew rate.
3. Idle all peripherals, MPORT and HWA.
4. If CLK_SEL = 0, the Bootloader powers up the PLL and sets its output frequency to 12.288 MHz (with a 375x multiplier using VP = 749, VS = 0, input divider disabled, output divide-by-2 enabled, and output divider enabled with VO = 0). If CLK_SEL = 1, the Bootloader keeps the PLL bypassed.
5. Apply manufacturing trim to the bandgap references.
6. Disable CLKOUT.
7. Set Register Configuration, if present in boot image.
8. Test for NOR boot on all asynchronous CS spaces ($\overline{\text{EM\_CS[2:5]}}$) with 16-bit access:
   (a) Check the first 2 bytes read from boot signature.
   (b) If the boot signature is not valid, go to step 9.
   (c) Attempt NOR boot, go to step 17.
9. Test for NAND boot on all asynchronous CS spaces ($\overline{\text{EM\_CS[2:5]}}$) with 8-bit access:
   (a) Check the first 2 bytes read from boot table for a boot signature match.
   (b) If the boot signature is not valid, go to step 10.
   (c) Attempt NAND boot, go to step 17.
10. Test for SPI EEPROM boot on SPI_CS[0] with 500-KHz clock rate and for Parallel Port Mode on External bus Selection Register set to 5, then set to 6:
   (a) Check the first 2 bytes read from boot table for a boot signature match.
   (b) If the boot signature is not valid, go to step 11.
   (c) Attempt SPI EEPROM boot, go to step 17.
11. Test for I2C EEPROM boot with a 7-bit slave address 0x50 and 400-kHz clock rate.
   (a) Check the first 2 bytes read from boot table for a boot signature match.
   (b) If the boot signature is not valid, go to step 12.
   (c) Attempt I2C EEPROM boot, go to step 17.
12. Test for MMC/SD boot --- ***MMC/SD boot is not supported.***
13. Set the PLL output to approximately 36 MHz. If CLK_SEL = 1, CLKIN multiplied by 3x, ; if CLK_SEL = 0, CLKIN is multiplied by 1125x.
14. Test for UART boot --- ***UART boot is not supported.***
15. Test for USB boot --- ***USB boot is not supported.***
16. If the boot signature is ***not*** valid, then go back to step 14 and repeat.
17. Enable TIMER0 to start counting 200 ms.
18. Ensure a minimum of 200 ms has elapsed since step 17 before proceeding to execute the bootloaded code.
19. Jump to the entry point specified in the boot image.

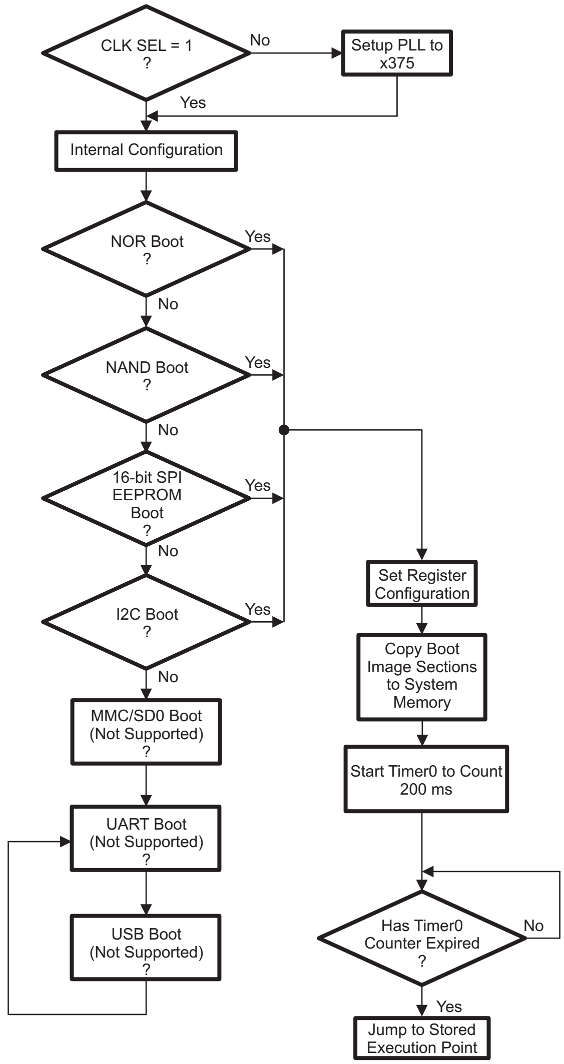


Figure 4-1. Bootloader Software Architecture

4.4.1 Boot Modes

The VC5505 DSP supports the following boot modes in the following device order: NOR Flash, NAND Flash, 16-bit SPI EEPROM, and I2C EEPROM. The boot mode is determined by checking for a valid boot signature on each supported boot device. The first boot device with a valid boot signature will be used to load and execute the user code. If none of the supported boot devices have a valid boot signature, the Bootloader goes into an endless loop checking the unsupported UART and USB boot modes and the device must be reset to look for another valid boot image in the supported boot modes.

4.4.2 Boot Configuration

After reset, the on-chip Bootloader programs the system clock generator based on the input clock selected via the CLK_SEL pin. If CLK_SEL = 0, the Bootloader programs the system clock generator and sets the system clock to 12.288 MHz (multiply the 32.768-KHz RTC oscillator clock by 375). If CLK_SEL = 1, the Bootloader bypasses the system clock generator altogether and the system clock is driven by the CLKIN pin.

Note:

- When CLK_SEL =1, the CLKIN frequency is expected to be 11.2896 MHz, 12.0 MHz, or 12.288 MHz.
- The on-chip Bootloader allows for DSP registers to be configured during the boot process. However, this feature must not be used to change the output frequency of the system clock generator during the boot process. Timer0 is also used by the bootloader to allow for 200 ms of BG_CAP settling time. The bootloader register modification feature ***must not*** modify the Timer0 registers.

At hardware reset, all of the peripheral clocks are "off" to conserve power. After hardware reset, the DSP boots via the bootloader code in ROM. During the boot process, the bootloader queries each peripheral to determine if it can boot from that peripheral. At that time, the individual peripheral clocks will be enabled for the query and then disabled again when the bootloader is finished with the peripheral. By the time the bootloader releases control to the user code, all peripheral clocks will be "off" and all domains in the ICR, except the CPU domain, will be idled.

4.4.3 DSP Resources Used By the Bootloader

The Bootloader uses SARAM block 31 for the storing of temporary data. This block of memory is reserved during the boot process. However, after the boot process is complete, it can be used by the user application.

4.5 Configurations at Reset

Some device configurations are determined at reset. The following subsections give more details.

4.5.1 *Device and Peripheral Configurations at Device Reset*

Table 4-2 summarizes the device boot and configuration pins that are required to be statically tied high, tied low, or left unconnected during device operation. For proper device operation, a device reset should be initiated after changing any of these pin functions.

Table 4-2. Default Functions Affected by Device Configuration Pins

CONFIGURATION PINS	SIGNAL NO.	IPU/IPD	FUNCTIONAL DESCRIPTION
DSP_LDO_EN	D12	–	[***Not supported on this device. Reserved for compatibility with future devices]***. For proper device operation, this pin ***must*** be connected to ground (V_{SS}). For future device family pin compatibility, board designs should have this pin layout with a zero-Ω resistor to ANA_LDOI and a zero-Ω resistor to ground. For VC5505 , only the zero-Ω resistor to ground should be populated.
DSP_LDO_V	D13	–	[***Not supported on this device. Reserved for compatibility with future devices]***. For proper device operation, this pin ***must*** be connected to the same supply as the ANA_LDOI pin (B12). For future device family pin compatibility, board designs should have this pin layout with a zero-Ω resistor to ANA_LDOI and a zero-Ω resistor to ground. For VC5505 , only the zero-Ω resistor to ANA_LDOI should be populated.
CLK_SEL	C7	–	Clock input select. 0 = 32-KHz on-chip oscillator drives the RTC timer and the DSP clock generator while CLKIN is ignored. 1 = CLKIN drives the DSP clock generator and the 32-KHz on-chip oscillator drives only the RTC timer. This pin is ***not*** allowed to change during device operation; it ***must*** be tied high or low at the board.

For proper device operation, external pullup/pulldown resistors may be required on these device configuration pins. For discussion situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.

This device also has RESERVED pins that need to be configured correctly for proper device operation (statically tied high, tied low, or left unconnected at all times). For more details on these pins, see Table 3-20, *Reserved and No Connects Terminal Functions*.

4.6 Configurations After Reset

The following sections provide details on configuring the device after reset. Multiplexed pin functions are selected by software after reset. For more details on multiplexed pin function control, see Section 4.7, *Multiplexed Pin Configurations*.

4.6.1 *External Bus Selection Register (EBSR)*

The External Bus Selection Register (EBSR) determines the mapping of the LCD controller, I2S2, I2S3, UART, SPI, and GPIO signals to 21 signals of the external parallel port pins. It also determines the mapping of the I2S or MMC/SD ports to serial port 1 pins and serial port 2 pins. The EBSR register is located at port address 0x1C00. Once the bit fields of this register are changed, the routing of the signals takes place on the next CPU clock cycle.

Additionally, the EBSR controls the function of the upper bits of the EMIF address bus. Pins EM_A[20:15] can be individually configured as GPIO pins through the Axx_MODE bits. When Axx_MODE = 1, the EM_A[xx] pin functions as a GPIO pin. When Axx_MODE = 0, the EM_A[xx] pin retains its EMIF functionality.

Before modifying the values of the external bus selection register, you must clock gate all affected peripherals through the Peripheral Clock Gating Control Register . After the external bus selection register has been modified, you must reset the peripherals before using them through the Peripheral Software Reset Counter Register.

After the boot process is complete, the external bus selection register must be modified only once, during device configuration. Continuously switching the EBSR configuration is not supported.

15	14	13	12	11	10	9	8
Reserved	PPMODE			SP1MODE		SP0MODE	
R-0	R/W-000			R/W-00		R/W-00	

7	6	5	4	3	2	1	0
Reserved	Reserved	A20_MODE	A19_MODE	A18_MODE	A17_MODE	A16_MODE	A15_MODE
R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 4-2. External Bus Selection Register (EBSR) [1C00h]

Table 4-3. EBSR Register Bit Descriptions

BIT	NAME	DESCRIPTION
15	RESERVED	Reserved. Read-only, writes have no effect.
14:12	PPMODE	Parallel Port Mode Control Bits. These bits control the pin multiplexing of the LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] pins on the parallel port. For more details, see Table 4-4, *LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] Pin Multiplexing*. 000 = Mode 0 (16-bit LCD Controller). All 21 signals of the LCD Bridge module are routed to the 21 external signals of the parallel port. 001 = Mode 1 (SPI, GPIO, UART, and I2S2). 7 signals of the SPI module, 6 GPIO signals, 4 signals of the UART module and 4 signals of the I2S2 module are routed to the 21 external signals of the parallel port. 010 = Mode 2 (8-bit LCD Controller and GPIO). 8-bits of pixel data of the LCD Controller module and 8 GPIO are routed to the 21 external signals of the parallel port. 011 = Mode 3 (8-bit LCD Controller, SPI, and I2S3). 8-bits of pixel data of the LCD Controller module, 4 signals of the SPI module, and 4 signals of the I2S3 module are routed to the 21 external signals of the parallel port. 100 = Mode 4 (8-bit LCD Controller, I2S2, and UART). 8-bits of pixel data of the LCD Controller module, 4 siignals of the I2S2 module, and 4 signals of the UART module are routed to the 21 external signals of the parallel port. 101 = Mode 5 (8-bit LCD Controller, SPI, and UART). 8-bits of pixel data of the LCD Controller module, 4 signals of the SPI module, and 4 signals of the UART module are routed to the 21 external signals of the parallel port. 110 = Mode 6 (SPI, I2S2, I2S3, and GPIO). 7 signals of the SPI module, 4 signals of the I2S2 module, 4 signals of the I2S3 module, and 6 GPIO are routed to the 21 external signals of the parallel port. 111 = Reserved.
11:10	SP1MODE	Serial Port 1 Mode Control Bits. The bits control the pin multiplexing of the MMC1, I2S1, and GPIO pins on serial port 1. For more details, see Table 4-5, *MMC1, I2S1 , and GP[11:6] Pin Multiplexing*. 00 = Mode 0 (MMC/SD1). All 6 signals of the MMC/SD1 module are routed to the 6 external signals of the serial port 1 . 01 = Mode 1 (I2S1 and GP[11:10]). 4 signals of the I2S1 module and 2 GP[11:10] signals are routed to the 6 external signals of the serial port 1. 10 = Mode 2 (GP[11:6]). 6 GPIO signals (GP[11:6]) are routed to the 6 external signals of the serial port 1. 11 = Reserved.

Table 4-3. EBSR Register Bit Descriptions (continued)

BIT	NAME	DESCRIPTION
9:8	SP0MODE	Serial Port 0 Mode Control Bits. The bits control the pin multiplexing of the MMC0, I2S0, and GPIO pins on serial port 0. For more details, see Section 4.7.1.3, *MMC0, I2S0, and GP[5:0] Pin Multiplexing*. 00 = Mode 0 (MMC/SD0). All 6 signals of the MMC/SD0 module are routed to the 6 external signals of the serial port 0. 01 = Mode 1 (I2S0 and GP[5:0]). 4 signals of the I2S0 module and 2 GP[5:4] signals are routed to the 6 external signals of the serial port 0. 10 = Mode 2 (GP[5:0]). 6 GPIO signals (GP[5:0]) are routed to the 6 external signals of the serial port 0. 11 = Reserved.
7	RESERVED	Reserved. Read-only, writes have no effect.
6	RESERVED	Reserved. Read-only, writes have no effect.
5	A20_MODE	A20 Pin Mode Bit. This bit controls the pin mulitplexing of the EMIF address 20 (EM_A[20]) and general-purpose input/output pin 26 (GP[26]) pin functions. 0 = Pin function is EMIF address pin 20 (EM_A[20]). 1 = Pin function is general-purpose input/output pin 26 (GP[26]).
4	A19_MODE	A19 Pin Mode Bit. This bit controls the pin mulitplexing of the EMIF address 19 (EM_A[19]) and general-purpose input/output pin 25 (GP[25]) pin functions. 0 = Pin function is EMIF address pin 19 (EM_A[19]). 1 = Pin function is general-purpose input/output pin 25 (GP[25]).
3	A18_MODE	A18 Pin Mode Bit. This bit controls the pin mulitplexing of the EMIF address 18 (EM_A[18]) and general-purpose input/output pin 24 (GP[24]) pin functions. 0 = Pin function is EMIF address pin 18 (EM_A[18]). 1 = Pin function is general-purpose input/output pin 24 (GP[24]).
2	A17_MODE	A17 Pin Mode Bit. This bit controls the pin mulitplexing of the EMIF address 17 (EM_A[17]) and general-purpose input/output pin 23 (GP[23]) pin functions. For more details, see Table 4-6, *EM_A[20:16] and GP[26:21] Pin Multiplexing*. 0 = Pin function is EMIF address pin 17 (EM_A[17]). 1 = Pin function is general-purpose input/output pin 23 (GP[23]).
1	A16_MODE	A16 Pin Mode Bit. This bit controls the pin mulitplexing of the EMIF address 16 (EM_A[16]) and general-purpose input/output pin 22 (GP[22]) pin functions. For more details, see Table 4-6, *EM_A[20:16] and GP[26:21] Pin Multiplexing*. 0 = Pin function is EMIF address pin 16 (EM_A[16]). 1 = Pin function is general-purpose input/output pin 22 (GP[22]).
0	A15_MODE	A15 Pin Mode Bit. This bit controls the pin mulitplexing of the EMIF address 15 (EM_A[15]) and general-purpose input/output pin 21 (GP[21]) pin functions. For more details, see Table 4-6, *EM_A[20:16] and GP[26:21] Pin Multiplexing*. 0 = Pin function is EMIF address pin 15 (EM_A[15]). 1 = Pin function is general-purpose input/output pin 21 (GP[21]).

4.6.2 EMIF and USB System Control Registers (ESCR and USBSCR) [1C33h and 1C32h]

After reset, by default, the CPU performs 16-bit accesses to the EMIF and USB registers and data space. To perform 8-bit accesses to the EMIF data space, the user must set the BYTEMODE bits to 01b for the "high byte" or 10b for the "low byte" in the EMIF System Control Register (ESCR). Similarly, the BYTEMODE bits in the USB System Control Register (USBSCR) must also be configured for byte access.

4.6.3 Peripheral Clock Gating Control Registers (PCGCR1 and PCGCR2) [1C02h and 1C03h]

After hardware reset, all of the peripheral clocks are "off" to conserve power. Then, the DSP executes the on-chip bootloader from ROM. As the bootloader executes, it selectively enables the clock of the peripheral being queried for a valid boot. If a valid boot source is not found, the bootloader disables the clock to that peripheral and moves on to the next peripheral in the boot order. After the boot process is complete, the peripheral clocks will be off and all domains in the ICR, except the CPU domain, will be idled (this includes the MPORT and HWA). The user must enable the clocks to the peripherals and CPU ports that are going to be used. The peripheral clock gating control registers (PCGCR1 and PCGCR2) are used to enable and disable the peripheral clocks.

4.6.4 Pull-up/Pull-down Inhibit Registers (PDINHIBR1/2/3) [1C17h, 1C18h, and 1C19h, respectively]

Each internal pullup and pulldown (IPU/IPD) resistor on the VC5505 DSP, except for the IPD on $\overline{\text{TRST}}$, can be individually controlled through the IPU/IPD registers (PDINHIBR1 [1C17h] , PDINHIBR2 [1C18h], and PDINHIBR3 [1C19h]). To minimize power consumption, internal pullup or pulldown resistors should be disabled in the presence of an external pullup or pulldown resistor or external driver. Section 4.8.1, *Pullup/Pulldown Resistors*, describes other situations in which an pullup and pulldown resistors are required.

4.6.5 Output Slew Rate Control Register (OSRCR) [1C16h]

To provide the lowest power consumption setting, the DSP has configurable slew rate control on the EMIF and CLKOUT output pins. The output slew rate control register (OSRCR) is used to set a subset of the device I/O pins to either fast or slow slew rate. The slew rate feature is implemented by staging/delaying turn-on times of the parallel p-channel drive transistors and parallel n-channel drive transistors of the output buffer. In the slow slew rate configuration, the delay is longer, but ultimately the same number of parallel transistors are used to drive the output high or low. Thus, the drive strength is ultimately the same strength. The slower slew rate control can be used for power savings and has the greatest effect at lower VDD_IO voltages.

4.7 Multiplexed Pin Configurations

The VC5505 DSP uses pin multiplexing to accommodate a larger number of peripheral functions in the smallest possible package, providing the ultimate flexibility for end applications. The external bus selection register (EBSR) controls all the pin multiplexing functions on the device.

4.7.1 Pin Multiplexing Details

This section discusses how to program the external bus selection register (EBSR) to select the desired peripheral functions and pin muxing. See the individual pin mux sections for pin muxing details for a specific muxed pin. After changing any of the pin mux control registers, it will be necessary to reset the peripherals that are affected.

4.7.1.1 LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] Pin Multiplexing [EBSR.PPMODE Bits]

The LCD Controller, SPI, UART, I2S2, I2S3, and GPIO signal muxing is determined by the value of the PPMODE bit fields in the External Bus Selection Register (EBSR) register. For more details on the actual pin functions, see Table 4-4 .

Table 4-4. LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] Pin Multiplexing

PDINHIBR3 REGISTER BIT FIELDS(1)	PIN MUX SIGNAL NAME	EBSR PPMODE BITS						
		MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6
		000	001	010	011	100	101	110
	LCD_EN_RDB/SPI_CLK	LCD_EN_RDB	SPI_CLK	LCD_EN_RDB	LCD_EN_RDB	LCD_EN_RDB	LCD_EN_RDB	SPI_CLK
	LCD_D[0]/SPI_RX	LCD_D[0]	SPI_RX	LCD_D[0]	LCD_D[0]	LCD_D[0]	LCD_D[0]	SPI_RX
	LCD_D[1]/SPI_TX	LCD_D[1]	SPI_TX	LCD_D[1]	LCD_D[1]	LCD_D[1]	LCD_D[1]	SPI_TX
P2PD	LCD_D[2]/GP[12]	LCD_D[2]	GP[12]	LCD_D[2]	LCD_D[2]	LCD_D[2]	LCD_D[2]	GP[12]
P3PD	LCD_D[3]/GP[13]	LCD_D[3]	GP[13]	LCD_D[3]	LCD_D[3]	LCD_D[3]	LCD_D[3]	GP[13]
P4PD	LCD_D[4]/GP[14]	LCD_D[4]	GP[14]	LCD_D[4]	LCD_D[4]	LCD_D[4]	LCD_D[4]	GP[14]
P5PD	LCD_D[5]/GP[15]	LCD_D[5]	GP[15]	LCD_D[5]	LCD_D[5]	LCD_D[5]	LCD_D[5]	GP[15]
P6PD	LCD_D[6]/GP[16]	LCD_D[6]	GP[16]	LCD_D[6]	LCD_D[6]	LCD_D[6]	LCD_D[6]	GP[16]
P7PD	LCD_D[7]/GP[17]	LCD_D[7]	GP[17]	LCD_D[7]	LCD_D[7]	LCD_D[7]	LCD_D[7]	GP[17]
P8PD	LCD_D[8]/I2S2_CLK/GP[18]/SPI_CLK	LCD_D[8]	I2S2_CLK	GP[18]	SPI_CLK	I2S2_CLK	SPI_CLK	I2S2_CLK
P9PD	LCD_D[9]/I2S2_FS/GP[19]/SPI_CS0	LCD_D[9]	I2S2_FS	GP[19]	SPI_CS0	I2S2_FS	SPI_CS0	I2S2_FS
P10PD	LCD_D[10]/I2S2_RX/GP[20]/SPI_RX	LCD_D[10]	I2S2_RX	GP[20]	SPI_RX	I2S2_RX	SPI_RX	I2S2_RX
P11PD	LCD_D[11]/I2S2_DX/GP[27]/SPI_TX	LCD_D[11]	I2S2_DX	GP[27]	SPI_TX	I2S2_DX	SPI_TX	I2S2_DX
P12PD	LCD_D[12]/UART_RTS/GP[28]/I2S3_CLK	LCD_D[12]	UART_RTS	GP[28]	I2S3_CLK	UART_RTS	UART_RTS	I2S3_CLK
P13PD	LCD_D[13]/UART_CTS/GP[29]/I2S3_FS	LCD_D[13]	UART_CTS	GP[29]	I2S3_FS	UART_CTS	UART_CTS	I2S3_FS
P14PD	LCD_D[14]/UART_RXD/GP[30]/I2S3_RX	LCD_D[14]	UART_RXD	GP[30]	I2S3_RX	UART_RXD	UART_RXD	I2S3_RX
P15PD	LCD_D[15]/UART_TXD/GP[31]/I2S3_DX	LCD_D[15]	UART_TXD	GP[31]	I2S3_DX	UART_TXD	UART_TXD	I2S3_DX
	LCD_CS0_E0/SPI_CS0	LCD_CS0_E0	SPI_CS0	LCD_CS0_E0	LCD_CS0_E0	LCD_CS0_E0	LCD_CS0_E0	SPI_CS0
	LCD_CS1_E1/SPI_CS1	LCD_CS1_E1	SPI_CS1	LCD_CS1_E1	LCD_CS1_E1	LCD_CS1_E1	LCD_CS1_E1	SPI_CS1
	LCD_RW_WRB/SPI_CS2	LCD_RW_WRB	SPI_CS2	LCD_RW_WRB	LCD_RW_WRB	LCD_RW_WRB	LCD_RW_WRB	SPI_CS2
	LCD_RS/SPI_CS3	LCD_RS	SPI_CS3	LCD_RS	LCD_RS	LCD_RS	LCD_RS	SPI_CS3

(1) The pin mux signals names with PDINHIBR3 register bit field references can have the pulldown resister enabled or disabled via this register.

4.7.1.2 MMC1, I2S1, and GP[11:6] Pin Multiplexing [EBSR.SP1MODE Bits]

The MMC1, I2S1, and GPIO signal muxing is determined by the value of the SP1MODE bit fields in the External Bus Selection Register (EBSR) register. For more details on the actual pin functions, see Table 4-5.

Table 4-5. MMC1, I2S1, and GP[11:6] Pin Multiplexing

PDINHIBR1 REGISTER BIT FIELDS(1)	PIN MUX SIGNAL NAME	EBSR SP1MODE BITS		
		MODE 0	MODE 1	MODE 2
		00	01	10
S10PD	MMC1_CLK/I2S1_CLK/GP[6]	MMC1_CLK	I2S1_CLK	GP[6]
S11PD	MMC1_CMD/I2S1_FS/GP[7]	MMC1_CMD	I2S1_FS	GP[7]
S12PD	MMC1_D0/I2S1_DX/GP[8]	MMC1_D0	I2S1_DX	GP[8]
S13PD	MMC1_D1/I2S1_RX/GP[9]	MMC1_D1	I2S1_RX	GP[9]
S14PD	MMC1_D2/GP[10]	MMC1_D2	GP[10]	GP[10]
S15PD	MMC1_D3/GP[11]	MMC1_D3	GP[11]	GP[11]

(1) The pin mux signals names with PDINHIBR1 register bit field references can have the pulldown register enabled or disabled via this register.

4.7.1.3 MMC0, I2S0, and GP[5:0] Pin Multiplexing [EBSR.SP0MODE Bits]

The MMC0, I2S0, and GPIO signal muxing is determined by the value of the SP0MODE bit fields in the External Bus Selection Register (EBSR) register. For more details on the actual pin functions, see Table 4-6.

Table 4-6. MMC0, I2S0, and GP[5:0] Pin Multiplexing

PDINHIBR1 REGISTER BIT FIELDS(1)	PIN MUX SIGNAL NAME	EBSR SP0MODE BITS		
		MODE 0	MODE 1	MODE 2
		00	01	10
S00PD	MMC0_CLK/I2S0_CLK/GP[0]	MMC0_CLK	I2S0_CLK	GP[0]
S01PD	MMC0_CMD/I2S0_FS/GP[1]	MMC0_CMD	I2S0_FS	GP[1]
S02PD	MMC0_D0/I2S0_DX/GP[2]	MMC0_D0	I2S0_DX	GP[2]
S03PD	MMC0_D1/I2S0_RX/GP[3]	MMC0_D1	I2S0_RX	GP[3]
S04PD	MMC0_D2/GP[4]	MMC0_D2	GP[4]	GP[4]
S05PD	MMC0_D3/GP[5]	MMC0_D3	GP[5]	GP[5]

(1) The pin mux signals names with PDINHIBR1 register bit field references can have the pulldown register enabled or disabled via this register.

4.7.1.4 EMIF EM_A[20:15] and GP[26:21] Pin Multiplexing [EBSR.Axx_MODE bits]

The EMIF Address and GPIO signal muxing is determined by the value of the A20_MODE, A19_MODE, A18_MODE, A17_MODE, A16_MODE, and A15_MODE bit fields in the External Bus Selection Register (EBSR) register. For more details on the actual pin functions, see Table 4-7.

Table 4-7. EM_A[20:16] and GP[26:21] Pin Multiplexing

PIN MUX SIGNAL NAME	Axx_MODE BIT	
	0	1
EM_A[15]/GP[21]	EM_A[15]	GP[21]
EM_A[16]/GP[22]	EM_A[16]	GP[22]
EM_A[17]/GP[23]	EM_A[17]	GP[23]
EM_A[18]/GP[24]	EM_A[18]	GP[24]
EM_A[19]/GP[25]	EM_A[19]	GP[25]
EM_A[20]/GP[26]	EM_A[20]	GP[26]

4.8 Debugging Considerations

4.8.1 Pullup/Pulldown Resistors

Proper board design should ensure that input pins to the VC5505 DSP always be at a valid logic level and not floating. This may be achieved via pullup/pulldown resistors. The DSP features internal pullup (IPU) and internal pulldown (IPD) resistors on many (all GPIO) pins to eliminate the need, unless otherwise noted, for external pullup/pulldown resistors.

An external pullup/pulldown resistor needs to be used in the following situations:

- Configuration Pins: An external pullup/pulldown resistor is recommended to set the desired value/state (see the configuration pins listed in Table 4-2, *Default Functions Affected by Device Configuration Pins*). Note that some configuration pins must connected directly to ground or to a specific supply voltage.
- Other Input Pins: If the IPU/IPD does not match the desired value/state, use an external pullup/pulldown resistor to pull the signal to the opposite rail.

For the configuration pins (listed in Table 4-2, *Default Functions Affected by Device Configuration Pins*), if they are both routed out and 3-stated (not driven), it is strongly recommended that an external pullup/pulldown resistor be implemented. In addition, applying external pullup/pulldown resistors on the configuration pins adds convenience to the user in debugging and flexibility in switching operating modes.

When an external pullup or pulldown resistor is used on a pin, the pin's internal pullup or pulldown resistor should be disabled through the Pull-up/Pull-down Inhibit Registers (PDINHIBR1/2/3) [1C17h, 1C18h, and 1C19h, respectively] to minimize power consumption.

Tips for choosing an external pullup/pulldown resistor:

- Consider the total amount of current that may pass through the pullup or pulldown resistor. Make sure to include the leakage currents of all the devices connected to the net, as well as any internal pullup or pulldown (IPU/IPD) resistors.
- Decide a target value for the net. For a pulldown resistor, this should be below the lowest VIL level of all inputs connected to the net. For a pullup resistor, this should be above the highest VIH level of all inputs on the net. A reasonable choice would be to target the VOL or VOH levels for the logic family of the limiting device; which, by definition, have margin to the VIL and VIH levels.
- Select a pullup/pulldown resistor with the largest possible value; but, which can still ensure that the net will reach the target pulled value when maximum current from all devices on the net is flowing through the resistor. The current to be considered includes leakage current plus, any other internal and external pullup/pulldown resistors on the net.
- For bidirectional nets, there is an additional consideration which sets a lower limit on the resistance value of the external resistor. Verify that the resistance is small enough that the weakest output buffer can drive the net to the opposite logic level (including margin).
- Remember to include tolerances when selecting the resistor value.
- For pullup resistors, also remember to include tolerances on the DV_{DD} rail.

For most systems, a 1-kΩ resistor can be used to oppose the IPU/IPD while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For most systems, a 20-kΩ resistor can be used to compliment the IPU/IPD on the configuration pins while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For more detailed information on input current (I_I), and the low-/high-level input voltages (V_{IL} and V_{IH}) for the VC5505 DSP, see Section 5.3, *Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature*.

For the internal pullup/pulldown resistors for all device pins, see the peripheral/system-specific terminal functions table in this document.

4.8.2 CLKOUT Pin

For debug purposes, the DSP includes a CLKOUT pin which can be used to tap different clocks within the clock generator. The SRC bits of the CLKOUT Control Source Register (CCSSR) can be used to specify the source for the CLKOUT pin.

Note: the bootloader disables the CLKOUT pin via CLKOFF bit in the ST3_55 CPU register.

For more information on the ST3_55 CPU register, see the *TMS320C55x 3.0 CPU* Reference Guide (literature number: SWPU073).

5 Device Operating Conditions

5.1 Absolute Maximum Ratings Over Operating Case Temperature Range (Unless Otherwise Noted)(1)

Supply voltage ranges:	Digital Core (CV_{DD}, CV_{DDRTC}, USB_V_{DD1P3})(2)	–0.5 V to 1.7 V
	I/O, 1.8 V, 2.5 V, 2.8 V, 3.3 V (DV_{DDIO}, DV_{DDEMIF}, DV_{DDRTC}) 3.3V USB supplies USB PHY (USB_V_{DDOSC}, USB_V_{DDPLL}, USB_V_{DDA3P3})(2)	–0.5 V to 4.2 V
	ANA_LDOI	–0.5 V to 4.2 V
	Analog, 1.3 V (V_{DDA_PLL}, USB_V_{DDA1P3}, V_{DDA_ANA})(2)	–0.5 V to 1.7 V
Input and Output voltage ranges:	V_I I/O, All pins with DV_{DDIO} or DV_{DDEMIF} or USB_V_{DDOSC} or USB_V_{DDPLL}or USB_V_{DDA3P3} as supply source	–0.5 V to 4.2 V
	V_O I/O, All pins with DV_{DDIO} or DV_{DDEMIF} or USB_V_{DDOSC}or USB_V_{DDPLL}or USB_V_{DDA3P3} as supply source	–0.5 V to 4.2 V
	RTC_XI and RTC_XO	–0.5 V to 1.7 V
	V_I and V_O, GPAIN[0]	–0.5 V to 4.2 V
	V_I and V_O, GPAIN[3:1]	–0.5 V to 1.7 V
	V_O, BG_CAP	–0.5 V to 1.7 V
	ANA_LDOO	–0.5 V to 1.7 V
Operating case temperature ranges, T_c:	Commercial Temperature (default)	0°C to 70°C
	Industrial Temperature	-40°C to 85°C
Storage temperature range, T_{stg}	(default)	–65°C to 150°C
Device Operating Life Power-On Hours (POH)	Commercial Temperature(3)	100, 000 POH
	Industrial Temperature(3)	100, 000 POH

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to $V_{SS.}$
(3) For devices running with CV_{DD} = 1.3 V @ 100 MHz for commercial temperature, the Device Operating Life Power-On Hours are 70, 000 POH of the total POH .
For devices running with CV_{DD} = 1.3 V @ 100 MHz for industrial temperature, the Device Operating Life Power-On Hours are 17, 000 POH of the total POH.

5.2 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
CV_{DD}	CV_{DD}	Supply voltage, Digital Core	60 MHz	0.998	1.05	1.15	V
			100 MHz	1.24	1.3	1.43	V
	CV_{DDRTC}	Supply voltage, RTC and RTC OSC	32.768 KHz	0.998		1.43	V
	USB_V_{DD1P3}	Supply voltage, Digital USB		1.24	1.3	1.43	V
	USB_V_{DDA1P3}	Supply voltage, 1.3 V Analog USB		1.24	1.3	1.43	V
	V_{DDA_ANA}	Supply voltage, 1.3 V SAR and Pwr Mgmt		1.24	1.3	1.43	V
	V_{DDA_PLL}	Supply voltage, 1.3 V System PLL		1.24	1.3	1.43	V
	USB_V_{DDPLL}	Supply voltage, 3.3 V USB PLL		2.97	3.3	3.63	V
DV_{DD}	DV_{DDIO} DV_{DDEMIF} DV_{DDRTC}	Supply voltage, I/O, 3.3 V		2.97	3.3	3.63	V
		Supply voltage, I/O, 2.8 V		2.52	2.8	3.08	V
		Supply voltage, I/O, 2.5 V		2.25	2.5	2.75	V
		Supply voltage, I/O, 1.8 V		1.65	1.8	1.98	V
	USB_V_{DDOSC}	Supply voltage, I/O, 3.3 V USB OSC		2.97	3.3	3.63	V
	USB_V_{DDA3P3}	Supply voltage, I/O, 3.3 V Analog USB PHY		2.97	3.3	3.63	V
	ANA_LDOI	Supply voltage, Analog Pwr Mgmt and LDO Input		1.8		3.6	V
V_{SS}	V_{SS}	Supply ground, Digital I/O		0	0	0	V
	V_{SSRTC}	Supply ground, RTC					
	USB_V_{SSOSC}	Supply ground, USB OSC					
	USB_V_{SSPLL}	Supply ground, USB PLL					
	USB_V_{SSA3P3}	Supply ground, 3.3 V Analog USB PHY					
	USB_V_{SSA1P3}	Supply ground, USB 1.3 V Analog USB PHY					
	USB_V_{SSREF}	Supply ground, USB Reference Current					
	V_{SSA_PLL}	Supply ground, System PLL					
	USB_V_{SS1P3}	Supply ground, 1.3 V Digital USB PHY					
	V_{SSA_ANA}	Supply ground, SAR and Pwr Mgmt					
V_{IH} (1)		High-level input voltage, 3.3, 2.8, 2.5, 1.8 V I/O (except GPAIN[3:0] pins) (2)		0.7 * DV_{DD}		DV_{DD} + 0.3	V
V_{IL} (1)		Low-level input voltage, 3.3, 2.8, 2.5, 1.8 V I/O (except GPAIN[3:0] pins) (2)		-0.3		0.3 * DV_{DD}	V
V_{IN}		Input voltage, GPAIN0 pin (3)		-0.3		3.6	V
		Input voltage, GPAIN[3:1] pins		-0.3		V_{DDA_ANA} + 0.3	V
T_c		Operating case temperature	Default (Commercial)	0		70	°C
			(Industrial)	-40		85	°C
$F_{SYSCLK1}$		DSP Operating Frequency (SYSCLK1)	1.05 V	0		60	MHz
			1.3 V	0		100	MHz

(1) DV_{DD} refers to the pin I/O supply voltage. To determine the I/O supply voltage for each pin, see Section 3.5 , *Terminal Functions*.
(2) The I2C pin SDA and SCL do not feature fail-safe I/O buffers. These pin could polentially draw current when the device is powered down. Dues to the fact that different voltage devices can be connected to I2C bus, the level of logic 0 (low) and logic 1 (high) are not fixed and depends on the associated DV_{DD}.
(3) The GNDON bit in the SARPINCTRL register should be set to "1" before SAR channels 0, 1, or 2 are enabled via the CHSEL bit in the SARCTRL register, when V_{IN} greater than V_{DDA_ANA}.

5.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS (1)		MIN	TYP	MAX	UNIT
V_{OH}	Full speed: USB_DN and USB_DP (2)			2.8		USB_V_{DDA3P3}	V
	High speed: USB_DN and USB_DP (2)			360		440	mV
	High-level output voltage, 3.3, 2.8, 2.5, 1.8 V I/O (except GPAIN[3:0] pins)	IO = I_{OH}		0.8 * DV_{DD}			V
	High-level output voltage, GPAIN[3:1] pins	IO = I_{OH}		0.8 * V_{DDA_ANA}			V
V_{OL}	Full speed: USB_DN and USB_DP (2)			0.0		0.3	V
	High speed: USB_DN and USB_DP (2)			–10		10	mV
	Low-level output voltage, 3.3, 2.8, 2.5, 1.8V I/O (except I2C and GPAIN[3:0] pins)	IO = I_{OL}				0.2 * DV_{DD}	V
	Low-level output voltage, I2C pins (3)	V_{DD} > 2 V, $I_{O\ L}$ = 3 mA		0		0.4	V
	Low-level output voltage, GPAIN[3:0] pins	IO = I_{OL}				0.2 * V_{DDA_ANA}	V
V_{HYS}	Input hysteresis (4)	DV_{DD} = 3.3 V			162		mV
		DV_{DD} = 2.5 V			141		mV
		DV_{DD} = 1.8 V			122		mV
V_{LDO}	ANA_LDOO voltage			1.24	1.3	1.43	V
I_{SD}	ANA_LDO shutdown current (5)	ANA_LDOI = V_{MIN}		3			mA
I_{ILPU} (6)	Input current [DC] (except WAKEUP, I2C, and GPAIN[3:0] pins)	Input only pin, internal pulldown or pullup disabled		-5		+5	μA
		DV_{DD} = 3.3 V with internal pullup enabled (7)			-59 to -161		μA
		DV_{DD} = 2.5 V with internal pullup enabled (7)			-31 to -93		μA
		DV_{DD} = 1.8 V with internal pullup enabled (7)			-14 to -44		μA
I_{IHPD} (6)	Input current [DC] (except WAKEUP, I2C, and GPAIN[3:0] pins	Input only pin, internal pulldown or pullup disabled		-5		+5	μA
		DV_{DD} = 3.3 V with internal pulldown enabled (7)			52 to 158		μA
		DV_{DD} = 2.5 V with internal pulldown enabled (7)			27 to 83		μA
		DV_{DD} = 1.8 V with internal pulldown enabled (7)			11 to 35		μA
I_{IH}/ I_{IL}	Input current [DC], ALL pins	V_I = V_{SS} to DV_{DD} with internal pullups and pulldowns disabled.		-5		+5	μA
I_{OH}	High-level output current [DC]	All Pins (except USB, EMIF, CLKOUT, and GPAIN[3:0] pins)		-4			mA
		EMIF pins	DV_{DD} = 3.3 V	-6			mA
			DV_{DD} = 1.8 V	-5			mA
		CLKOUT pin	DV_{DD} = 3.3 V	-6			mA
			DV_{DD} = 1.8 V	-4			mA
		GPAIN[3:1] pins (GPAIN0 is open-drain and cannot drive high)	DV_{DD} = V_{DDA_ANA} = 1.3 V, External Regulator (8)	-4			mA
			DV_{DD} = V_{DDA_ANA} = 1.3 V, Internal Regulator (8)	-100			μA

(1) For test conditions shown as MIN, MAX, or TYP, use the appropriate value specified in the recommended operating conditions table.
(2) The USB I/Os adhere to the Universal Bus Specification Revision 2.0 (USB2.0 spec).
(3) V_{DD} is the voltage to which the I2C bus pullup resistors are connected.
(4) Applies to all input pins except WAKEUP, I2C pins, GPAIN[3:0], RTC_XI, and USB_MXI.
(5) I_{SD} is the amount of current the LDO is ensured to deliver before shutting down to protect itself.
(6) I_I applies to input-only pins and bi-directional pins. For input-only pins, I_I indicates the input leakage current. For bi-directional pins, I_I indicates the input leakage current and off-state (Hi-Z) output leakage current.
(7) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.
(8) When the ANA_LDO supplies V_{DDA_ANA}, it is not recommended to use the GPAIN[3:1] signals for general-purpose outputs (driving high). The I_{SD} parameter of the ANA_LDO is too low to drive any realistic load on the GPAIN[3:1] pins while also supplying the PLL through V_{DDA_PLL} and the SAR through V_{DDA_ANA}.

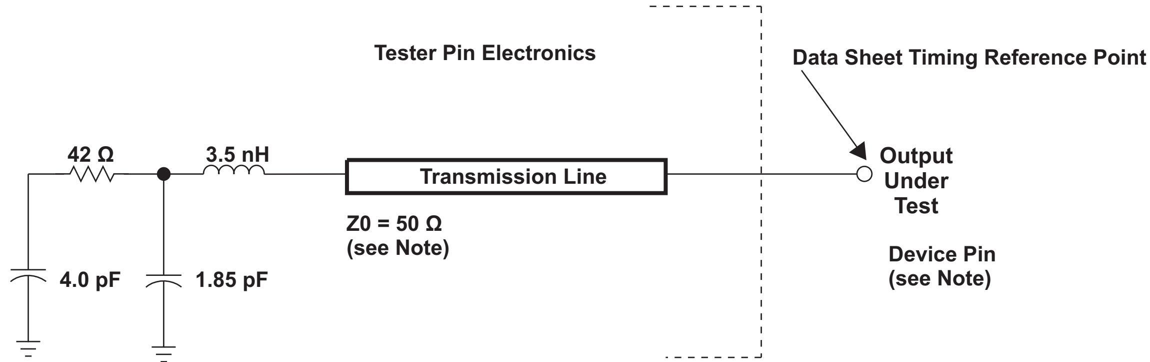
Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted) *(continued)*

PARAMETER		TEST CONDITIONS [1]		MIN	TYP	MAX	UNIT
I_{OL}	Low-level output current [DC]	All Pins (except USB, EMIF, CLKOUT, and GPAIN[3:0] pins)				+4	mA
		EMIF pins	DV_{DD} = 3.3 V			+6	mA
			DV_{DD} = 1.8 V			+5	mA
		CLKOUT pin	DV_{DD} = 3.3 V			+6	mA
			DV_{DD} = 1.8 V			+4	mA
		GPAIN[3:0]	$DV_{DD} = V_{DDA\_ANA}$ = 1.3 V, external regulator			+4	mA
			$DV_{DD} = V_{DDA\_ANA}$ = 1.3 V, internal regulator[8]			+4	mA
I_{OZ} [9]	I/O Off-state output current	All Pins (except USB and GPAIN[3:0])		-10		+10	μA
		GPAIN[3:0] pins		-10		+10	μA
I_{CDD}	Core (CV_{DD}) supply current	Active, CV_{DD} = 1.3 V, DSP clock = 100 MHz Room Temp (25 °C), 75% DMAC + 25% ADD (typical sine wave data switching)			0.22		mW/MHz
		Active, CV_{DD} = 1.05 V, DSP clock = 60 MHz Room Temp (25 °C), 75% DMAC + 25% ADD (typical data switching)			0.15		mW/MHz
		Active, CV_{DD} = 1.3 V, DSP clock = 100 MHz Room Temp (25 °C), 75% DMAC + 25% NOP (typical sine wave data switching)			0.22		mW/MHz
		Active, CV_{DD} = 1.05 V, DSP clock = 60 MHz Room Temp (25 °C), 75% DMAC + 25% NOP (typical data switching)			0.14		mW/MHz
		Active, CV_{DD} = 1.3 V, DSP clock = 100 MHz Room Temp (25 °C), Hardware FFT Accelerator 1024-pt FFT, ROM execution			0.31		mW/MHz
		Active, CV_{DD} = 1.05 V, DSP clock = 60 MHz Room Temp (25 °C), Hardware FFT Accelerator 1024-pt FFT, ROM execution			0.25		mW/MHz
		Standby, CV_{DD} = 1.3 V, Master clock disabled, Room Temp (25 °C), DARAM and SARAM in active mode			0.44		mW
		Standby, CV_{DD} = 1.05 V, Master clock disabled, Room Temp (25 °C), DARAM and SARAM in active mode			0.26		mW
		Standby, CV_{DD} = 1.3 V, Master clock disabled, Room Temp (25 °C), DARAM in retention and SARAM in active mode			0.40		mW
		Standby, CV_{DD} = 1.05 V, Master clock disabled, Room Temp (25 °C), DARAM in retention and SARAM in active mode			0.23		mW
		Standby, CV_{DD} = 1.3 V, Master clock disabled, Room Temp (25 °C), DARAM in active mode and SARAM in retention			0.28		mW
		Standby, CV_{DD} = 1.05 V, Master clock disabled, Room Temp (25 °C), DARAM in active mode and SARAM in retention			0.15		mW
	Analog PLL (V_{DDA_PLL}) supply current	V_{DDA_PLL} = 1.37 V Room Temp (25 °C), Phase detector = 170 kHz, VCO = 120 MHz			0.7	1.2	mA
	SAR Analog (V_{DDA_ANA}) supply current	V_{DDA_ANA} = 1.37 V, SAR clock = 2 MHz, Temp (70 °C)				1	mA
C_I	Input capacitance					4	pF
C_o	Output capacitance					4	pF

(9) I_{OZ} applies to output-only pins, indicating off-state (Hi-Z) output leakage current.

6 Peripheral Information and Electrical Specifications

6.1 Parameter Information



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 6-1. 3.3-V Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.1.1 1.8-V, 2.5-V, 2.8-V, and 3.3-V Signal Transition Levels

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL} MAX and V_{OH} MIN for output clocks.

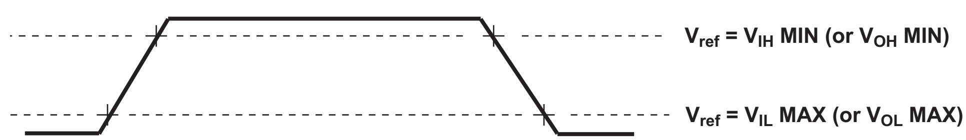


Figure 6-2. Rise and Fall Transition Time Voltage Reference Levels

6.1.2 3.3-V Signal Transition Rates

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

6.1.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data manual do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number SPRA839). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

6.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals ***must*** transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

6.3 Power Supplies

The VC5505 includes four core voltag-level supplies (CV_{DD}, CV_{DDRTC}, USB_V_{DD1P3}, USB_V_{DDA1P3}), and several I/O supplies (DV_{DDIO}, DV_{DDEMIF}, DV_{DDRTC}, USB_V_{DDOSC}, and USB_V_{DDA3P3}), as well as several analog supplies (ANA_LDOI, V_{DDA_PLL}, V_{DDA_ANA}, and USB_V_{DDPLL}). To ensure proper device operation, a specific power-up sequence must be followed. Some TI power-supply devices include features that facilitate power sequencing—for example, Auto-Track and Slow-Start/Enable features. For more information regarding TI's power management products and suggested devices to power TI DSPs, visit www.ti.com/processorpower.

6.3.1 Power-Supply Sequencing

The VC5505 includes four core voltage-level supplies (CV_{DD}, CV_{DDRTC}, USB_V_{DD1P3}, USB_V_{DDA1P3}), and several I/O supplies including—DV_{DDIO}, DV_{DDEMIF}, DV_{DDRTC}, USB_V_{DDOSC}, and USB_V_{DDA3P3}

For proper device operation, the general power-up sequence requirements can be summarized as ANA_LDOI and all core-level supplies must come up first, followed by the I/O level supplies. Specifically, the power-up sequence requirement is:

1. Apply power to the ANA_LDOI, CV_{DDRTC}, CV_{DD}, USB_V_{DD1P3}, USB_V_{DDA1P3}, V_{DDA_ANA}, and V_{DDA_PLL}.

   Note: the Analog LDO output (ANA_LDOO) can be used to power the V_{DDA_ANA}, and V_{DDA_PLL} supplies.

2. Apply power to I/Os: DV_{DDIO}, DV_{DDEMIF}, DV_{DDRTC}, USB_V_{DDOSC}, USB_V_{DDA3P3}, and USB_V_{DDPLL}.

Core supplies must be powered before I/O supplies. If the I/O supplies are powered before the core supply, the core signals controlling bi-directional I/Os are in an "undetermined state" and can set some of the bi-directional I/Os to drive against an external device, causing bus contention. Therefore, the I/O Supplies (DV_{DDIO}, DV_{DDEMIF}, DV_{DDRTC}, USB_V_{DDOSC}, USB_V_{DDA3P3}, and USB_V_{DDPLL}) should not ramp above 1.65 V before core supplies (CV_{DDRTC}, CV_{DD}, USB_V_{DD1P3}, USB_V_{DDA1P3}) reach 0.9 V.

If the USB subsystem is not used, the USB Core (USB_V_{DD1P3}, USB_V_{DDA1P3}) and USB PHY and I/O level supplies (USB_V_{DDOSC}, USB_V_{DDA3P3}, and USB_V_{DDPLL}) can be powered on and off anytime after this sequence. When powering on these supplies, the USB PHY, USB oscillator, and USB PLL (USB_V_{DDOSC}, USB_V_{DDA3P3}, and USB_V_{DDPLL}) should not ramp above 1.65 V before the USB Core (USB_V_{DD1P3}, USB_V_{DDA1P3}) reaches 0.9 V. When powering off these supplies, the USB Core (USB_V_{DD1P3}, USB_V_{DDA1P3}) should not drop below 0.9 V before the USB PHY, USB oscillator, and USB PLL (USB_V_{DDOSC}, USB_V_{DDA3P3}, and USB_V_{DDPLL}) drop below 1.65 V.

6.3.2 Power-Supply Design Considerations

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the VC5505 device, the PC board should include separate power planes for core, I/O, V_{DDA_ANA} and V_{DDA_PLL} (which can share the same PCB power plane), and ground; all bypassed with high-quality low-ESL/ESR capacitors.

6.3.3 Power-Supply Decoupling

In order to properly decouple the supply planes from system noise, place capacitors (caps) as close as possible to the VC5505 . These caps need to be no more than 1.25 cm maximum distance from the VC5505 power pins to be effective. Physically smaller caps, such as 0402, are better but need to be evaluated from a yield/manufacturing point-of-view. Parasitic inductance limits the effectiveness of the decoupling capacitors, therefore physically smaller capacitors should be used while maintaining the largest available capacitance value.

Larger caps for each supply can be placed further away for bulk decoupling. Large bulk caps (on the order of 10 μF) should be furthest away, but still as close as possible. Large caps for each supply should be placed outside of the BGA footprint.

As with the selection of any component, verification of capacitor availability over the product's production lifetime should be considered.

On the VC5505 the recommended decoupling capacitance for the DSP core supplies should be 1 μF in parallel with 0.01-μF capacitor per supply pin.

6.3.4 LDO Input Decoupling

The LDO inputs should follow the same decoupling guidelines as other power-supply pins above.

6.3.5 LDO Output Decoupling

The LDO circuits implement a voltage feedback control system which has been designed to optimize gain and stability tradeoffs. As such, there are design assumptions for the amount of capacitance on the LDO outputs. For proper device operation, the following external decoupling capacitors should be used:

- ANA_LDOO– 1μF
- DSP_LDOO – 1μF
- USB_LDOO – none required

6.4 External Clock Input From RTC_XI, CLKIN, and USB_MXI Pins

The VC5505 DSP includes two options to provide an external clock input to the system clock generator:

- Use the on-chip real-time clock (RTC) oscillator with an external 32.768-kHz crystal connected to the RTC_XI and RTC_XO pins.
- Use an external 11.2896-, 12.0-, or 12.288-MHz LVCMOS clock input fed into the CLKIN pin that operates at the same voltage as the DV_{DDIO} supply (1.8-, 2.5-, 2.8-, or 3.3-V).

The CLK_SEL pin determines which input is used as the clock source for the system clock generator, For more details, see Section 4.5.1, *Device and Peripheral Configurations at Device Reset*. The crystal for the RTC oscillator is not required if CLKIN is used as the system reference clock; however, the RTC must still be powered. The RTC registers starting at I/O address 1900h will not be accessible without an RTC clock. This includes the RTC Power Management Register which provides control to the on-chip LDOs and WAKEUP and RTC_CLKOUT pins. Section 6.4.1, *Real-Time Clock (RTC) On-Chip Oscillator With External Crystal* provides more details on using the RTC on-chip oscillator with an external crystal. Section 6.4.2, *CLKIN Pin With LVCMOS-Compatible Clock Input* provides details on using an external LVCMOS-compatible clock input fed into the CLKIN pin.

Additionally, the USB requires a reference clock generated using a dedicated on-chip oscillator with a 12-MHz external crystal connected to the USB_MXI and USB_MXO pins. The USB reference clock is not required if the USB peripheral is not being used. Section 6.4.3, *USB On-Chip Oscillator With External Crystal* provides details on using the USB on-chip oscillator with an external crystal.

6.4.1 Real-Time Clock (RTC) On-Chip Oscillator With External Crystal

The on-chip oscillator requires an external 32.768-kHz crystal connected across the RTC_XI and RTC_XO pins, along with two load capacitors, as shown in Figure 6-3. The external crystal load capacitors must be connected only to the RTC oscillator ground pin (V_{SSRTC}). ***Do not*** connect to board ground (V_{SS}). Position the V_{SS} lead on the board between RTC_XI and RTC_XO as a shield to reduce direct capacitance between RTC_XI and RTC_XO leads on the board. The CV_{DDRTC} pin can be connected to the same power supply as CV_{DD} , or may be connected to a different supply that meets the recommended operating conditions (see Section 5.2), if desired.

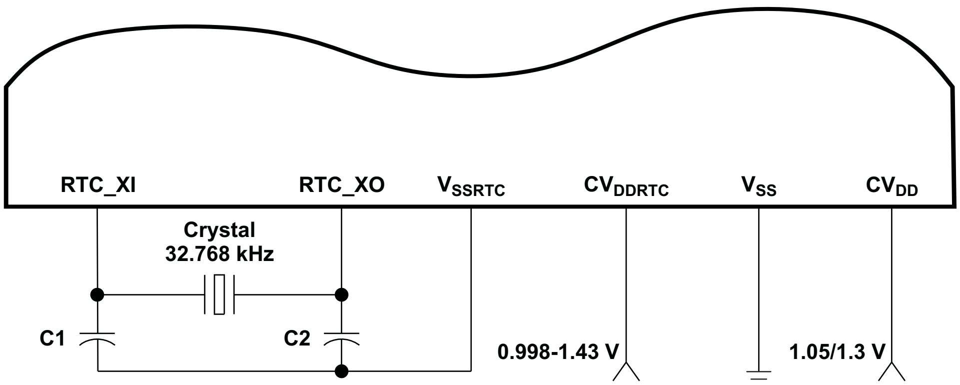


Figure 6-3. 32.768-kHz RTC Oscillator

The crystal should be in fundamental-mode function, and parallel resonant, with a maximum effective series resistance (ESR) specified in Table 6-1. The load capacitors, C1 and C2, are the total capacitance of the circuit board and components, excluding the IC and crystal. The load capacitors values are usually approximately twice the value of the crystal's load capacitance, CL, which is specified in the crystal manufacturer's datasheet and should be chosen such that the equation is satisfied. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (RTC_XI and RTC_XO) and to the V_{SSRTC} pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

Table 6-1. Input Requirements for Crystal on the 32.768-kHz RTC Oscillator

PARAMETER	MIN	NOM	MAX	UNIT
Start-up time (from power up until oscillating at stable frequency of 32.768-kHz)(1)	0.2		2	sec
Oscillation frequency		32.768		kHz
ESR			100	kΩ
Maximum shunt capacitance			1.6	pF
Maximum crystal drive			1.0	μW

(1) The startup time is highly dependent on the ESR and the capacitive load of the crystal.

6.4.2 *CLKIN Pin With LVCMOS-Compatible Clock Input (Optional)*

Note: If CLKIN is not used, the pin ***must*** be tied low.

A LVCMOS-compatible clock input of a frequency less than 24 MHz can be fed into the CLKIN pin for use by the DSP system clock generator. The external connections are shown in Figure 6-4 and Figure 6-5. The bootloader assumes that the CLKIN pin is connected to the LVCMOS-compatible clock source with a frequency of 11.2896-, 12.0-, or 12.288-MHz. These frequencies were selected to support boot mode peripheral speeds of 500 KHz for SPI, 400 KHz for I2C, and 57600 baud for UART (UART is currently not supported on this device). These clock frequencies are achieved by dividing the CLKIN value by 25 for SPI, by 32 for I2C, and by 208 for UART. If a faster external clock is input, then these boot modes will run at faster clock speeds. If the system design utilizes faster peripherals or these boot modes are not used, CLKIN values higher than 12.288 MHz can be used. **Note:** the CLKIN pin operates at the same voltage as the DV_{DDIO} supply (1.8-, 2.5-, 2.8-, or 3.3-V).

In this configuration the RTC oscillator can be optionally disabled by connecting RTC_XI to CV_{DDRTC} and RTC_XO to ground (V_{SS}). However, when the RTC oscillator is disabled the RTC registers starting at I/O address 1900h will not be accessible. This includes the RTC Power Management Register which provides control to the on-chip LDOs and WAKEUP and RTC_CLKOUT pins. **Note:** the RTC must still be powered even if the RTC oscillator is disabled.

For more details on the RTC on-chip oscillator, see Section 6.4.1, *Real-Time Clock (RTC) On-Chip Oscillator With External Crystal*.

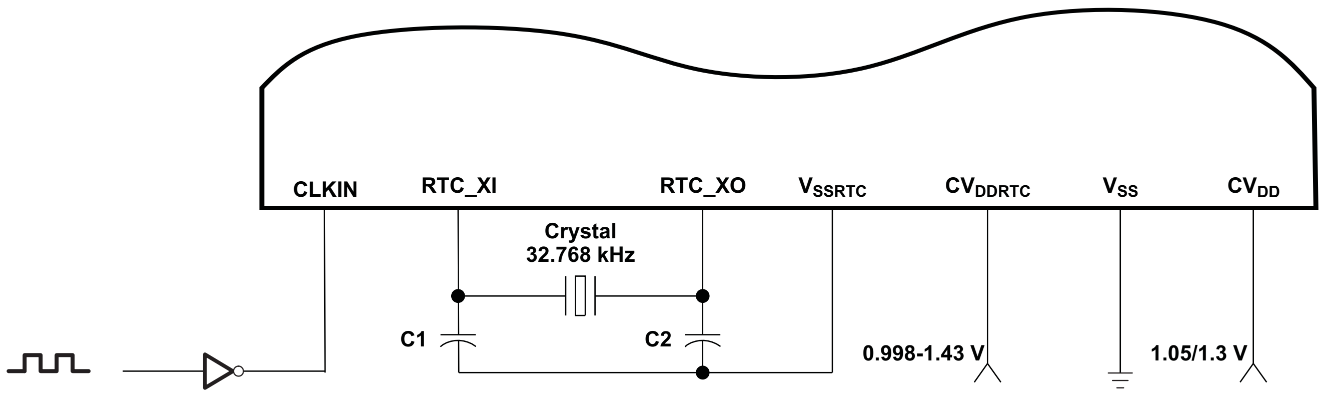


Figure 6-4. LVCMOS-Compatible Clock Input With RTC Oscillator Enabled

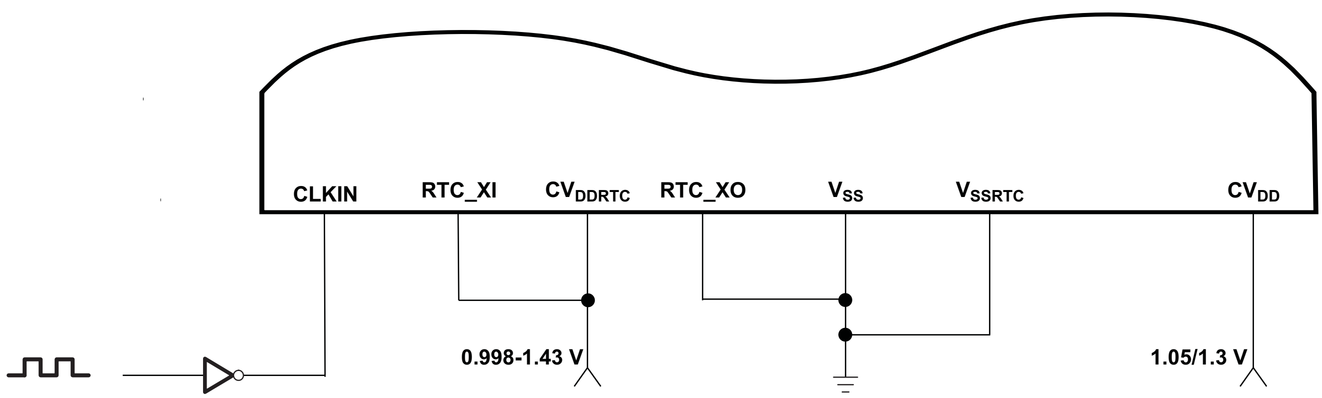


Figure 6-5. LVCMOS-Compatible Clock Input With RTC Oscillator Disabled

6.4.3 USB On-Chip Oscillator With External Crystal (Optional)

When using the USB, the USB on-chip oscillator requires an external 12-MHz crystal connected across the USB_MXI and USB_MXO pins, along with two load capacitors, as shown in Figure 6-6. The external crystal load capacitors must be connected only to the USB oscillator ground pin (USB_V_{SSOSC}). ***Do not*** connect to board ground (VSS). The USB_V_{DDOSC} pin can be connected to the same power supply as USB_V_{DDA3P3}.

The USB on-chip oscillator can be permanently disabled, via tie-offs, if the USB peripheral is not being used. To permanently disable the USB oscillator, connect the USB_MXI pin to ground (V_{SS}) and leave the USB_MXO pin unconnected. The USB oscillator power pins (USB_V_{DDOSC} and USB_V_{SSOSC}) should also be connected to ground.

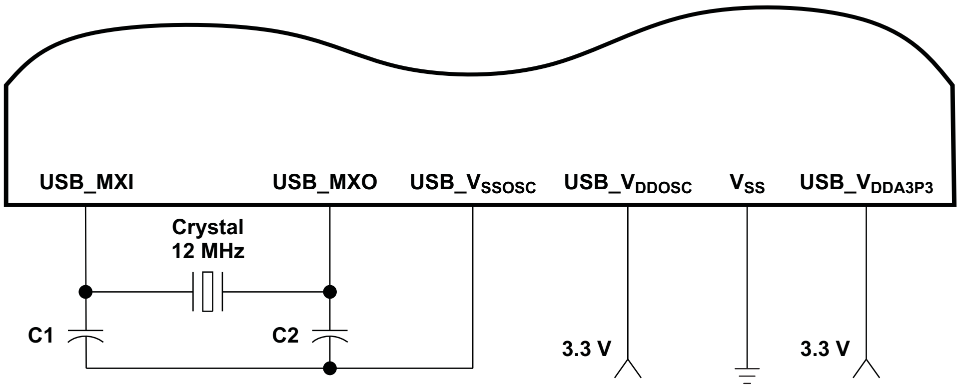


Figure 6-6. 12-MHz USB Oscillator

The crystal should be in fundamental-mode operation, and parallel resonant, with a maximum effective series resistance (ESR) specified in Table 6-2. The load capacitors, C1 and C2 are the total capacitance of the circuit board and components, excluding the IC and crystal. The load capacitor value is usually approximately twice the value of the crystal's load capacitance, CL, which is specified in the crystal manufacturer's datasheet and should be chosen such that the equation below is satisfied. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (USB_MXI and USB_MXO) and to the USB_V_{SSOSC} pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

Table 6-2. Input Requirements for Crystal on the 12-MHz USB Oscillator

PARAMETER	MIN	NOM	MAX	UNIT
Start-up time (from power up until oscillating at stable frequency of 12 MHz)(1)		0.100	10	ms
Oscillation frequency		12		MHz
ESR			100	Ω
Frequency stability(2)			±100	ppm
Maximum shunt capacitance			5	pF
Maximum crystal drive			330	μW

(1) The startup time is highly dependent on the ESR and the capacitive load of the crystal.
(2) If the USB is used, a 12-MHz, ±100-ppm crystal is recommended.

6.5 Clock PLLs

The VC5505 DSP uses a software-programmable PLL to generate frequencies required by the CPU, DMA, and peripherals. The reference clock for the PLL is taken from either the CLKIN pin or the RTC on-chip oscillator (as specified through the CLK_SEL pin).

6.5.1 PLL Device-Specific Information

There is a minimum and maximum operating frequency for CLKIN, PLLOUT, and the system clock (SYSCLK). The system clock generator must be configured not to exceed any of these constraints documented in this section (certain combinations of external clock inputs, internal dividers, and PLL multiply ratios might not be supported).

Table 6-3. PLLC1 Clock Frequency Ranges

CLOCK SIGNAL NAME	CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
	MIN	MAX	MIN	MAX	
CLKIN(1)		11.2896 12 12.288		11.2896 12 12.288	MHz
RTC Clock		32.768		32.768	KHz
PLLIN	32.768	170	32.768	170	KHz
PLLOUT	60	120	60	120	MHz
SYSCLK	0.032768	60	0.032768	100	MHz
PLL_LOCKTIME	4		4		ms

(1) These CLKIN values are used when the CLK_SEL pin = 1.

The PLL has a lock time requirements that must be followed. The PLL lock time is the amount of time needed for the PLL to complete its phase-locking sequence.

6.5.2 Clock PLL Considerations With External Clock Sources

If the CLKIN pin is used to provide the reference clock to the PLL, to minimize the clock jitter a single clean power supply should power both the VC5505 device and the external clock oscillator circuit. The minimum CLKIN rise and fall times should also be observed. For the input clock timing requirements, see Section 6.5.3, *Clock PLL Electrical Data/Timing (Input and Output Clocks)*.

Rise/fall times, duty cycles (high/low pulse durations), and the load capacitance of the external clock source must meet the device requirements in this data manual (see Section 5.3, *Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature*, and Section 6.5.3, *Clock PLL Electrical Data/Timing (Input and Output Clocks)*.

6.5.3 Clock PLL Electrical Data/Timing (Input and Output Clocks)

Table 6-4. Timing Requirements for CLKIN(1) (2) (see Figure 6-7)

NO.			CV_{DD} = 1.05 V			CV_{DD} = 1.3 V			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
1	$t_{c(CLKIN)}$	Cycle time, external clock driven on CLKIN		88.577, 83.333, or 81.380	16.67		88.577, 83.333, or 81.380	10	ns
2	$t_{w(CLKINH)}$	Pulse width, CLKIN high	0.466 * $t_{c(CLKIN)}$			0.466 * $t_{c(CLKIN)}$			ns
3	$t_{w(CLKINL)}$	Pulse width, CLKIN low	0.466 * $t_{c(CLKIN)}$			0.466 * $t_{c(CLKIN)}$			ns
4	$t_{t(CLKIN)}$	Transition time, CLKIN			0.34 * $t_{c(CLKIN)}$			0.34 * $t_{c(CLKIN)}$	ns

(1) The CLKIN frequency and PLL multiply factor should be chosen such that the resulting clock frequency is within the specific range for CPU operating frequency.
(2) The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.

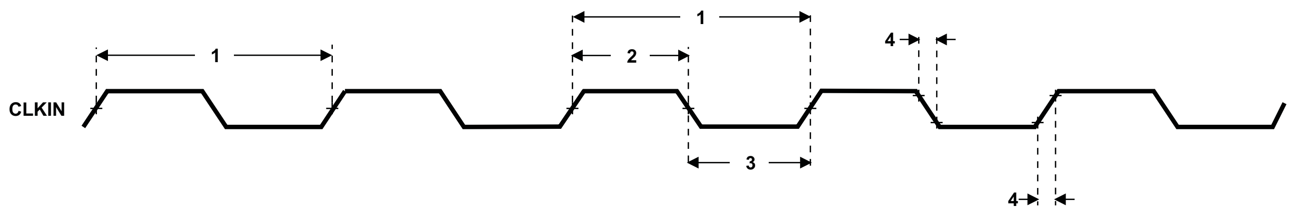


Figure 6-7. CLKIN Timing

Table 6-5. Switching Characteristics Over Recommended Operating Conditions for CLKOUT(1) (2) (see Figure 6-8)

NO.	PARAMETER		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(CLKOUT)}$	Cycle time, CLKOUT	P	16.67	P	10	ns
2	$t_{w(CLKOUTH)}$	Pulse duration, CLKOUT high	7.497	9.163	4.5	5.5	ns
3	$t_{w(CLKOUTL)}$	Pulse duration, CLKOUT low	7.497	9.163	4.5	5.5	ns
4	$t_{t(CLKOUTR)}$	Transition time (rise), CLKOUT(3)		5		5	ns
5	$t_{t(CLKOUTF)}$	Transition time (fall), CLKOUT(3)		5		5	ns

(1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
(2) P = 1/SYSCLK clock frequency in nanoseconds (ns). For example, when SYSCLK frequency is 100 MHz, use P = 10 ns.
(3) Transition time is measured with the slew rate set to FAST and DV_{DDIO} = 1.65 V. (For more detailed information, see the Section 4.6.5 , *Output Slew Rate Control Register (OSRCR) [1C16h].*).

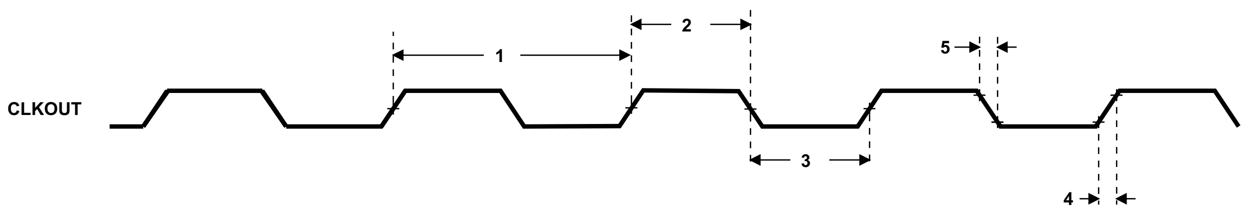


Figure 6-8. CLKOUT Timing

6.6 Direct Memory Access (DMA) Controller

The DMA controller is used to move data among internal memory, external memory, and peripherals without intervention from the CPU and in the background of CPU operation.

The DSP includes a total of four DMA controllers. Aside from the DSP resources they can access, all four DMA controllers are identical.

The DMA controller has the following features:

- Operation that is independent of the CPU.
- Four channels, which allow the DMA controller to keep track of the context of four independent block transfers.
- Event synchronization. DMA transfers in each channel can be made dependent on the occurrence of selected events.
- An interrupt for each channel. Each channel can send an interrupt to the CPU on completion of the programmed transfer.
- A dedicated clock idle domain. The four device DMA controllers can be put into a low-power state by independently turning off their input clocks.

6.6.1 DMA Channel Synchronization Events

The DMA controllers allow activity in their channels to be synchronized to selected events. The DSP supports 20 separate synchronization events and each channel can be tied to separate sync events independent of the other channels. Synchronization events are selected by programming the CHnEVT field in the DMAn channel event source registers (DMAnCESR1 and DMAnCESR2).

6.7 Reset

Supports only one type of reset, device reset.

The VC5505 has two main types of reset: hardware reset and software reset.

Hardware reset is responsible for initializing all key states of the device. It occurs whenever the $\overline{\text{RESET}}$ pin is asserted or when the internal power-on-reset (POR) circuit deasserts an internal signal called POWERGOOD. VC5505 device's internal POR is a voltage comparator that monitors the DSP_LDOO pin voltage and generates the internal POWERGOOD signal. POWERGOOD is asserted when the DSP_LDOO voltage is above a minimum threshold voltage provided by the bandgap. On VC5505 , the voltage comparator circuit is present and active in the POR circuit even though the DSP_LDO is not currently supported. The $\overline{\text{RESET}}$ pin and the POWERGOOD signal are internally combined with a logical AND gate to produce an (active low) hardware reset (see Figure 6-9, *Power-On Reset Timing Requirements* and Figure 6-10, *Reset Timing Requirements*).

There are two types of software reset: the CPU's software reset instruction and the software control of the peripheral reset signals. For more information on the CPU's software reset instruction, see the *TMS320C55x CPU 3.0 CPU* Reference Guide (literature number: SWPU073). In all VC5505 documentation, all references to "reset" refer to hardware reset. Any references to software reset will explicitly state software reset.

The VC5505 RTC has one additional type of reset, a power-on-reset (POR) for the registers in the RTC core. This POR monitors the voltage of CV_{DD_RTC} and resets the RTC registers when power is first applied to the RTC core.

6.7.1 Power-On Reset (POR) Circuits

The VC5505 device includes two power-on reset (POR) circuits, one for the RTC (RTC POR) and another for the rest of the chip (MAIN POR).

6.7.1.1 RTC Power-On Reset (POR)

The RTC POR ensures that the flip-flops in the CV_{DD_RTC} power domain have an initial state upon powerup. In particular, the RTCNOPWR register is reset by this POR and is used to indicate that the RTC time registers need to be initialized with the current time and date when power is first applied.

6.7.1.2 Main Power-On Reset (POR)

The VC5505 device includes an analog power-on reset (POR) circuit that keeps the DSP in reset until specific voltages have reached predetermined levels. The output of the POR circuit, POWERGOOD, is held low until the following conditions are satisfied:

- ANA_LDOI is powered and the bandgap is active for at least approximately 8 ms
- VDD_ANA is powered for at least approximately 4 ms
- DSP_LDOO is powered and above a threshold of approximately 900 mV (see **Note:**)

Once these conditions are met, the internal POWERGOOD signal is set high. The POWERGOOD signal is internally combined with the $\overline{\text{RESET}}$ pin signal, via an AND-gate, to produce the DSP subsystem's global reset. This global reset is the hardware reset for the whole chip, except the RTC. When the global reset is deasserted (high), the boot sequence starts. For more detailed information on the boot sequence, see Section 4.4, *Boot Sequence*.

Note: The DSP_LDO is not supported on VC5505 device, but it's output voltage is still monitored by the MAIN POR and must reach, and remain, higher than the POR's threshold for the POWERGOOD signal to be high. The DSP_LDOO pin must be left floating and be properly bypassed as specified in the DSP_LDOO entry in Table 3-19, *Regulators and Power Management Terminal Functions*. By leaving this pin floating, the VC5505 's internal circuits provide the necessary voltage above the POR's threshold for POWERGOOD.

6.7.1.3 Reset Pin (RESET)

The VC5505 can receive an external reset signal on the RESET pin. As specified above in Section 6.7.1.2, *Main Power-On Reset*, the RESET pin is combined with the internal POWERGOOD signal, that is generated by the MAIN POR, via an AND-gate. The output of the AND gate provides the hardware reset to the chip. The RESET pin may be tied high and the MAIN POR will provide the hardware reset, or the RESET pin may be externally generated.

Once the internal hardware reset, from the MAIN POR and the RESET pin, goes high, the DSP clock generator is enabled and the DSP starts the boot sequence. For more information on the boot sequence, see Section 4.4, *Boot Sequence*.

6.7.2 Pin Behaviors at Reset

During normal operation, pins are controlled by the respective peripheral selected in the External Bus Selection Register (EBSR) register. During power-on reset and reset, the behavior of the output pins changes and is categorized as follows:

- **High Group:** EM_CS4, EM_CS5, EM_CS2, EM_CS3, EM_DQM0, EM_DQM1, EM_OE, EM_WE, LCD_RS/SPI_CS3, RSV15, RSV14, XF
- **Low Group:** LCD_EN_RDB/SPI_CLK, EM_R/W, MMC0_CLK/I2S0_CLK/GP[0], MMC1_CLK/I2S1_CLK/GP[6], RSV12
- **Z Group:** EM_D[15:0], EMU[1:0], SCL, SDA, LCD_D[0]/SPI_RX, LCD_D[1]/SPI_TX, LCD_D[10]/I2S2_RX/GP[20]/SPI_RX, LCD_D[11]/I2S2_DX/GP[27]/SPI_TX, LCD_D[12]/I2S2_RTS/GP[28]/I2S3_CLK, LCD_D[13]/I2S2_CTS/GP[29]/I2S3_RS, LCD_D[14]/I2S2_RXD/GP[30]/I2S3_RX, LCD_D[15]/I2S2_TXD/GP[31]/I2S3_DX, LCD_D[2]/GP[12], LCD_D[3]/GP[13], LCD_D[4]/GP[14], LCD_D[5]/GP[15], LCD_D[6]/GP[16], LCD_D[7]/GP[17], LCD_D[8]/I2S2_CLK/GP[18]/SPI_CLK,LCD_D[9]/I2S2_FS/GP[19]/SPI_CS0, RTC_CLKOUT, MMC0_CMD/I2S0_FS/GP[1], MMC0_D0/I2S0_DX/GP[2], MMC0_D1/I2S0_RX/GP[3], MMC0_D2/GP[4], MMC0_D3/GP[5], MMC1_CMD/I2S1_FS/GP[7], MMC1_D0/I2S1_DX/GP[8], MMC1_D1/I2S1_RX/GP[9], MMC1_D2/GP[10], MMC1_D3/GP[11], TDO, WAKEUP
- **CLKOUT Group:** CLKOUT, LCD_CS1_E1/SPI_CS1
- **SYNCH 0→1 Group:** LCD_CS0_E0/SPI_CS0, LCD_RW_WRB/SPI_CS2, RSV13
- **SYNCH 1→0 Group:** RSV10, RSV11
- **SYNCH X→1 Group:** EM_BA[1:0]
- **SYNCH X→0 Group:** EM_A[20:0]

6.7.3 Reset Electrical Data/Timing

Table 6-6. Timing Requirements for Reset[(1)] (see Figure 6-9 and Figure 6-10)

NO.			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{w(RSTL)}$	Pulse duration, $\overline{\text{RESET}}$ low	3P		3P		ns

(1) (1)P = 1/SYSCLK clock frequency in ns. For example, if SYSCLK = 12 MHz, use P = 83.3 ns. In IDLE3 mode the system clock generator is bypassed and the SYSCLK frequency is equal to either CLKIN or the RTC clock frequency depending on CLK_SEL.

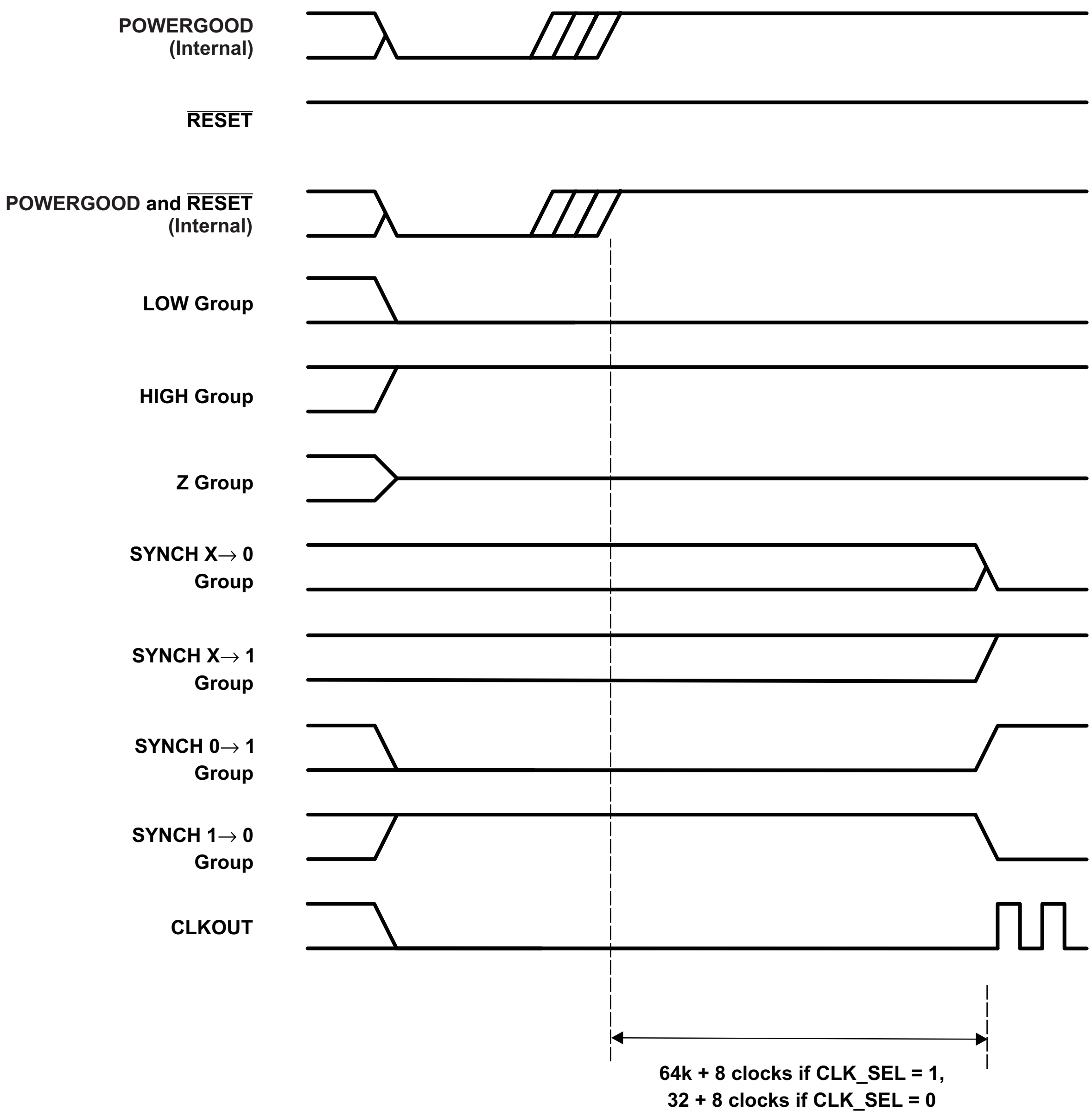


Figure 6-9. Power-On Reset Timing Requirements

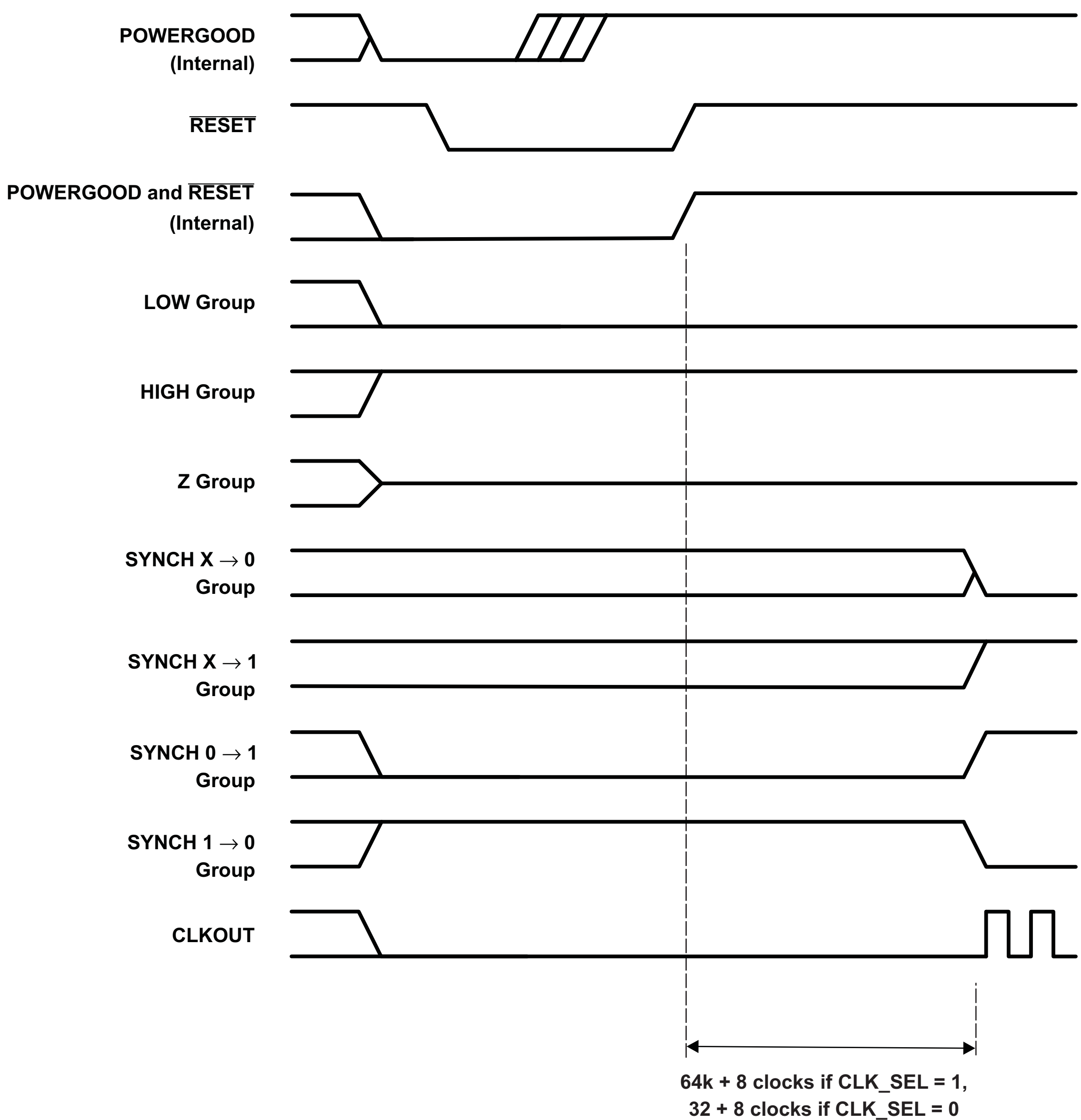


Figure 6-10. Reset Timing Requirements

6.8 Wake-up Events, Interrupts, and XF

The VC5505 device has a number of interrupts to service the needs of its peripherals. The interrupts can be selectively enabled or disabled.

6.8.1 Interrupts Electrical Data/Timing

Table 6-7. Timing Requirements for Interrupts[1] (see Figure 6-11)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V MIN	MAX	UNIT
1	$t_{w(INTH)}$	Pulse duration, interrupt high CPU active	2P		ns
2	$t_{w(INTL)}$	Pulse duration, interrupt low CPU active	2P		ns

(1) P = 1/SYSCLK clock frequency in ns. For example, when running parts at 100 MHz, use P = 10 ns.

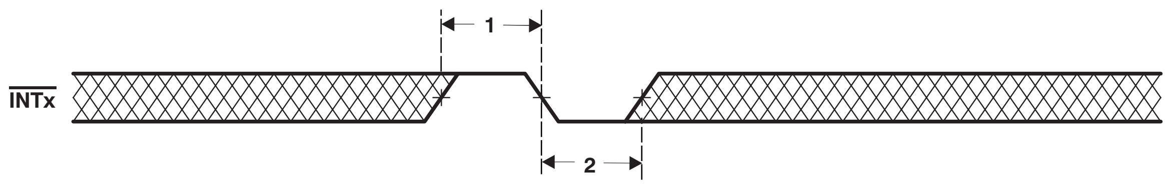


Figure 6-11. External Interrupt Timings

6.8.2 Wake-Up From IDLE Electrical Data/Timing

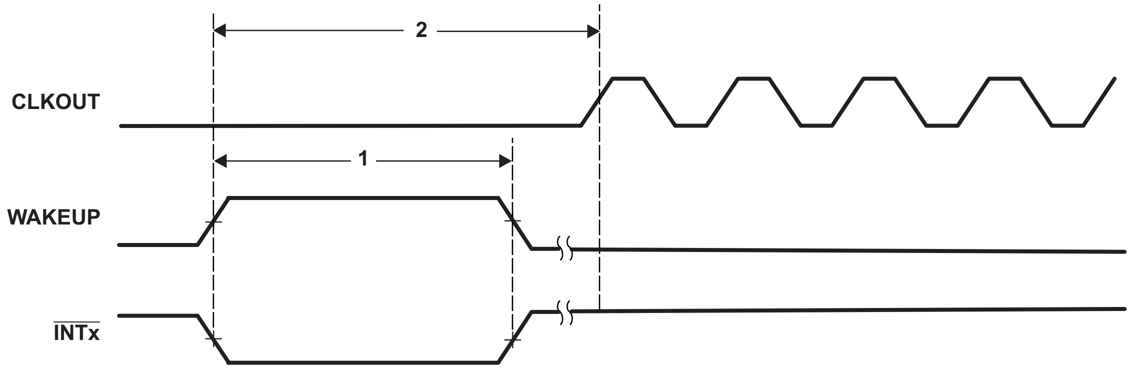
Table 6-8. Timing Requirements for Wake-Up From IDLE (see Figure 6-12)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V MIN	MAX	UNIT
1	$t_{w(WKPL)}$	Pulse duration, WAKEUP or $\overline{INTx}$ low, SYSCLKDIS = 1	10		ns

Table 6-9. Switching Characteristics Over Recommended Operating Conditions For Wake-Up From IDLE[1] [2] [3] (see Figure 6-12)

NO.	PARAMETER			CV_{DD} = 1.05 V CV_{DD} = 1.3 V MIN	TYP	MAX	UNIT
2	$t_{d(WKEVTH-CKLGEN)}$	Delay time, Wake-Up event high to CPU active	IDLE3 Mode with SYSCLKDIS = 1, WAKEUP or $\overline{INTx}$ event, CLK_SEL = 1	P			ns
			IDLE3 Mode with SYSCLKDIS = 1, WAKEUP or $\overline{INTx}$ event, CLK_SEL = 0	C			ns
			IDLE2 Mode; $\overline{INTx}$ event	3P			ns

(1) P = 1/SYSCLK clock frequency in ns. For example, when running parts at 100 MHz, P = 10 ns.
(2) C = 1/RTCCLK= 30.5 µs. RTCCLK is the clock output of the 32.768-kHz RTC oscillator.
(3) Assumes the internal LDOs are used with a 0.1uF bandgap capacitor.



A. INT[1:0] can only be used as a wake-up event for IDLE3 and IDLE2 modes.
B. RTC interrupt (internal signal) can be used as wake-up event for IDLE3 and IDLE2 modes.
C. Any unmasked interrupt can be used to exit the IDLE2 mode.
D. CLKOUT reflects either the CPU clock, SAR, USB PHY, or PLL clock dependent on the setting of the CLOCKOUT Clock Source Register. For this diagram, CLKOUT refers to the CPU clock.

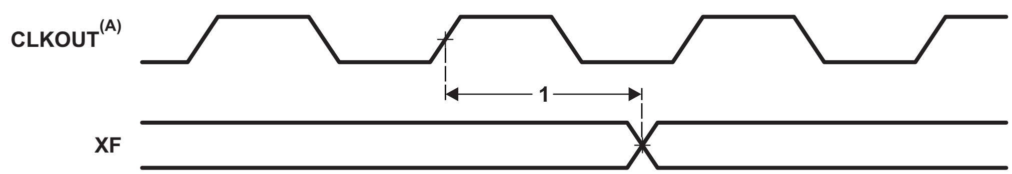
Figure 6-12. Wake-Up From IDLE Timings

6.8.3 XF Electrical Data/Timing

Table 6-10. Switching Characteristics Over Recommended Operating Conditions For XF(1) (2) (see Figure 6-13)

NO.	PARAMETER		CV_{DD} = 1.05 V CV_{DD} = 1.3 V MIN	MAX	UNIT
1	$t_{d(XF)}$	Delay time, CLKOUT high to XF high	0	10.2	ns

(1) P = 1/SYSCLK clock frequency in ns. For example, when running parts at 100 MHz, P = 10 ns.
(2) C = 1/RTCCLK= 30.5 µs. RTCCLK is the clock output of the 32.768-kHz RTC oscillator.



A. CLKOUT reflects either the CPU clock, SAR, USB PHY, or PLL clock dependent on the setting of the CLOCKOUT Clock Source Register. For this diagram, CLKOUT refers to the CPU clock.

Figure 6-13. XF Timings

6.9 External Memory Interface (EMIF)

VC5505 supports several memory and external device interfaces, including: NOR Flash, NAND Flash, and SRAM.

The EMIF provides an 8-bit or 16-bit data bus, an address bus width up to 21 bits, and 4 chip selects, along with memory control signals.

The EM_A[20:15] address signals are multiplexed with the GPIO peripheral and controlled by the External Bus Selection Register (EBSR). For more detail on the pin muxing, see the Section 4.6.1, *External Bus Selection Register (EBSR)*.

6.9.1 EMIF Asynchronous Memory Support

The EMIF supports asynchronous:

- SRAM memories

- NAND Flash memories
- NOR Flash memories

The EMIF data bus can be configured for both 8- or 16-bit width. The device supports up to 21 address lines and four external wait/interrupt inputs. Up to four asynchronous chip selects are supported by EMIF (EM_CS[5:2]).

Each chip select has the following individually programmable attributes:

- Data bus width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turn around time
- Extended Wait Option With Programmable Timeout
- Select Strobe Option
- NAND flash controller supports 1-bit and 4-bit ECC calculation on blocks of 512 bytes

6.9.2 EMIF Peripheral Register Description(s)

Table 6-11 shows the EMIF registers.

Table 6-11. External Memory Interface (EMIF) Peripheral Registers(1)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
1000h	REV	Revision Register
1001h	STATUS	Status Register
1004h	AWCCR1	Asynchronous Wait Cycle Configuration Register 1
1005h	AWCCR2	Asynchronous Wait Cycle Configuration Register 2
1010h	ACS2CR1	Asynchronous CS2 Configuration Register 1
1011h	ACS2CR2	Asynchronous CS2 Configuration Register 2
1014h	ACS3CR1	Asynchronous CS3 Configuration Register 1
1015h	ACS3CR2	Asynchronous CS3 Configuration Register 2
1018h	ACS4CR1	Asynchronous CS4 Configuration Register 1
1019h	ACS4CR2	Asynchronous CS4 Configuration Register 2
101Ch	ACS5CR1	Asynchronous CS5 Configuration Register 1
101Dh	ACS5CR2	Asynchronous CS5 Configuration Register 2
1040h	EIRR	EMIF Interrupt Raw Register
1044h	EIMR	EMIF Interrupt Mask Register
1048h	EIMSR	EMIF Interrupt Mask Set Register
104Ch	EIMCR	EMIF Interrupt Mask Clear Register
1060h	NANDFCR	NAND Flash Control Register
1064h	NANDFSR1	NAND Flash Status Register 1
1065h	NANDFSR2	NAND Flash Status Register 2
1068h	PGMODECTRL1	Page Mode Control Register 1
1069h	PGMODECTRL2	Page Mode Control Register 2
1070h	NCS2ECC1	NAND Flash CS2 1-Bit ECC Register 1
1071h	NCS2ECC2	NAND Flash CS2 1-Bit ECC Register 2
1074h	NCS3ECC1	NAND Flash CS3 1-Bit ECC Register 1
1075h	NCS3ECC2	NAND Flash CS3 1-Bit ECC Register 2
1078h	NCS4ECC1	NAND Flash CS4 1-Bit ECC Register 1

(1) Before reading or writing to the EMIF registers, be sure to set the BYTEMODE bits to 00b in the EMIF system control register to enable word accesses to the EMIF registers.

Table 6-11. External Memory Interface (EMIF) Peripheral Registers [(1)] (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
1079h	NCS4ECC2	NAND Flash CS4 1-Bit ECC Register 2
107Ch	NCS5ECC1	NAND Flash CS5 1-Bit ECC Register 1
107Dh	NCS5ECC2	NAND Flash CS5 1-Bit ECC Register 2
10BCh	NAND4BITECCLOAD	NAND Flash 4-Bit ECC Load Register
10C0h	NAND4BITECC1	NAND Flash 4-Bit ECC Register 1
10C1h	NAND4BITECC2	NAND Flash 4-Bit ECC Register 2
10C4h	NAND4BITECC3	NAND Flash 4-Bit ECC Register 3
10C5h	NAND4BITECC4	NAND Flash 4-Bit ECC Register 4
10C8h	NAND4BITECC5	NAND Flash 4-Bit ECC Register 5
10C9h	NAND4BITECC6	NAND Flash 4-Bit ECC Register 6
10CCh	NAND4BITECC7	NAND Flash 4-Bit ECC Register 7
10CDh	NAND4BITECC8	NAND Flash 4-Bit ECC Register 8
10D0h	NANDERRADD1	NAND Flash 4-Bit ECC Error Address Register 1
10D1h	NANDERRADD2	NAND Flash 4-Bit ECC Error Address Register 2
10D4h	NANDERRADD3	NAND Flash 4-Bit ECC Error Address Register 3
10D5h	NANDERRADD4	NAND Flash 4-Bit ECC Error Address Register 4
10D8h	NANDERRVAL1	NAND Flash 4-Bit ECC Error Value Register 1
10D9h	NANDERRVAL2	NAND Flash 4-Bit ECC Error Value Register 2
10DCh	NANDERRVAL3	NAND Flash 4-Bit ECC Error Value Register 3
10DDh	NANDERRVAL4	NAND Flash 4-Bit ECC Error Value Register 4

6.9.3 EMIF Electrical Data/Timing CV_{DD} = 1.05 V, DV_{DDEMIF} = 3.3/2.8/2.5/1.8 V

Table 6-12. Timing Requirements for EMIF Asynchronous Memory[1] (see Figure 6-14, Figure 6-16, and Figure 6-17)

NO.			CV_{DD} = 1.05 V DV_{DDEMIF} = 3.3/2.8/2.5/1.8 V MIN	NOM	MAX	UNIT
READS and WRITES						
2	$t_{w(EM\_WAIT)}$	Pulse duration, EM_WAITx assertion and deassertion	2E			ns
READS						
12	$t_{su(EMDV-EMOEH)}$	Setup time, EM_D[15:0] valid before $\overline{EM\_OE}$ high	14.5			ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EM_D[15:0] valid after $\overline{EM\_OE}$ high	0			ns
14	$t_{su\ (EMOEL-EMWAIT)}$	Setup Time, EM_WAITx asserted before end of Strobe Phase[2]	4E + 9			ns
WRITES						
26	$t_{su\ (EMWEL-EMWAIT)}$	Setup Time, EM_WAITx asserted before end of Strobe Phase[2]	4E + 9			ns

(1) E = SYSCLK period in ns, if EMIF is set for "full rate" ***or*** E = SYSCLK/2 period in ns, if EMIF is set for "half rate" as defined by bit 14 of the EMIF Status register (0x1001h). For example, when EMIF is set to full rate and SYSCLK is selected and set to 100 MHz, E = 10 ns.
(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAITx must be asserted to add extended wait states. Figure 6-16 and Figure 6-17 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 6-13. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory[(1)] [(2)] (see Figure 6-15 and Figure 6-17)[(3)]

NO.	PARAMETER		CVDD = 1.05 V DVDDEMIF = 3.3/2.8/2.5/1.8 V MIN	NOM	MAX	UNIT
READS and WRITES						
1	$t_{d(TURNAROUND)}$	Turn around time	(TA)*E - 9	(TA)*E	(TA)*E + 9	ns
READS						
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH)*E - 9	(RS+RST+RH)*E	(RS+RST+RH)*E + 9	ns
		EMIF read cycle time (EW = 1)	(RS+RST+RH+(EWC*16))*E - 9	(RS+RST+RH+(EWC*16))*E	(RS+RST+RH+(EWC*16))*E + 9	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, EM_CS[5:2] low to EM_OE low (SS = 0)	(RS)*E-9	(RS)*E	(RS)*E+9	ns
		Output setup time, EM_CS[5:2] low to EM_OE low (SS = 1)	-9	0	+9	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, EM_OE high to EM_CS[5:2] high (SS = 0)	(RH)*E - 9	(RH)*E	(RH)*E + 9	ns
		Output hold time, EM_OE high to EM_CS[5:2] high (SS = 1)	-9	0	+9	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EM_BA[1:0] valid to EM_OE low	(RS)*E-9	(RS)*E	(RS)*E+9	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, EM_OE high to EM_BA[1:0] invalid	(RH)*E-9	(RH)*E	(RH)*E+9	ns
8	$t_{su(EMBAV-EMOEL)}$	Output setup time, EM_A[20:0] valid to EM_OE low	(RS)*E-9	(RS)*E	(RS)*E+9	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, EM_OE high to EM_A[20:0] invalid	(RH)*E-9	(RH)*E	(RH)*E+9	ns
10	$t_{w(EMOEL)}$	EM_OE active low width (EW = 0)	(RST)*E-9	(RST)*E	(RST)*E+9	ns
		EM_OE active low width (EW = 1)	(RST+(EWC*16))*E-9	(RST+(EWC*16))*E	(RST+(EWC*16))*E+9	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EM_WAITx deasserted to EM_OE high	4E-9	4E	4E+9	ns
WRITES						
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH)*E-9	(WS+WST+WH)*E	(WS+WST+WH)*E+9	ns
		EMIF write cycle time (EW = 1)	(WS+WST+WH+(EWC*16))*E - 9	(WS+WST+WH+(EWC*16))*E	(WS+WST+WH+(EWC*16))*E + 9	ns
16	$t_{su(EMCSL-EMWEL)}$	Output setup time, EM_CS[5:2] low to EM_WE low (SS = 0)	(WS)*E - 9	(WS)*E	(WS)*E + 9	ns
		Output setup time, EM_CS[5:2] low to EM_WE low (SS = 1)	-9	0	+9	ns
17	$t_{h(EMWEH-EMCSH)}$	Output hold time, EM_WE high to EM_CS[5:2] high (SS = 0)	(WH)*E-9	(WH)*E	(WH)*E+9	ns
		Output hold time, EM_WE high to EM_CS[5:2] high (SS = 1)	-9	0	+9	ns
18	$t_{su(EMBAV-EMWEL)}$	Output setup time, EM_BA[1:0] valid to EM_WE low	(WS)*E-9	(WS)*E	(WS)*E+9	ns
19	$t_{h(EMWEH-EMBAIV)}$	Output hold time, EM_WE high to EM_BA[1:0] invalid	(WH)*E-9	(WH)*E	(WH)*E+9	ns
20	$t_{su(EMAV-EMWEL)}$	Output setup time, EM_A[20:0] valid to EM_WE low	(WS)*E-9	(WS)*E	(WS)*E+9	ns
21	$t_{h(EMWEH-EMAIV)}$	Output hold time, EM_WE high to EM_A[20:0] invalid	(WH)*E-9	(WH)*E	(WH)*E+9	ns

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Configuration and Asynchronous Wait Cycle Configuration Registers.
(2) E = SYSCLK period in ns, if EMIF is set for "full rate" ***or*** E = SYSCLK/2 period in ns, if EMIF is set for "half rate" as defined by bit 14 of the EMIF Status register (0x1001h). For example, when EMIF is set to full rate and SYSCLK is selected and set to 100 MHz, E = 10 ns.
(3) EWC = external wait cycles determined by EM_WAITx input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register.

Table 6-13. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory (1) (2) (see Figure 6-15 and Figure 6-17) (3) (continued)

NO.	PARAMETER		CV_{DD} = 1.05 V DV_{DDEMIF} = 3.3/2.8/2.5/1.8 V			UNIT
			MIN	NOM	MAX	
22	$t_{w(EMWEL)}$	$\overline{EM\_WE}$ active low width (EW = 0)	(WST)*E-9	(WST)*E	(WST)*E+9	ns
		$\overline{EM\_WE}$ active low width (EW = 1)	(WST+(EWC*16))*E-9	(WST+(EWC*16))*E	(WST+(EWC*16))*E+9	ns
23	$t_{d(EMWAITH-EMWEH)}$	Delay time from EM_WAITx deasserted to $\overline{EM\_WE}$ high	3E-9	4E	4E+9	ns
24	$t_{su(EMDV-EMWEL)}$	Output setup time, EM_D[15:0] valid to $\overline{EM\_WE}$ low	(WS)*E-9	(WS)*E	(WS)*E+9	ns
25	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_D[15:0] invalid	(WH)*E-9	(WH)*E	(WH)*E+9	ns

6.9.4 EMIF Electrical Data/Timing CV_{DD} = 1.3 V, DV_{DDEMIF} = 3.3/2.8/2.5/1.8 V

Table 6-14. Timing Requirements for EMIF Asynchronous Memory[1] (see Figure 6-14, Figure 6-16, and Figure 6-17)

NO.			CV_{DD} = 1.3 V DV_{DDEMIF} = 3.3/2.8/2.5/1.8 V MIN	NOM	MAX	UNIT
READS and WRITES						
2	$t_{w(EM\_WAIT)}$	Pulse duration, EM_WAITx assertion and deassertion	2E			ns
READS						
12	$t_{su(EMDV-EMOEH)}$	Setup time, EM_D[15:0] valid before $\overline{EM\_OE}$ high	11			ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EM_D[15:0] valid after $\overline{EM\_OE}$ high	0			ns
14	$t_{su\ (EMOEL-EMWAIT)}$	Setup Time, EM_WAITx asserted before end of Strobe Phase[2]	4E + 5			ns
WRITES						
26	$t_{su\ (EMWEL-EMWAIT)}$	Setup Time, EM_WAITx asserted before end of Strobe Phase[2]	4E + 5			ns

(1) E = SYSCLK period in ns, if EMIF is set for "full rate" ***or*** E = SYSCLK/2 period in ns, if EMIF is set for "half rate" as defined by bit 14 of the EMIF Status register (0x1001h). For example, when EMIF is set to full rate and SYSCLK is selected and set to 100 MHz, E = 10 ns.

(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAITx must be asserted to add extended wait states. Figure 6-16 and Figure 6-17 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 6-15. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory[1] [2] [3] (see Figure 6-14, Figure 6-16, and Figure 6-17)

NO.	PARAMETER		CV_{DD} = 1.3 V DV_{DDEMIF} = 3.3/2.8/2.5/1.8 V MIN	NOM	MAX	UNIT
	READS and WRITES					
1	$t_{d(TURNAROUND)}$	Turn around time	(TA)*E - 5	(TA)*E	(TA)*E + 5	ns
	READS					
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH)*E - 5	(RS+RST+RH)*E	(RS+RST+RH)*E + 5	ns
		EMIF read cycle time (EW = 1)	(RS+RST+RH+(EWC*16))*E - 5	(RS+RST+RH+(EWC*16))*E	(RS+RST+RH+(EWC*16))*E + 5	ns
4	$t_{su(EMCSL-EMOEL)}$	Output setup time, EM_CS[5:2] low to EM_OE low (SS = 0)	(RS)*E-5	(RS)*E	(RS)*E+5	ns
		Output setup time, EM_CS[5:2] low to EM_OE low (SS = 1)	-5	0	+5	ns
5	$t_{h(EMOEH-EMCSH)}$	Output hold time, EM_OE high to EM_CS[5:2] high (SS = 0)	(RH)*E - 5	(RH)*E	(RH)*E + 5	ns
		Output hold time, EM_OE high to EM_CE[5:2] high (SS = 1)	-5	0	+5	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EM_BA[1:0] valid to EM_OE low	(RS)*E-5	(RS)*E	(RS)*E+5	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, EM_OE high to EM_BA[1:0] invalid	(RH)*E-5	(RH)*E	(RH)*E+5	ns
8	$t_{su(EMAV-EMOEL)}$	Output setup time, EM_A[20:0] valid to EM_OE low	(RS)*E-5	(RS)*E	(RS)*E+5	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, EM_OE high to EM_A[20:0] invalid	(RH)*E-5	(RH)*E	(RH)*E+5	ns
10	$t_{w(EMOEL)}$	EM_OE active low width (EW = 0)	(RST)*E-5	(RST)*E	(RST)*E+5	ns
		EM_OE active low width (EW = 1)	(RST+(EWC*16))*E-5	(RST+(EWC*16))*E	(RST+(EWC*16))*E+5	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EM_WAITx deasserted to EM_OE high	4E-5	4E	4E+5	ns
	WRITES					
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH)*E-5	(WS+WST+WH)*E	(WS+WST+WH)*E+5	ns
		EMIF write cycle time (EW = 1)	(WS+WST+WH+(EWC*16))*E - 5	(WS+WST+WH+(EWC*16))*E	(WS+WST+WH+(EWC*16))*E + 5	ns
16	$t_{su(EMCSL-EMWEL)}$	Output setup time, EM_CS[5:2] low to EM_WE low (SS = 0)	(WS)*E - 5	(WS)*E	(WS)*E + 5	ns
		Output setup time, EM_CS[5:2] low to EM_WE low (SS = 1)	-5	0	+5	ns
17	$t_{h(EMWEH-EMCSH)}$	Output hold time, EM_WE high to EM_CS[5:2] high (SS = 0)	(WH)*E-5	(WH)*E	(WH)*E+5	ns
		Output hold time, EM_WE high to EM_CS[5:2] high (SS = 1)	-5	0	+5	ns
18	$t_{su(EMBAV-EMWEL)}$	Output setup time, EM_BA[1:0] valid to EM_WE low	(WS)*E-5	(WS)*E	(WS)*E+5	ns
19	$t_{h(EMWEH-EMBAIV)}$	Output hold time, EM_WE high to EM_BA[1:0] invalid	(WH)*E-5	(WH)*E	(WH)*E+5	ns
20	$t_{su(EMAV-EMWEL)}$	Output setup time, EM_A[20:0] valid to EM_WE low	(WS)*E-5	(WS)*E	(WS)*E+5	ns
21	$t_{h(EMWEH-EMAIV)}$	Output hold time, EM_WE high to EM_A[20:0] invalid	(WH)*E-5	(WH)*E	(WH)*E+5	ns

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Configuration and Asynchronous Wait Cycle Configuration Registers.

(2) E = SYSCLK period in ns, if EMIF is set for "full rate" ***or*** E = SYSCLK/2 period in ns, if EMIF is set for "half rate" as defined by bit 14 of the EMIF Status register (0x1001h). For example, when EMIF is set to full rate and SYSCLK is selected and set to 100 MHz, E = 10 ns.

(3) EWC = external wait cycles determined by EM_WAITx input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register.

Table 6-15. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory (1) (2) (3) (see Figure 6-14 , Figure 6-16 , and Figure 6-17) (continued)

NO.	PARAMETER		CV_{DD} = 1.3 V DV_{DDEMIF} = 3.3/2.8/2.5/1.8 V			UNIT
			MIN	NOM	MAX	
22	$t_{w(EMWEL)}$	$\overline{EM\_WE}$ active low width (EW = 0)	(WST)*E-5	(WST)*E	(WST)*E+5	ns
		$\overline{EM\_WE}$ active low width (EW = 1)	(WST+(EWC*16))*E-5	(WST+(EWC*16))*E	(WST+(EWC*16))*E+5	ns
23	$t_{d(EMWAITH-EMWEH)}$	Delay time from EM_WAITx deasserted to $\overline{EM\_WE}$ high	3E-5	4E	4E+5	ns
24	$t_{su(EMDV-EMWEL)}$	Output setup time, EM_D[15:0] valid to $\overline{EM\_WE}$ low	(WS)*E-5	(WS)*E	(WS)*E+5	ns
25	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_D[15:0] invalid	(WH)*E-5	(WH)*E	(WH)*E+5	ns

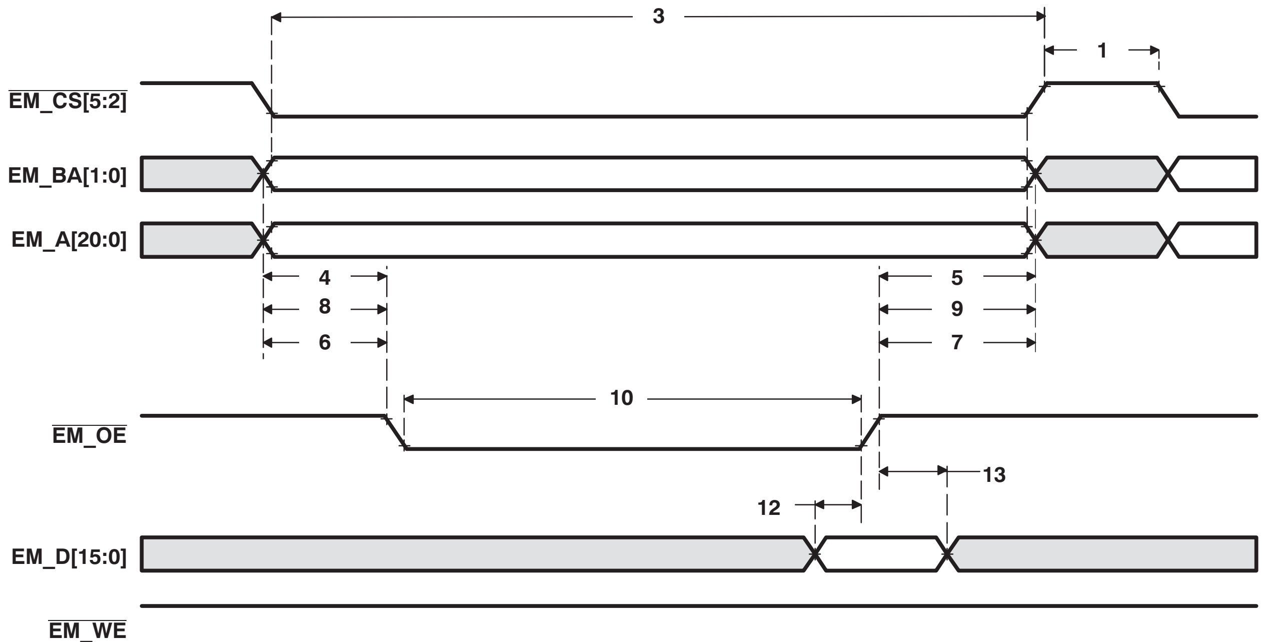


Figure 6-14. Asynchronous Memory Read Timing for EMIF

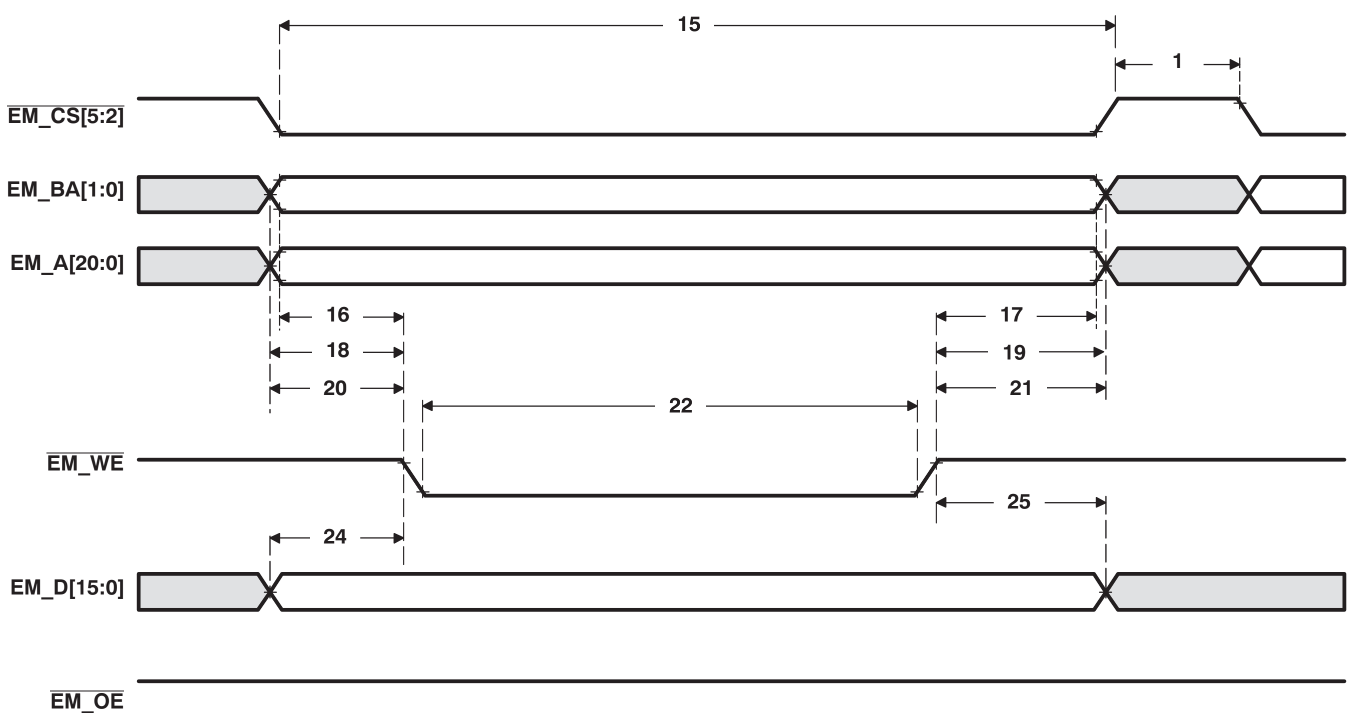


Figure 6-15. Asynchronous Memory Write Timing for EMIF

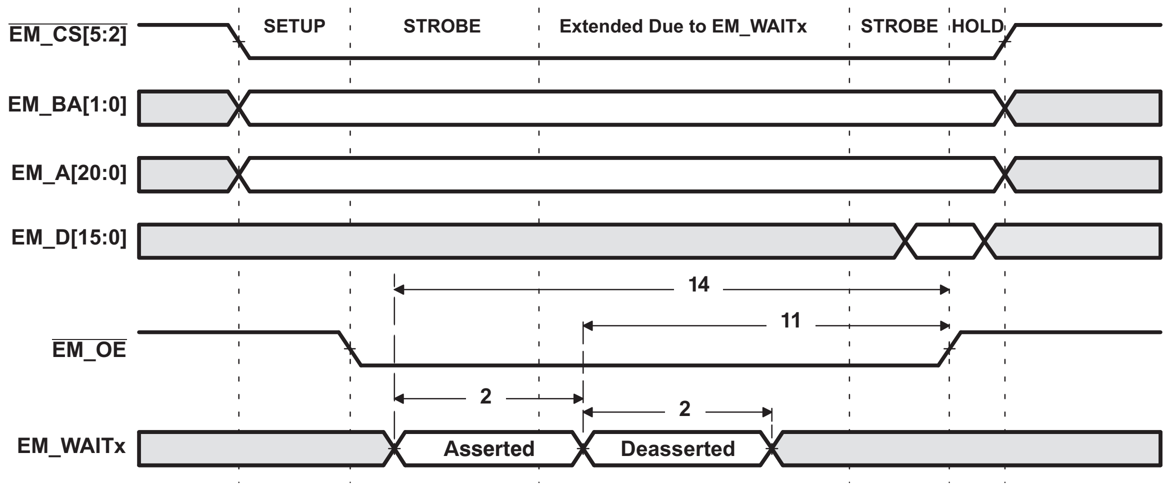


Figure 6-16. EM_WAITx Read Timing Requirements

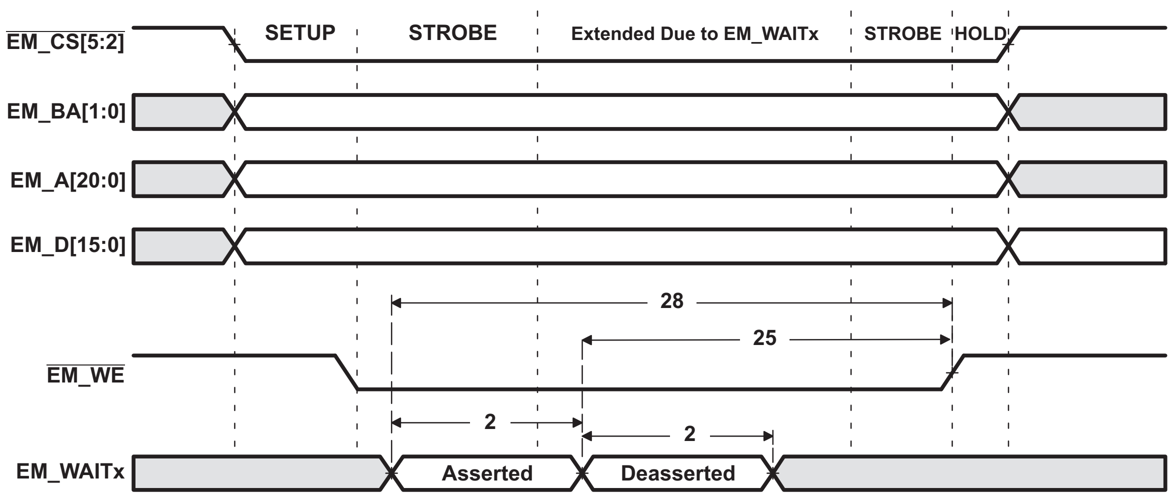


Figure 6-17. EM_WAITx Write Timing Requirements

6.10 Multimedia Card/Secure Digital (MMC/SD)

The VC5505 includes two MMC/SD controllers which are compliant with MMC V3.31, Secure Digital Part 1 Physical Layer Specification V2.0, and Secure Digital Input Output (SDIO) V3.3 specifications. The MMC/SD card controller supports these industry standards and assumes the reader is familiar with these standards.

Each VC5505 MMC/SD Controller has the following features:

- Multimedia Card/Secure Digital (MMC/SD) protocol support
- Programmable clock frequency
- 512 bit Read/Write FIFO to lower system overhead
- Slave DMA transfer capability

The MMC/SD card controller transfers data between the CPU and DMA controller on one side and MMC/SD card on the other side. The CPU and DMA controller can read/write the data in the card by accessing the registers in the MMC/SD controller.

The MMC/SD controller on this device, does not support the SPI mode of operation.

6.10.1 MMC/SD Peripheral Register Description(s)

Table 6-16 and Table 6-17 shows the MMC/SD registers. The MMC/SD0 registers start at address 0x3A00 and the MMC/SD1 registers start at address 0x3B00.

Table 6-16. MMC/SD0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
3A00h	MMCCTL	MMC Control Register
3A04h	MMCCLK	MMC Memory Clock Control Register
3A08h	MMCST0	MMC Status Register 0
3A0Ch	MMCST1	MMC Status Register 1
3A10h	MMCIM	MMC Interrupt Mask Register
3A14h	MMCTOR	MMC Response Time-Out Register
3A18h	MMCTOD	MMC Data Read Time-Out Register
3A1Ch	MMCBLEN	MMC Block Length Register
3A20h	MMCNBLK	MMC Number of Blocks Register
3A24h	MMCNBLC	MMC Number of Blocks Counter Register
3A28h	MMCDRR1	MMC Data Receive 1 Register
3A29h	MMCDRR2	MMC Data Receive 2 Register
3A2Ch	MMCDXR1	MMC Data Transmit 1 Register
3A2Dh	MMCDXR2	MMC Data Transmit 2 Register
3A30h	MMCCMD	MMC Command Register
3A34h	MMCARGHL	MMC Argument Register
3A38h	MMCRSP0	MMC Response Register 0
3A39h	MMCRSP1	MMC Response Register 1
3A3Ch	MMCRSP2	MMC Response Register 2
3A3Dh	MMCRSP3	MMC Response Register 3
3A40h	MMCRSP4	MMC Response Register 4
3A41h	MMCRSP5	MMC Response Register 5
3A44h	MMCRSP6	MMC Response Register 6
3A45h	MMCRSP7	MMC Response Register 7
3A48h	MMCDRSP	MMC Data Response Register
3A50h	MMCCIDX	MMC Command Index Register
3A64h – 3A70h	–	Reserved
3A74h	MMCFIFOCTL	MMC FIFO Control Register

Table 6-17. MMC/SD1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
3B00h	MMCCTL	MMC Control Register
3B04h	MMCCLK	MMC Memory Clock Control Register
3B08h	MMCST0	MMC Status Register 0
3B0Ch	MMCST1	MMC Status Register 1
3B10h	MMCIM	MMC Interrupt Mask Register
3B14h	MMCTOR	MMC Response Time-Out Register
3B18h	MMCTOD	MMC Data Read Time-Out Register
3B1Ch	MMCBLEN	MMC Block Length Register
3B20h	MMCNBLK	MMC Number of Blocks Register
3B24h	MMCNBLC	MMC Number of Blocks Counter Register
3B28h	MMCDRR1	MMC Data Receive 1 Register
3B29h	MMCDRR2	MMC Data Receive 2 Register
3B2Ch	MMCDXR1	MMC Data Transmit 1 Register
3B2Dh	MMCDXR2	MMC Data Transmit 2 Register
3B30h	MMCCMD	MMC Command Register
3B34h	MMCARGHL	MMC Argument Register
3B38h	MMCRSP0	MMC Response Register 0
3B39h	MMCRSP1	MMC Response Register 1
3B3Ch	MMCRSP2	MMC Response Register 2
3B3Dh	MMCRSP3	MMC Response Register 3
3B40h	MMCRSP4	MMC Response Register 4
3B41h	MMCRSP5	MMC Response Register 5
3B44h	MMCRSP6	MMC Response Register 6
3B45h	MMCRSP7	MMC Response Register 7
3B48h	MMCDRSP	MMC Data Response Register
3B50h	MMCCIDX	MMC Command Index Register
3B74h	MMCFIFOCTL	MMC FIFO Control Register

6.10.2 MMC/SD Electrical Data/Timing

Table 6-18. Timing Requirements for MMC/SD (see Figure 6-18 and Figure 6-21)

NO.			CV_{DD} = 1.3 V FAST MODE MIN	CV_{DD} = 1.3 V FAST MODE MAX	CV_{DD} = 1.05 V STD MODE MIN	CV_{DD} = 1.05 V STD MODE MAX	UNIT
1	$t_{su(CMDV-CLKH)}$	Setup time, MMCx_CMD data input valid before MMCx_CLK high	3		3		ns
2	$t_{h(CLKH-CMDV)}$	Hold time, MMCx_CMD data input valid after MMCx_CLK high	3		3		ns
3	$t_{su(DATV-CLKH)}$	Setup time, MMC_Dx data input valid before MMCx_CLK high	3		3		ns
4	$t_{h(CLKH-DATV)}$	Hold time, MMC_Dx data input valid after MMCx_CLK high	3		3		ns

Table 6-19. Switching Characteristics Over Recommended Operating Conditions for MMC Output[(1)] (see Figure 6-18 and Figure 6-21)

NO.	PARAMETER		CV_{DD} = 1.3 V FAST MODE MIN	CV_{DD} = 1.3 V FAST MODE MAX	CV_{DD} = 1.05 V STD MODE MIN	CV_{DD} = 1.05 V STD MODE MAX	UNIT
7	$f_{(CLK)}$	Operating frequency, MMCx_CLK	0	50[(2)]	0	25[(2)]	MHz
8	$f_{(CLK\_ID)}$	Identfication mode frequency, MMCx_CLK	0	400	0	400	kHz
9	$t_{w(CLKL)}$	Pulse width, MMCx_CLK low	7		10		ns
10	$t_{w(CLKH)}$	Pulse width, MMCx_CLK high	7		10		ns
11	$t_{r(CLK)}$	Rise time, MMCx_CLK		3		10	ns
12	$t_{f(CLK)}$	Fall time, MMCx_CLK		3		10	ns
13	$t_{d(MDCLKL-CMDIV)}$	Delay time, MMCx_CLK low to MMC_CMD data output invalid	-4		-4		ns
14	$t_{d(MDCLKL-CMDV)}$	Delay time, MMCx_CLK low to MMC_CMD data output valid		4		5	ns
15	$t_{d(MDCLKL-DATIV)}$	Delay time, MMCx_CLK low to MMC_Dx data output invalid	-4		-4		ns
16	$t_{d(MDCLKL-DATV)}$	Delay time, MMCx_CLK low to MMC_Dx data output valid		4		5	ns

(1) For MMC/SD, the parametric values are measured at DV_{DDIO} = 3.3 V or 2.75 V.
(2) Use this value or SYS_CLK/2 whichever is smaller.

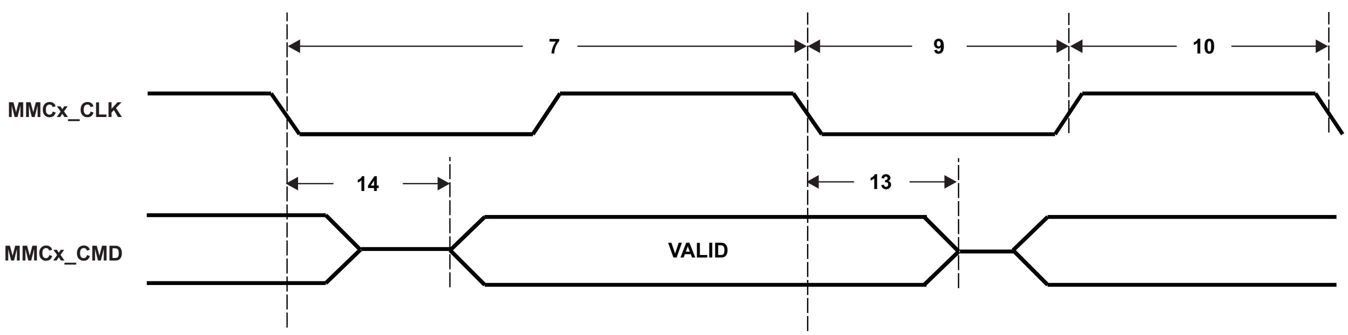


Figure 6-18. MMC/SD Host Command Write Timing

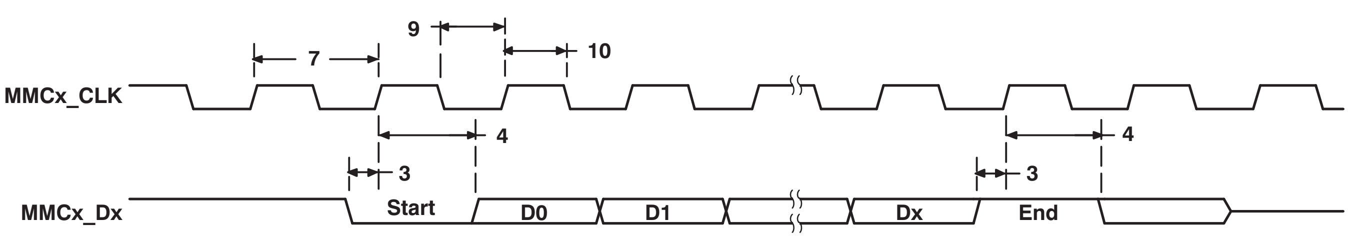


Figure 6-19. MMC/SD Card Response Timing

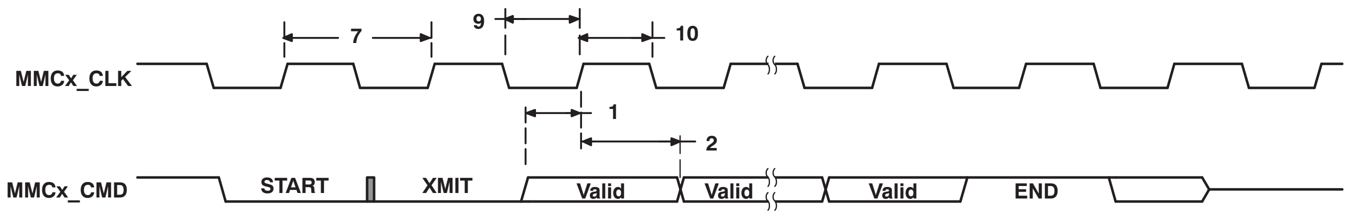


Figure 6-20. MMC/SD Host Write Timing

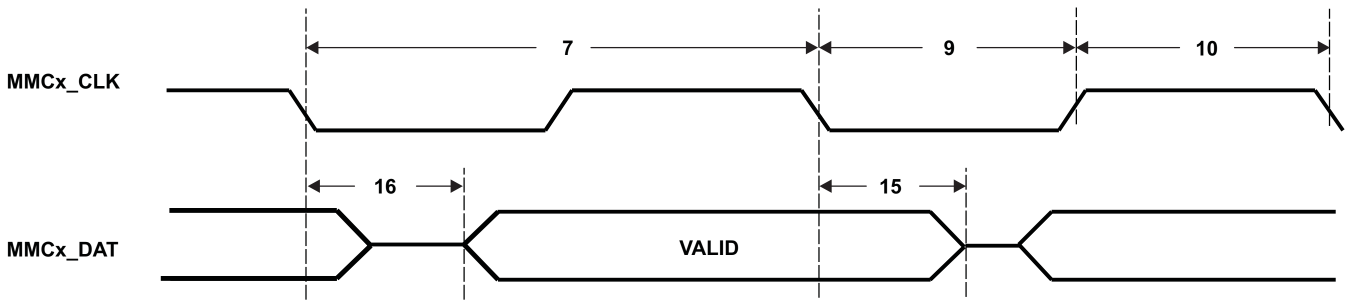


Figure 6-21. MMC/SD Data Write Timing

6.11 Real-Time Clock (RTC)

The VC5505 includes a Real-Time Clock (RTC) with its own separated power supply and isolation circuits. The separate supply and isolation circuits allow the RTC to run while the rest of the VC5505 device (Core and I/O) is powered off. All RTC registers are preserved (except for RTC Control and RTC Update Registers) and the counter continues to operate when the device is powered off. The RTC also has the capability to wakeup the device from idle states via alarms, periodic interrupts, or an external WAKEUP input. Additionally, the RTC is able to output an alarm or periodic interrupt on the WAKEUP pin to cause external power management to re-enable power to the DSP Core and I/O.

The VC5505 RTC provides the following features:

- 100-year calendar up to year 2099.
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Millisecond time correction
- Binary-coded-decimal (BCD) representation of time, calendar, and alarm
- 24-hour clock mode
- Second, minute, hour, day, or week alarm interrupt
- Periodic interrupt: every millisecond, second, minute, hour, or day
- Alarm interrupt: precise time of day
- Single interrupt to the DSP CPU
- 32.768-kHz crystal oscillator with frequency calibration

Control of the RTC is maintained through a set of I/O memory mapped registers (see Table 6-20). Note that any write to these registers will be synchronized to the RTC 32.768-KHz clock; thus, the CPU must run at least 3X faster than the RTC. Writes to these registers will not be evident until the next two 32.768-KHz clock cycles later. Furthermore, if the RTC Oscillator is disabled, no RTC register can be written to.

The RTC has its own power-on-reset (POR) circuit which resets the registers in the RTC core domain when power is first applied to the CV_{DD_RTC} power pin. The RTC flops are not reset by the device's $\overline{RESET}$ pin nor the digital core's POR (powergood signal) which monitors the DSP_LDOO voltage.

The scratch registers in the RTC can be used to take advantage of this unique reset domain to keep track of when the DSP boots and whether the RTC time registers have already been initialized to the current clock time or whether the software needs to go into a routine to prompt the user to set the time/date.

6.11.1 RTC Peripheral Register Description(s)

Table 6-20 shows the RTC registers.

Table 6-20. Real-Time Clock (RTC) Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
1900h	RTCINTEN	RTC Interrupt Enable Register
1901h	RTCUPDATE	RTC Update Register
1904h	RTCMIL	Milliseconds Register
1905h	RTCMILA	Milliseconds Alarm Register
1908h	RTCSEC	Seconds Register
1909h	RTCSECA	Seconds Alarm Register
190Ch	RTCMIN	Minutes Register
190Dh	RTCMINA	Minutes Alarm Register
1910h	RTCHOUR	Hours Register
1911h	RTCHOURA	Hours Alarm Register
1914h	RTCDAY	Days Register
1915h	RTCDAYA	Days Alarm Register
1918h	RTCMONTH	Months Register
1919h	RTCMONTHA	Months Alarm Register
191Ch	RTCYEAR	Years Register
191Dh	RTCYEARA	Years Alarm Register
1920h	RTCINTFL	RTC Interrupt Flag Register
1921h	RTCNOPWR	RTC Lost Power Status Register
1924h	RTCINTREG	RTC Interrupt Register
1928h	RTCDRIFT	RTC Compensation Register
192Ch	RTCOSC	RTC Oscillator Register
1930h	RTCPMGT	RTC Power Management Register
1960h	RTCSCR1	RTC LSW Scratch Register 1
1961h	RTCSCR2	RTC MSW Scratch Register 2
1964h	RTCSCR3	RTC LSW Scratch Register 3
1965h	RTCSCR4	RTC MSW Scratch Register 4

6.11.1.1 RTC Electrical Data/Timing

For more detailed information on RTC electrical timings, specifically WAKEUP, see the Section 6.7.3, *Reset Electrical Data/Timing*.

6.12 Inter-Integrated Circuit (I2C)

The inter-integrated circuit (I2C) module provides an interface between VC5505 and other devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive 2 to 8-bit data to/from the DSP through the I2C module. The I2C port *does not* support CBUS compatible devices.

The I2C port supports the following features:

- Compatible with Philips I2C Specification Revision 2.1 (January 2000)
- Data Transfer Rate from 10 kbps to 400 kbps (Philips Fast-Mode Rate)
- Noise Filter to Remove Noise 50 ns or Less
- Seven- and Ten-Bit Device Addressing Modes
- Master (Transmit/Receive) and Slave (Transmit/Receive) Functionality
- One Read DMA Event and One Write DMA Event, which can be used by the DMA Controller
- One Interrupt that can be used by the CPU
- Slew-Rate Limited Open-Drain Output Buffers

The I2C module clock must be in the range from 6.7 MHz to 13.3 MHz. This is necessary for proper operation of the I2C module. With the I2C module clock in this range, the noise filters on the SDA and SCL pins suppress noise that has a duration of 50 ns or shorter. The I2C module clock is derived from the DSP clock divided by a programmable prescaler.

6.12.1 I2C Peripheral Register Description(s)

Table 6-21 shows the Inter-Integrated Circuit (I2C) registers.

Table 6-21. Inter-Integrated Circuit (I2C) Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
1A00h	ICOAR	I2C Own Address Register
1A04h	ICIMR	I2C Interrupt Mask Register
1A08h	ICSTR	I2C Interrupt Status Register
1A0Ch	ICCLKL	I2C Clock Low-Time Divider Register
1A10h	ICCLKH	I2C Clock High-Time Divider Register
1A14h	ICCNT	I2C Data Count Register
1A18h	ICDRR	I2C Data Receive Register
1A1Ch	ICSAR	I2C Slave Address Register
1A20h	ICDXR	I2C Data Transmit Register
1A24h	ICMDR	I2C Mode Register
1A28h	ICIVR	I2C Interrupt Vector Register
1A2Ch	ICEMDR	I2C Extended Mode Register
1A30h	ICPSC	I2C Prescaler Register
1A34h	ICPID1	I2C Peripheral Identification Register 1
1A38h	ICPID2	I2C Peripheral Identification Register 2

6.12.2 I2C Electrical Data/Timing

Table 6-22. Timing Requirements for I2C Timings[1] (see Figure 6-22)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V STANDARD MODE MIN	STANDARD MODE MAX	FAST MODE MIN	FAST MODE MAX	UNIT
1	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
3	$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100[2]		ns
7	$t_{h(SDA-SCLL)}$	Hold time, SDA valid after SCL low	0[3]		0[3]	0.9[4]	µs
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
9	$t_{r(SDA)}$	Rise time, SDA[5]		1000	$20 + 0.1C_b$ [6]	300	ns
10	$t_{r(SCL)}$	Rise time, SCL[5]		1000	$20 + 0.1C_b$ [6]	300	ns
11	$t_{f(SDA)}$	Fall time, SDA[5]		300	$20 + 0.1C_b$ [6]	300	ns
12	$t_{f(SCL)}$	Fall time, SCL[5]		300	$20 + 0.1C_b$ [6]	300	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
15	C_b [6]	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down. Also these pins are not 3.6 V-tolerant (their V_{IH} cannot go above DV_{DDIO} + 0.3 V).
(2) A Fast-mode I^2C-bus™ device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-Bus Specification) before the SCL line is released.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
(5) The rise/fall times are measured at 30% and 70% of DV_{DDIO}. The fall time is only slightly influenced by the external bus load (C_b) and external pullup resistor. However, the rise time (t_r) is mainly determined by the bus load capacitance and the value of the pullup resistor. The pullup resistor must be selected to meet the I2C rise and fall time values specified.
(6) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

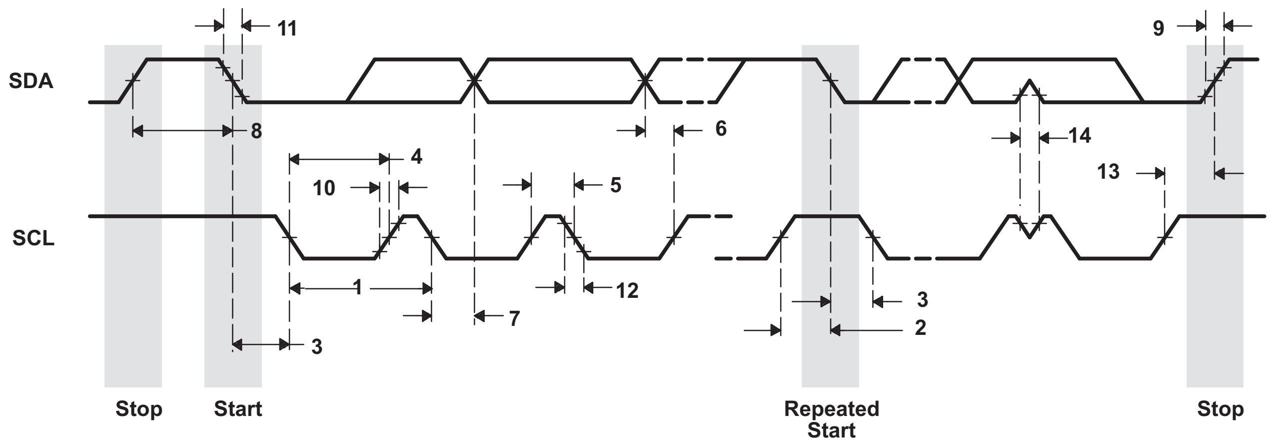


Figure 6-22. I2C Receive Timings

Table 6-23. Switching Characteristics for I2C Timings[(1)] (see Figure 6-23)

NO.	PARAMETER		CV_{DD} = 1.05 V, CV_{DD} = 1.3 V				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
16	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
17	$t_{d(SCLH-SDAL)}$	Delay time, SCL high to SDA low (for a repeated START condition)	4.7		0.6		µs
18	$t_{d(SDAL-SCLL)}$	Delay time, SDA low to SCL low (for a START and a repeated START condition)	4		0.6		µs
19	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
20	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
21	$t_{d(SDAV-SCLH)}$	Delay time, SDA valid to SCL high	250		100		ns
22	$t_{v(SCLL-SDAV)}$	Valid time, SDA valid after SCL low	0		0	0.9	µs
23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
24	$t_{r(SDA)}$	Rise time, SDA[(2)]		1000	$20 + 0.1C_b$ [(1)]	300	ns
25	$t_{r(SCL)}$	Rise time, SCL[(2)]		1000	$20 + 0.1C_b$ [(1)]	300	ns
26	$t_{f(SDA)}$	Fall time, SDA[(2)]		300	$20 + 0.1C_b$ [(1)]	300	ns
27	$t_{f(SCL)}$	Fall time, SCL[(2)]		300	$20 + 0.1C_b$ [(1)]	300	ns
28	$t_{d(SCLH-SDAH)}$	Delay time, SCL high to SDA high (for STOP condition)	4		0.6		µs
29	C_p	Capacitance for each I2C pin		10		10	pF

(1) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.
(2) The rise/fall times are measured at 30% and 70% of DV_{DDIO}. The fall time is only slightly influenced by the external bus load (C_b) and external pullup resistor. However, the rise time (t_r) is mainly determined by the bus load capacitance and the value of the pullup resistor. The pullup resistor must be selected to meet the I2C rise and fall time values specified.

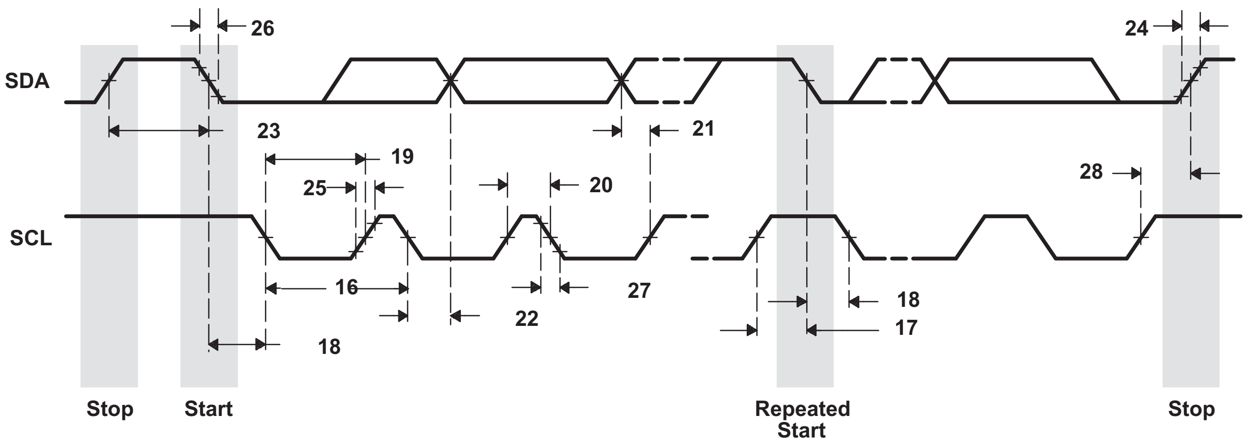


Figure 6-23. I2C Transmit Timings

6.13 Universal Asynchronous Receiver/Transmitter (UART)

The UART performs serial-to-parallel conversions on data received from an external peripheral device and parallel-to-serial conversions on data transmitted to an external peripheral device via a serial bus.

The VC5505 has one UART peripheral with the following features:

- Programmable baud rates (frequency pre-scale values from 1 to 65535)
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no PARITY bit generation and detection
  - 1, 1.5, or 2 STOP bit generation
- 16-byte depth transmitter and receiver FIFOs:
  - The UART can be operated with or without the FIFOs
  - 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
- DMA signaling capability for both received and transmitted data
- CPU interrupt capability for both received and transmitted data
- False START bit detection
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, and framing error simulation
- Programmable autoflow control using CTS and RTS signals

6.13.1 UART Peripheral Register Description(s)

Table 6-24 shows the UART registers.

Table 6-24. UART Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
1B00h	RBR	Receiver Buffer Register (read only)
1B00h	THR	Transmitter Holding Register (write only)
1B02h	IER	Interrupt Enable Register
1B04h	IIR	Interrupt Identification Register (read only)
1B04h	FCR	FIFO Control Register (write only)
1B06h	LCR	Line Control Register
1B08h	MCR	Modem Control Register
1B0Ah	LSR	Line Status Register
1B0Ch	MSR	Modem Status Register
1B0Eh	SCR	Scratch Register
1B10h	DLL	Divisor LSB Latch
1B12h	DLH	Divisor MSB Latch
1B18h	PWREMU_MGMT	Power and Emulation Management Register

6.13.2 UART Electrical Data/Timing [Receive/Transmit]

Table 6-25. Timing Requirements for UART Receive[(1)] (see Figure 6-24)

NO.			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
4	$t_{w(URXDB)}$	Pulse duration, receive data bit (UART_RXD) [15/30/100 pF]	U - 3	U + 3	U - 3	U + 3	ns
5	$t_{w(URXSB)}$	Pulse duration, receive start bit [15/30/100 pF]	U - 3	U + 3	U - 3	U + 3	ns

(1) U = UART baud time = 1/programmed baud rate.

Table 6-26. Switching Characteristics Over Recommended Operating Conditions for UART Transmit[(1)] (see Figure 6-24)

NO.	PARAMETER		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
1	$f_{(baud)}$	Maximum programmable bit rate		3.75		6.25	MHz
2	$t_{w(UTXDB)}$	Pulse duration, transmit data bit (UART_TXD) [15/30/100 pF]	U - 3	U + 3	U - 3	U + 3	ns
3	$t_{w(UTXSB)}$	Pulse duration, transmit start bit [15/30/100 pF]	U - 3	U + 3	U - 3	U + 3	ns

(1) U = UART baud time = 1/programmed baud rate.

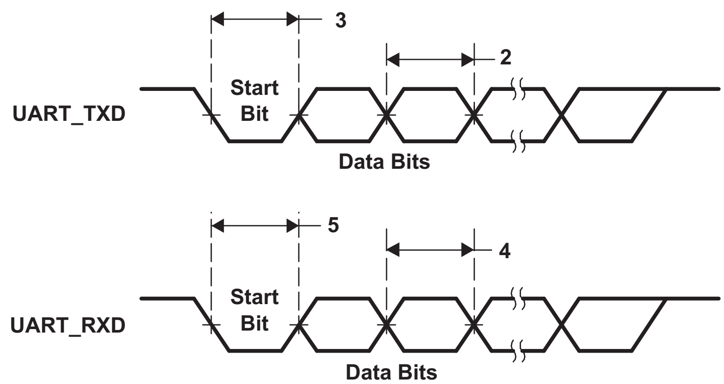


Figure 6-24. UART Transmit/Receive Timing

6.14 Inter-IC Sound (I2S)

The VC5505 I2S peripherals allow serial transfer of full-duplex streaming data, usually audio data, between the device and an external I2S peripheral device such as an audio codec.

The VC5505 supports 4 independent dual-channel I2S peripherals, each with the following features:

- Full-duplex (transmit and receive) dual-channel communication
- Double buffered data registers that allow for continuous data streaming
- I2S/Left-justified and DSP data format with a data delay of 1 or 2 bits
- Data word-lengths of 8, 10, 12, 14, 16, 18, 20, 24, or 32 bits
- Ability to sign-extend received data samples for easy use in signal processing algorithms
- Programmable polarity for both frame synchronization and bit clocks
- Stereo (in I2S/Left-justified or DSP data formats) or mono (in DSP data format) mode
- Detection of over-run, under-run, and frame-sync error conditions

6.14.1 I2S Peripheral Register Description(s)

Table 6-27 through Table 6-30 show the I2S0 through I2S3 registers.

Table 6-27. I2S0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
2800h	I2S0SCTRL	I2S0 Serializer Control Register
2804h	I2S0SRATE	I2S0 Sample Rate Generator Register
2808h	I2S0TXLT0	I2S0 Transmit Left Data 0 Register
2809h	I2S0TXLT1	I2S0 Transmit Left Data 1 Register
280Ch	I2S0TXRT0	I2S0 Transmit Right Data 0 Register
280Dh	I2S0TXRT1	I2S0 Transmit Right Data 1 Register
2810h	I2S0INTFL	I2S0 Interrupt Flag Register
2814h	I2S0INTMASK	I2S0 Interrupt Mask Register
2828h	I2S0RXLT0	I2S0 Receive Left Data 0 Register
2829h	I2S0RXLT1	I2S0 Receive Left Data 1 Register
282Ch	I2S0RXRT0	I2S0 Receive Right Data 0 Register
282Dh	I2S0RXRT1	I2S0 Receive Right Data 1 Register

Table 6-28. I2S1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
2900h	I2S1SCTRL	I2S1 Serializer Control Register
2904h	I2S1SRATE	I2S1 Sample Rate Generator Register
2908h	I2S1TXLT0	I2S1 Transmit Left Data 0 Register
2909h	I2S1TXLT1	I2S1 Transmit Left Data 1 Register
290Ch	I2S1TXRT0	I2S1 Transmit Right Data 0 Register
290Dh	I2S1TXRT1	I2S1 Transmit Right Data 1 Register
2910h	I2S1INTFL	I2S1 Interrupt Flag Register
2914h	I2S1INTMASK	I2S1 Interrupt Mask Register
2928h	I2S1RXLT0	I2S1 Receive Left Data 0 Register
2929h	I2S1RXLT1	I2S1 Receive Left Data 1 Register
292Ch	I2S1RXRT0	I2S1 Receive Right Data 0 Register
292Dh	I2S1RXRT1	I2S1 Receive Right Data 1 Register

Table 6-29. I2S2 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
2A00h	I2S2SCTRL	I2S2 Serializer Control Register
2A04h	I2S2SRATE	I2S2 Sample Rate Generator Register
2A08h	I2S2TXLT0	I2S2 Transmit Left Data 0 Register
2A09h	I2S2TXLT1	I2S2 Transmit Left Data 1 Register
2A0Ch	I2S2TXRT0	I2S2 Transmit Right Data 0 Register
2A0Dh	I2S2TXRT1	I2S2 Transmit Right Data 1 Register
2A10h	I2S2INTFL	I2S2 Interrupt Flag Register
2A14h	I2S2INTMASK	I2S2 Interrupt Mask Register
2A28h	I2S2RXLT0	I2S2 Receive Left Data 0 Register
2A29h	I2S2RXLT1	I2S2 Receive Left Data 1 Register
2A2Ch	I2S2RXRT0	I2S2 Receive Right Data 0 Register
2A2Dh	I2S2RXRT1	I2S2 Receive Right Data 1 Register

Table 6-30. I2S3 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
2B00h	I2S3SCTRL	I2S3 Serializer Control Register
2B04h	I2S3SRATE	I2S3 Sample Rate Generator Register
2B08h	I2S3TXLT0	I2S3 Transmit Left Data 0 Register
2B09h	I2S3TXLT1	I2S3 Transmit Left Data 1 Register
2B0Ch	I2S3TXRT0	I2S3 Transmit Right Data 0 Register
2B0Dh	I2S3TXRT1	I2S3 Transmit Right Data 1 Register
2B10h	I2S3INTFL	I2S3 Interrupt Flag Register
2B14h	I2S3INTMASK	I2S3 Interrupt Mask Register
2B28h	I2S3RXLT0	I2S3 Receive Left Data 0 Register
2B29h	I2S3RXLT1	I2S3 Receive Left Data 1 Register
2B2Ch	I2S3RXRT0	I2S3 Receive Right Data 0 Register
2B2Dh	I2S3RXRT1	I2S3 Receive Right Data 1 Register

6.14.2 I2S Electrical Data/Timing

Table 6-31. Timing Requirements for I2S [I/O = 3.3 V, 2.8 V, and 2.5 V][1] (see Figure 6-25)

NO.			MASTER				SLAVE				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, I2S_CLK	40 or 2P[1] [2]		40 or 2P[1] [2]		40 or 2P[1] [2]		40 or 2P[1] [2]		ns
2	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high	20		20		20		20		ns
3	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low	20		20		20		20		ns
7	$t_{su(RXV-CLKH)}$	Setup time, I2S_RX valid before I2S CLK high (CLKPOL = 0)	5		5		5		5		ns
	$t_{su(RXV-CLKL)}$	Setup time, I2S_RX valid before I2S_CLK low (CLKPOL = 1)	5		5		5		5		ns
8	$t_{h(CLKH-RXV)}$	Hold time, I2S_RX valid after I2S_CLK high (CLKPOL = 0)	7		7		2		2		ns
	$t_{h(CLKL-RXV)}$	Hold time, I2S_RX valid after I2S_CLK low (CLKPOL = 1)	7		7		2		2		ns
9	$t_{su(FSV-CLKH)}$	Setup time, I2S_FS valid before I2S_CLK high (CLKPOL = 0)	–		–		15		15		ns
	$t_{su(FSV-CLKL)}$	Setup time, I2S_FS valid before I2S_CLK low (CLKPOL = 1)	–		–		15		15		ns
10	$t_{h(CLKH-FSV)}$	Hold time, I2S_FS valid after I2S_CLK high (CLKPOL = 0)	–		–		$t_{w(CLKH)}$ + 0.6[3]		$t_{w(CLKH)}$ + 0.6[3]		ns
	$t_{h(CLKL-FSV)}$	Hold time, I2S_FS valid after I2S_CLK low (CLKPOL = 1)	–		–		$t_{w(CLKL)}$ + 0.6[3]		$t_{w(CLKL)}$ + 0.6[3]		ns

(1) P = SYSCLK period in ns. For example, when running parts at 100 MHz, use P = 10 ns.
(2) Use whichever value is greater.
(3) In Slave Mode, I2S_FS is required to be latched on both edges of I2S input clock (I2S_CLK).

Table 6-32. Timing Requirements for I2S [I/O = 1.8 V][(1)] (see Figure 6-25)

NO.			MASTER				SLAVE				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, I2S_CLK	50 or 2P[(1) (2)]		40 or 2P[(1) (2)]		50 or 2P[(1) (2)]		40 or 2P[(1) (2)]		ns
2	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high	25		20		25		20		ns
3	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low	25		20		25		20		ns
7	$t_{su(RXV-CLKH)}$	Setup time, I2S_RX valid before I2S CLK high (CLKPOL = 0)	5		5		5		5		ns
	$t_{su(RXV-CLKL)}$	Setup time, I2S_RX valid before I2S_CLK low (CLKPOL = 1)	5		5		5		5		ns
8	$t_{h(CLKH-RXV)}$	Hold time, I2S_RX valid after I2S_CLK high (CLKPOL = 0)	7		7		2		2		ns
	$t_{h(CLKL-RXV)}$	Hold time, I2S_RX valid after I2S_CLK low (CLKPOL = 1)	7		7		2		2		ns
9	$t_{su(FSV-CLKH)}$	Setup time, I2S_FS valid before I2S_CLK high (CLKPOL = 0)	–		–		15		15		ns
	$t_{su(FSV-CLKL)}$	Setup time, I2S_FS valid before I2S_CLK low (CLKPOL = 1)	–		–		15		15		ns
10	$t_{h(CLKH-FSV)}$	Hold time, I2S_FS valid after I2S_CLK high (CLKPOL = 0)	–		–		$t_{w(CLKH)}$ + 0.6[(3)]		$t_{w(CLKH)}$ + 0.6[(3)]		ns
	$t_{h(CLKL-FSV)}$	Hold time, I2S_FS valid after I2S_CLK low (CLKPOL = 1)	–		–		$t_{w(CLKL)}$ + 0.6[(3)]		$t_{w(CLKL)}$ + 0.6[(3)]		ns

(1) P = SYSCLK period in ns. For example, when running parts at 100 MHz, use P = 10 ns.
(2) Use whichever value is greater.
(3) In Slave Mode, I2S_FS is required to be latched on both edges of I2S input clock (I2S_CLK).

Table 6-33. Switching Characteristics Over Recommended Operating Conditions for I2S Output [I/O = 3.3 V, 2.8 V, or 2.5 V] (see Figure 6-25)

NO.	PARAMETER		MASTER				SLAVE				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, I2S_CLK	40 or 2P (1) (2)		40 or 2P (1) (2)		40 or 2P (1) (2)		40 or 2P (1) (2)		ns
2	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high (CLKPOL = 0)	20		20		20		20		ns
	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low (CLKPOL = 1)	20		20		20		20		ns
3	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low (CLKPOL = 0)	20		20		20		20		ns
	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high (CLKPOL = 1)	20		20		20		20		ns
4	$t_{dmax(CLKL-DXV)}$	Output Delay time, I2S_CLK low to I2S_DX valid (CLKPOL = 0)		15		14		12		12	ns
	$t_{dmax(CLKH-DXV)}$	Output Delay time, I2S_CLK high to I2S_DX valid (CLKPOL = 1)		15		14		12		12	ns
5	$t_{oh(DXV-CLKH)}$	Output Hold time, I2S_CLK high to I2S_DX invalid (CLKPOL = 0)	0		0		0		0		ns
	$t_{oh(DXV-CLKL)}$	Output Hold time, I2S_CLK low to I2S_DX invalid (CLKPOL = 1)	0		0		0		0		ns
6	$t_{dmax(CLKL-FSV)}$	Delay time, I2S_CLK low to I2S_FS valid (CLKPOL = 0)		14		14		–		–	ns
	$t_{dmax(CLKH-FSV)}$	Delay time, I2S_CLK high to I2S_FS valid (CLKPOL = 1)		14		14		–		–	ns

(1) P = SYSCLK period in ns. For example, when running parts at 100 MHz, use P = 10 ns.
(2) Use whichever value is greater.

Table 6-34. Switching Characteristics Over Recommended Operating Conditions for I2S Output [I/O = 1.8 V] (see Figure 6-25)

NO.	PARAMETER		MASTER				SLAVE				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, I2S_CLK	50 or 2P(1) (2)		40 or 2P(1) (2)		50 or 2P(1) (2)		40 or 2P(1) (2)		ns
2	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high (CLKPOL = 0)	25		20		25		20		ns
	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low (CLKPOL = 1)	25		20		25		20		ns
3	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low (CLKPOL = 0)	25		20		25		20		ns
	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high (CLKPOL = 1)	25		20		25		20		ns
4	$t_{dmax(CLKL-DXV)}$	Output Delay time, I2S_CLK low to I2S_DX valid (CLKPOL = 0)		19		14		15		12	ns
	$t_{dmax(CLKH-DXV)}$	Output Delay time, I2S_CLK high to I2S_DX valid (CLKPOL = 1)		19		14		15		12	ns
5	$t_{oh(DXV-CLKH)}$	Output Hold time, I2S_CLK high to I2S_DX invalid (CLKPOL = 0)	0		0		0		0		ns
	$t_{oh(DXV-CLKL)}$	Output Hold time, I2S_CLK low to I2S_DX invalid (CLKPOL = 1)	0		0		0		0		ns
6	$t_{dmax(CLKL-FSV)}$	Delay time, I2S_CLK low to I2S_FS valid (CLKPOL = 0)		14		14		–		–	ns
	$t_{dmax(CLKH-FSV)}$	Delay time, I2S_CLK high to I2S_FS valid (CLKPOL = 1)		14		14		–		–	ns

(1) P = SYSCLK period in ns. For example, when running parts at 100 MHz, use P = 10 ns.
(2) Use whichever value is greater.

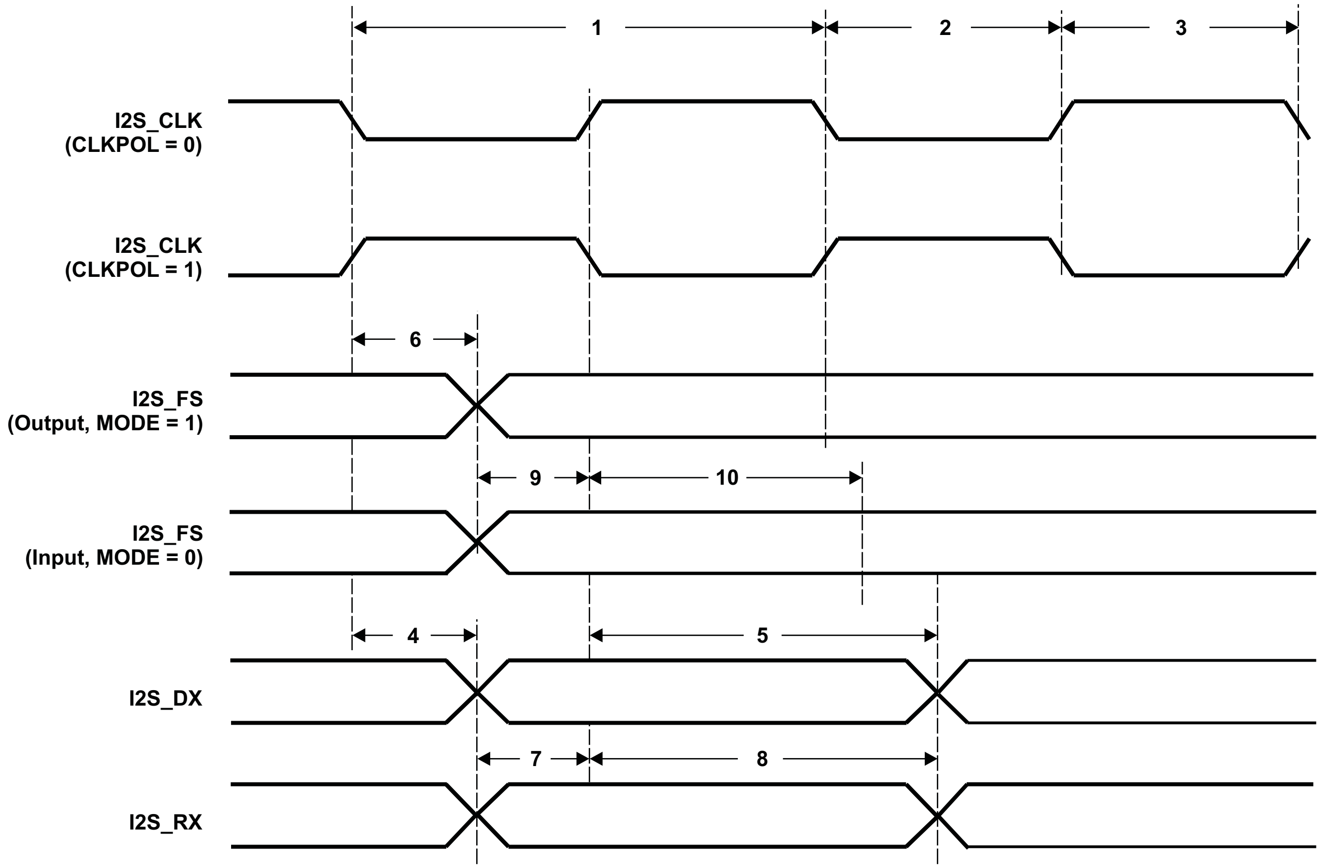


Figure 6-25. I2S Input and Output Timings

6.15 Liquid Crystal Display Controller (LCDC)

The VC5505 includes a LCD Interface Display Driver (LIDD) controller.

The LIDD Controller supports the asynchronous LCD interface and has the following features:

- Provides full-timing programmability of control signals and output data

Note: Raster mode is ***not*** supported on this device.

The LCD controller is responsible for generating the correct external timing. The DMA engine provides a constant flow of data from the frame buffer(s) to the external LCD panel via the LIDD controller. In addition, CPU access is provided to read and write registers.

6.15.1 LCDC Peripheral Register Description(s)

Table 6-35 shows the LCDC peripheral registers.

Table 6-35. LCD Controller Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
2E00h	LCDREVMIN	LCD Minor Revision Register
2E01h	LCDREVMAJ	LCD Major Revision Register
2E04h	LCDCR	LCD Control Register
2E08h	LCDSR	LCD Status Register
2E0Ch	LCDLIDDCR	LCD LIDD Control Register
2E10h	LCDLIDDCS0CONFIG0	LCD LIDD CS0 Configuration Register 0
2E11h	LCDLIDDCS0CONFIG1	LCD LIDD CS0 Configuration Register 1
2E14h	LCDLIDDCS0ADDR	LCD LIDD CS0 Address Read/Write Register
2E18h	LCDLIDDCS0DATA	LCD LIDD CS0 Data Read/Write Register
2E1Ch	LCDLIDDCS1CONFIG0	LCD LIDD CS1 Configuration Register 0
2E1Dh	LCDLIDDCS1CONFIG1	LCD LIDD CS1 Configuration Register 1
2E20h	LCDLIDDCS1ADDR	LCD LIDD CS1 Address Read/Write Register
2E24h	LCDLIDDCS1DATA	LCD LIDD CS1 Data Read/Write Register
2E28h – 2E3Ah	—	Reserved
2E40h	LCDDMACR	LCD DMA Control Register
2E44h	LCDDMAFB0BAR0	LCD DMA Frame Buffer 0 Base Address Register 0
2E45h	LCDDMAFB0BAR1	LCD DMA Frame Buffer 0 Base Address Register 1
2E48h	LCDDMAFB0CAR0	LCD DMA Frame Buffer 0 Ceiling Address Register 0
2E49h	LCDDMAFB0CAR1	LCD DMA Frame Buffer 0 Ceiling Address Register 1
2E4Ch	LCDDMAFB1BAR0	LCD DMA Frame Buffer 1 Base Address Register 0
2E4Dh	LCDDMAFB1BAR1	LCD DMA Frame Buffer 1 Base Address Register 1
2E50h	LCDDMAFB1CAR0	LCD DMA Frame Buffer 1 Ceiling Address Register 0
2E51h	LCDDMAFB1CAR1	LCD DMA Frame Buffer 1 Ceiling Address Register 1

6.15.2 LCDC Electrical Data/Timing

Table 6-36. Timing Requirements for LCD LIDD Mode(1) (see Figure 6-26 through Figure 6-33)

NO.			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
16	$t_{su(LCD\_D-CLK)}$	Setup time, LCD_D[15:0] valid before LCD_CLK rising edge	25		40		ns
17	$t_{h(CLK-LCD\_D)}$	Hold time, LCD_D[15:0] valid after LCD_CLK rising edge	0		0		ns

(1) Over operating free-air temperature range (unless otherwise noted)

Table 6-37. Switching Characteristics Over Recommended Operating Conditions for LCD LIDD Mode (see Figure 6-26 through Figure 6-33)

NO.	PARAMETER		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
4	$t_{d(LCD\_D\_V)}$	Delay time, LCD_CLK rising edge to LCD_D[15:0] valid (write)		10		15	ns
5	$t_{d(LCD\_D\_I)}$	Delay time, LCD_CLK rising edge to LCD_D[15:0] invalid (write)	-6		-6		ns
6	$t_{d(LCD\_E\_A)}$	Delay time, LCD_CLK rising edge to LCD_CSx_Ex low		10		15	ns
7	$t_{d(LCD\_E\_I)}$	Delay time, LCD_CLKrising edge to LCD_CSx_Ex high	-6		-6		ns
8	$t_{d(LCD\_A\_A)}$	Delay time, LCD_CLKrising edge to LCD_RS low		10		15	ns
9	$t_{d(LCD\_A\_I)}$	Delay time, LCD_CLK rising edge to LCD_RS high	-6		-6		ns
10	$t_{d(LCD\_W\_A)}$	Delay time, LCD_CLK rising edge to LCD_RW_WRB low		10		15	ns
11	$t_{d(LCD\_W\_I)}$	Delay time, LCD_CLK rising edge to LCD_RW_WRB high	-6		-6		ns
12	$t_{d(LCD\_STRB\_A)}$	Delay time, LCD_CLK rising edge to LCD_EN_RDB high		10		15	ns
13	$t_{d(LCD\_STRB\_I)}$	Delay time, LCD_CLK rising edge to LCD_EN_RDB low	-6		-6		ns
14	$t_{d(LCD\_D\_Z)}$	Delay time, LCD_CLK rising edge to LCD_D[15:0] in 3-state		10		15	ns
15	$t_{d(Z\_LCD\_D)}$	Delay time, LCD_CLK rising edge to LCD_D[15:0] valid from 3-state	-6		-6		ns

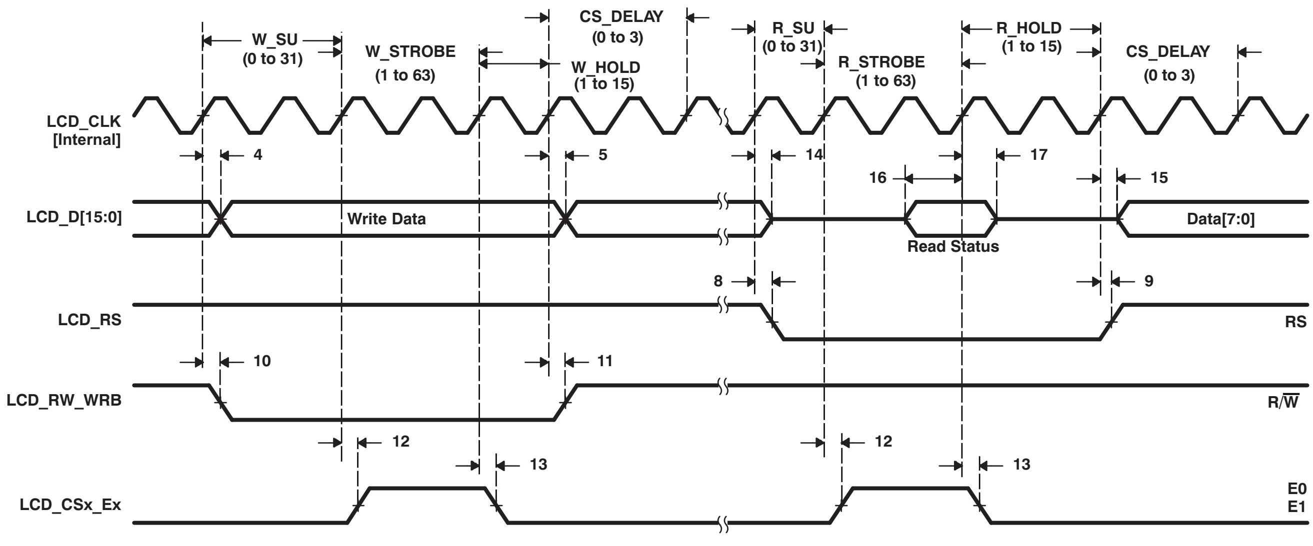


Figure 6-26. Character Display HD44780 Write

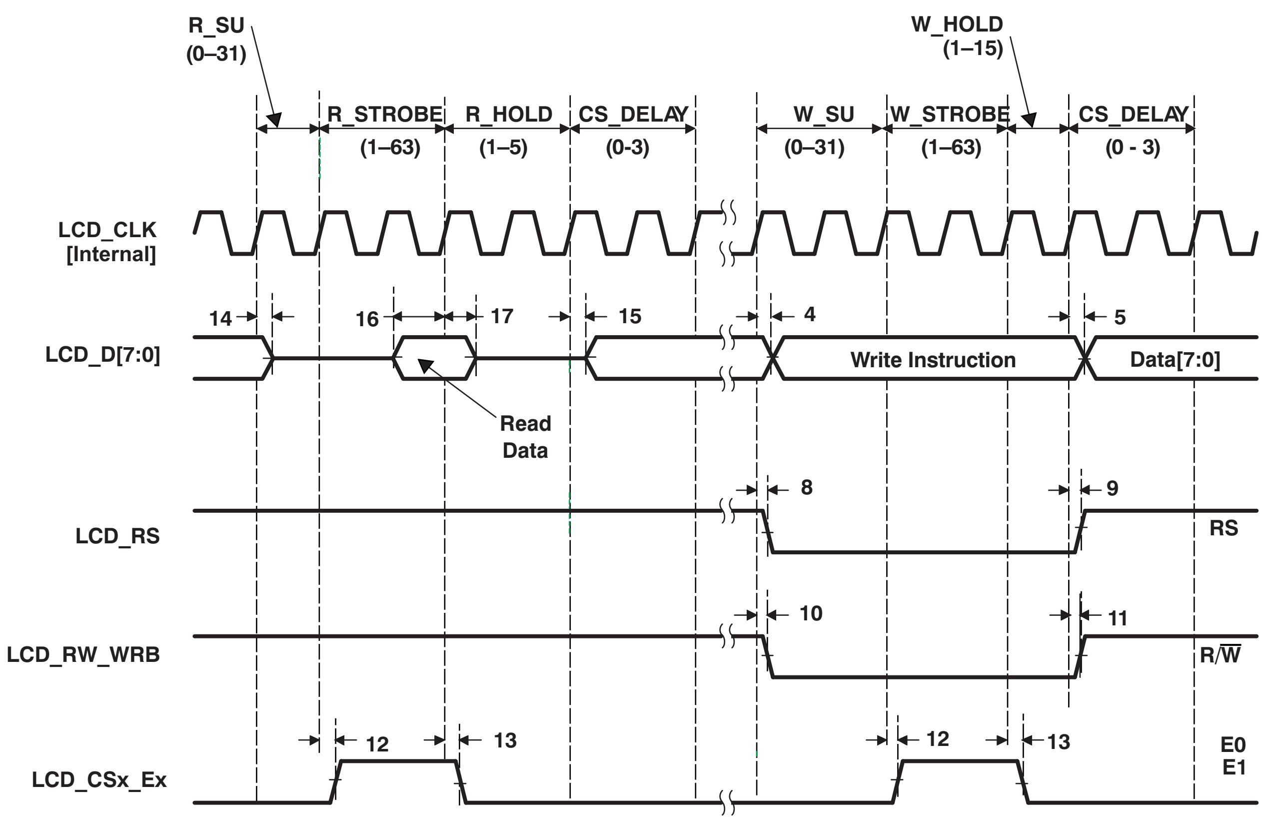


Figure 6-27. Character Display HD44780 Read

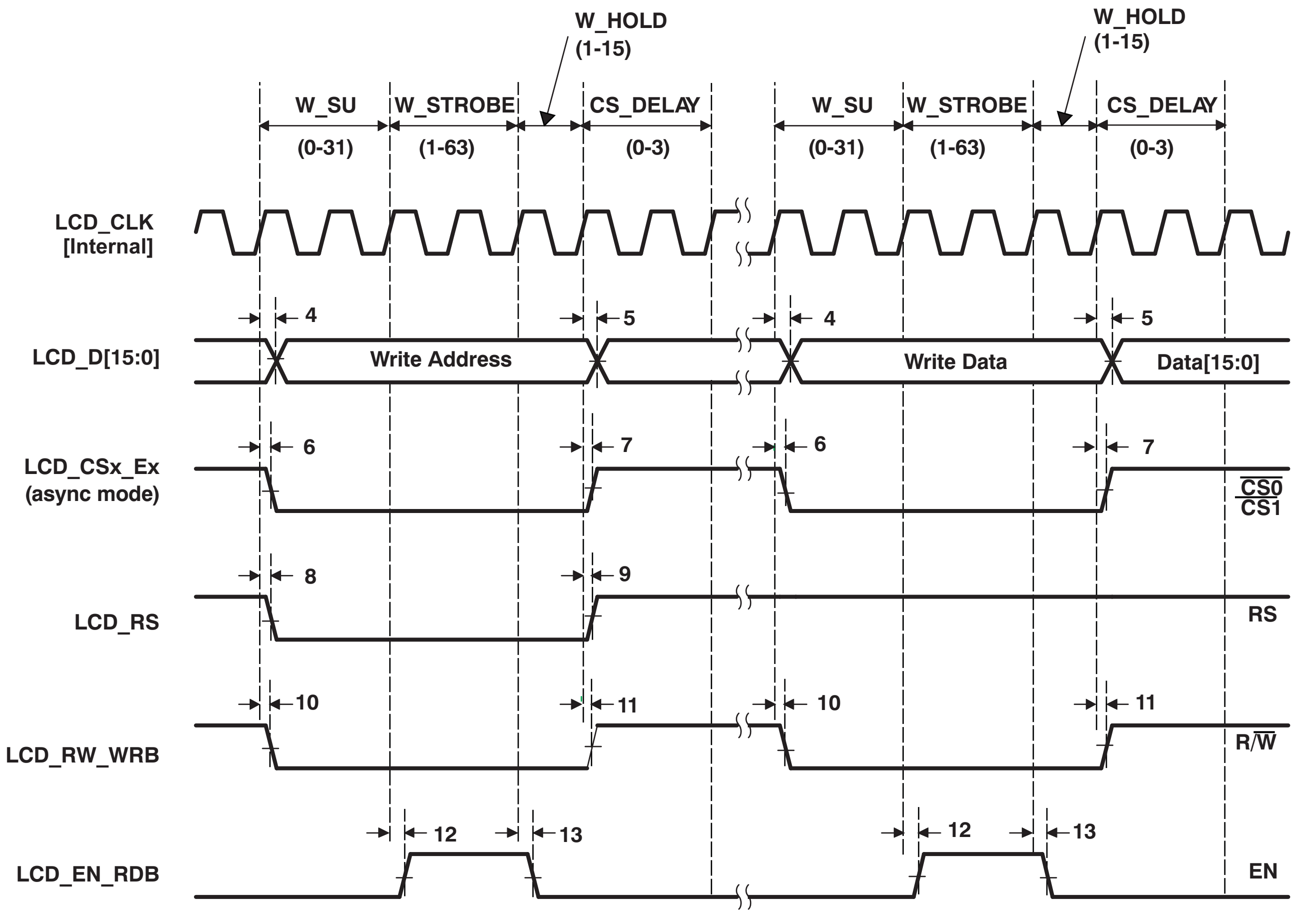


Figure 6-28. Micro-Interface Graphic Display 6800 Write

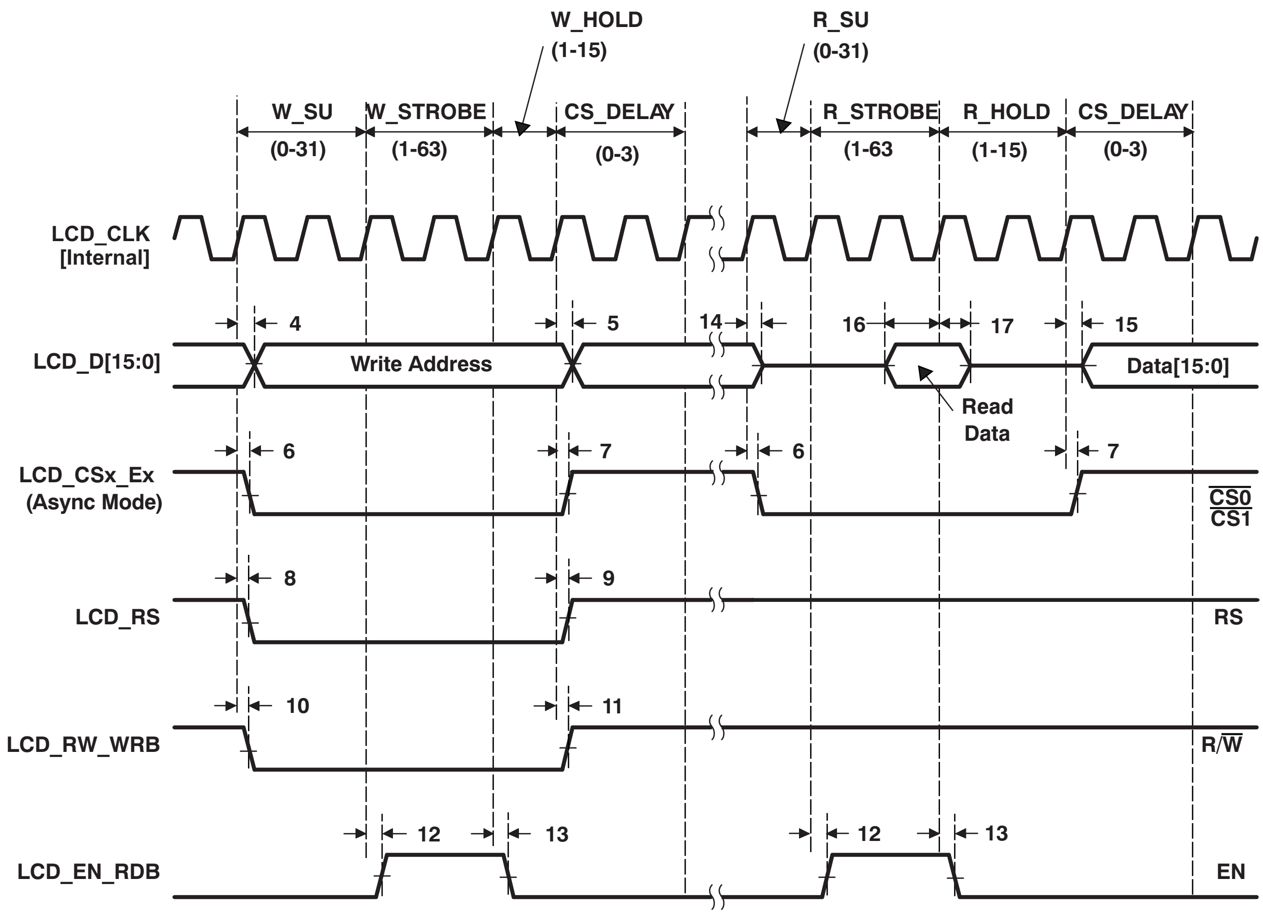


Figure 6-29. Micro-Interface Graphic Display 6800 Read

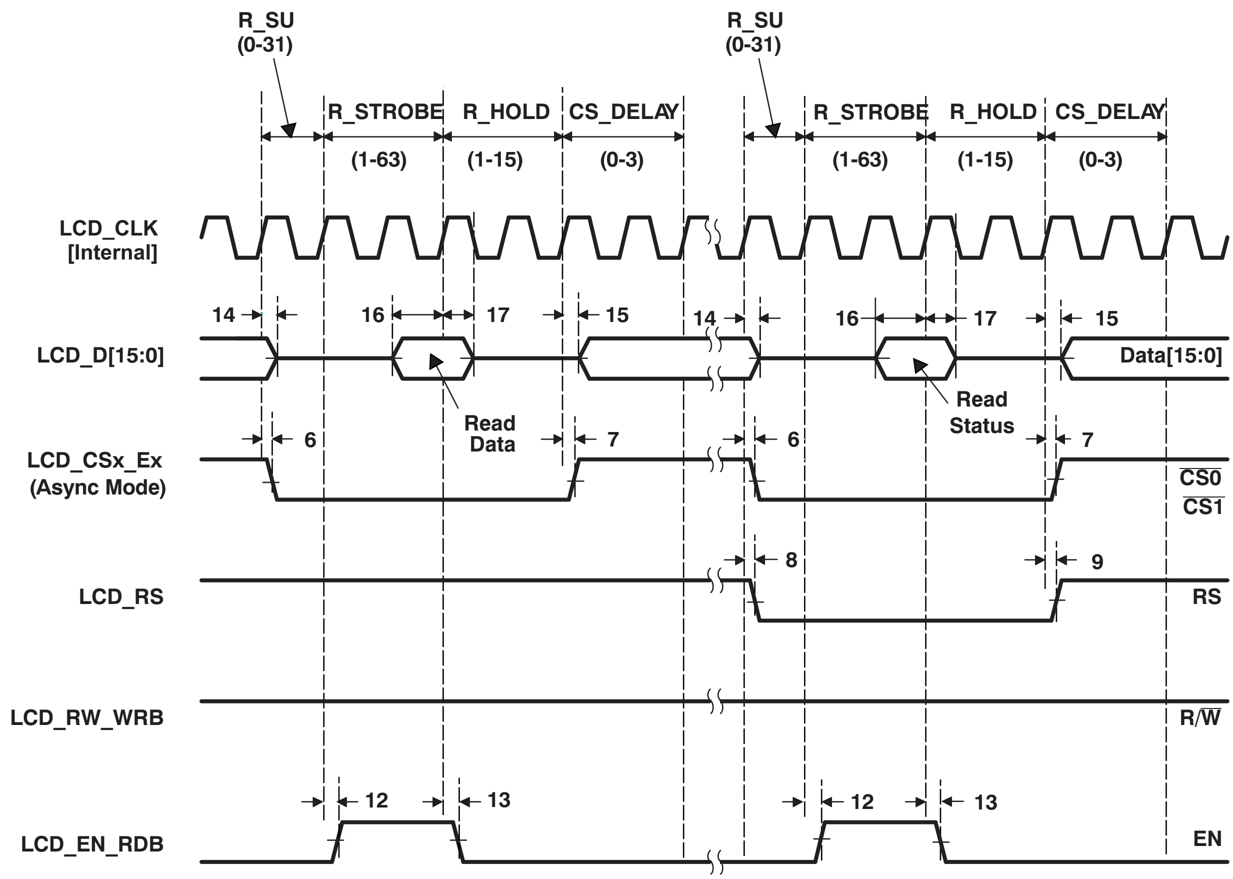


Figure 6-30. Micro-Interface Graphic Display 6800 Status

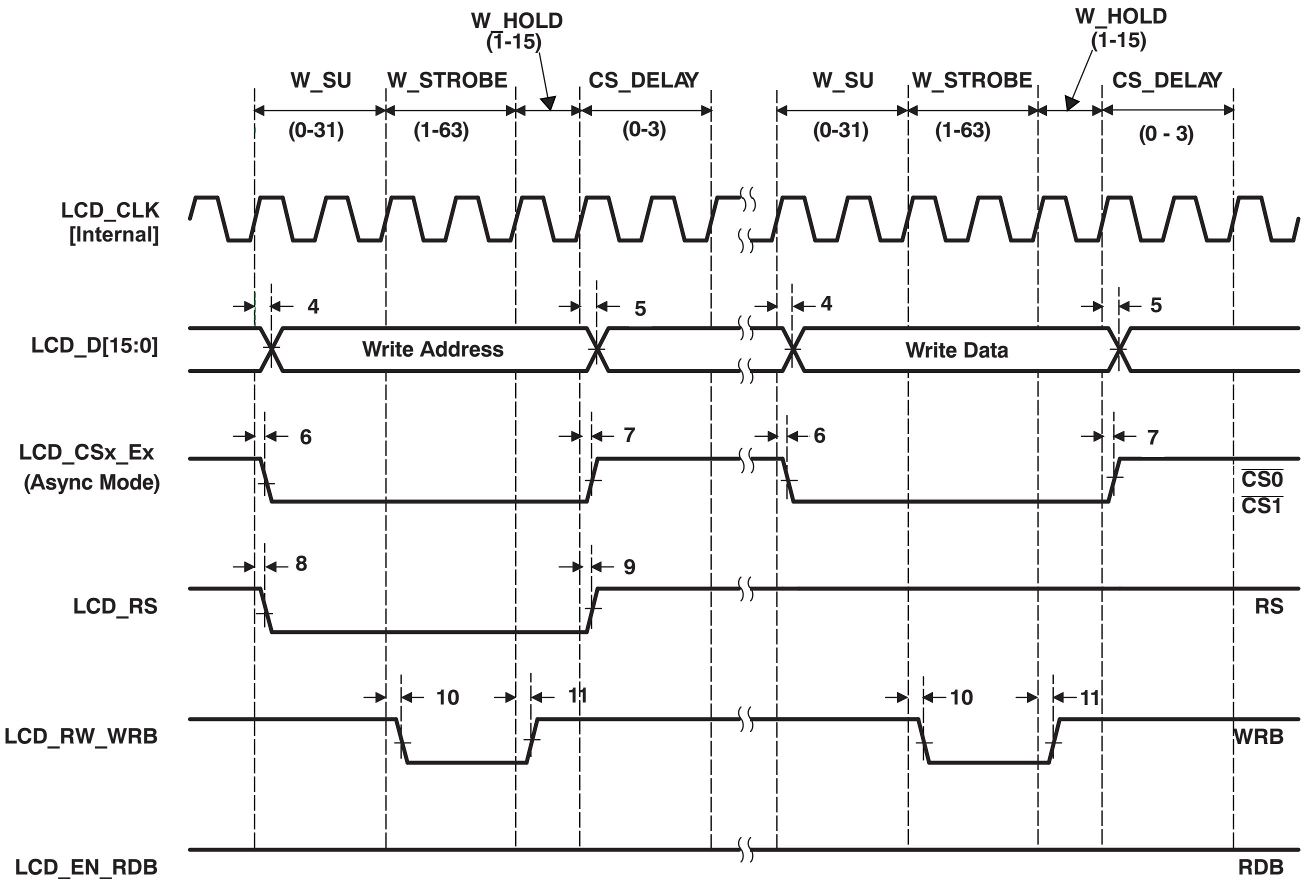


Figure 6-31. Micro-Interface Graphic Display 8080 Write

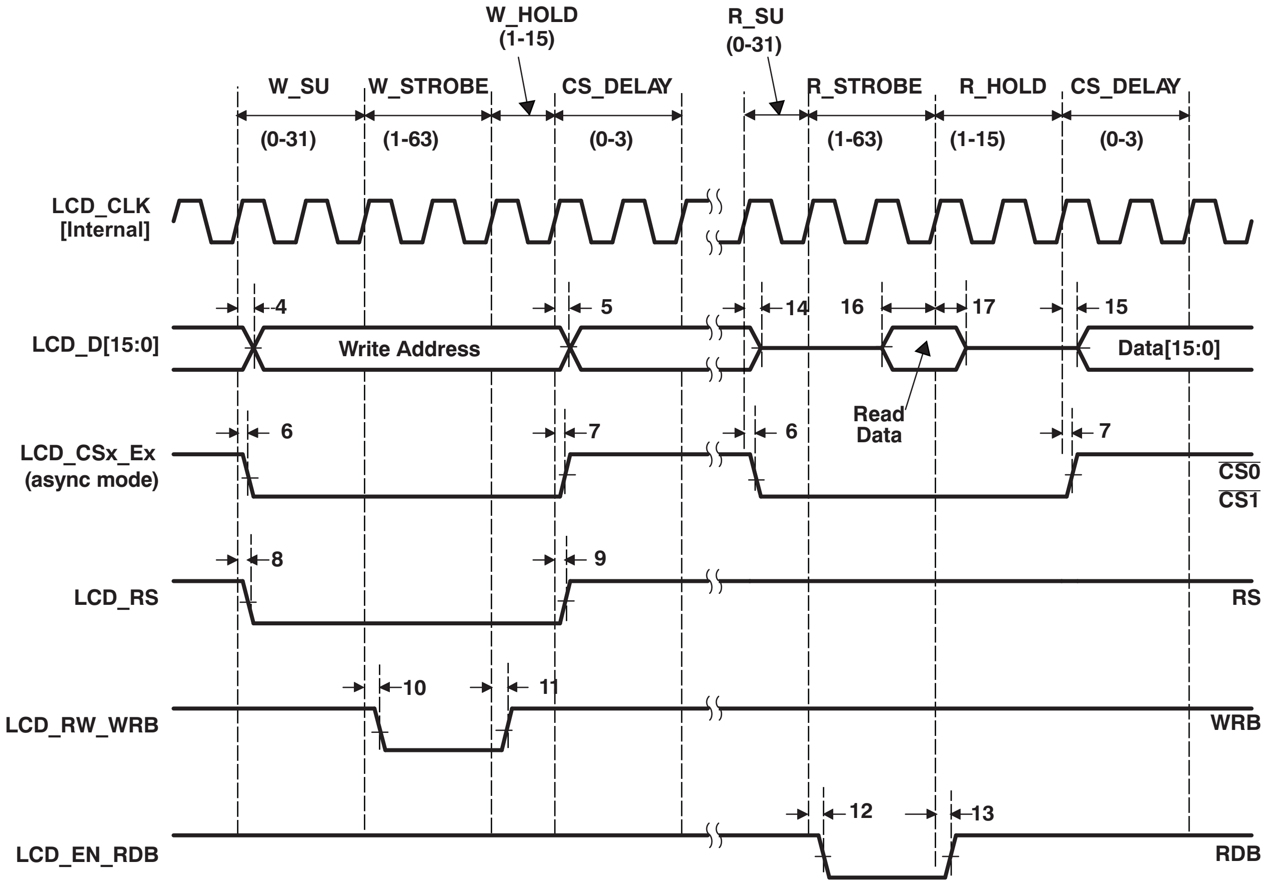


Figure 6-32. Micro-Interface Graphic Display 8080 Read

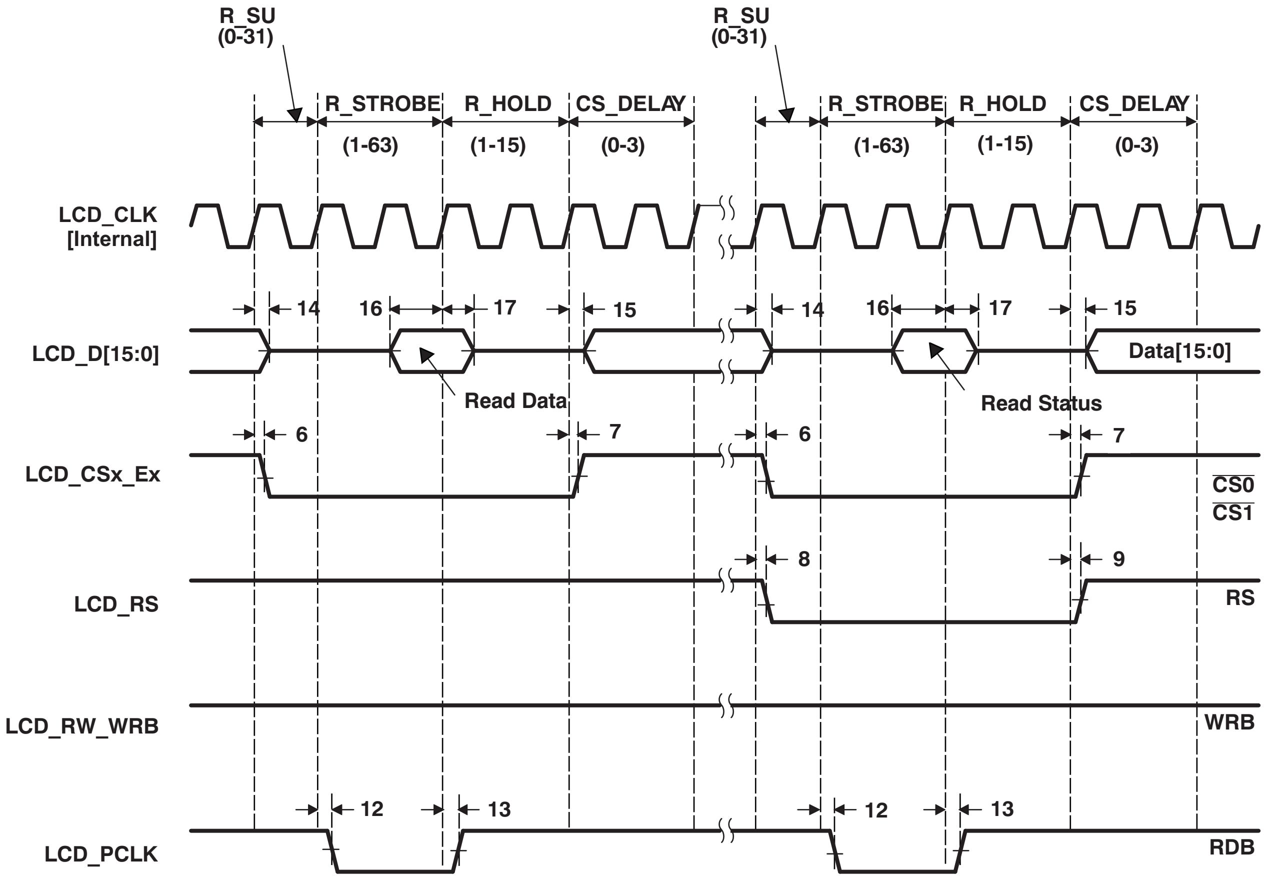


Figure 6-33. Micro-Interface Graphic Display 8080 Status

6.15.2.1 10-Bit SAR ADC

The VC5505 includes a 10-bit SAR ADC using a switched capacitor architecture which converts an analog input signal to a digital value at a maximum rate of 62.5-k samples per second (ksps) for use by the DSP. This SAR module supports six channels that are connected to four general purpose analog pins (GPAIN [3:0]) which can be used as general purpose outputs.

The VC5505 SAR supports the following features:

- Up to 62.5 ksps (2-MHz clock with 32 cycles per conversion)
- Single conversion and continuous back-to-back conversion modes
- Interrupt driven or polling conversion or DMA event generation
- Internal configurable bandgap reference voltages of 1 V or 0.8 V; or external V_{ref} of V_{DDA_ANA}
- One 3.6-V Tolerant analog input (GPAIN0) with internal voltage division for conversion of battery voltage
- Software controlled power down
- Individually configurable general-purpose digital outputs

6.15.2.1.1 SAR ADC Peripheral Register Description(s)

Table 6-38 shows the SAR ADC peripheral registers.

Table 6-38. SAR Analog Control Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
7012h	SARCTRL	SAR A/D Control Register
7014h	SARDATA	SAR A/D Data Register
7016h	SARCLKCTRL	SAR A/D Clock Control Register
7018h	SARPINCTRL	SAR A/D Reference and Pin Control Register
701Ah	SARGPOCTRL	SAR A/D GPO Control Register

6.15.2.1.2 SAR ADC Electrical Data/Timing

Table 6-39. Switching Characteristics Over Recommended Operating Conditions for ADC Characteristics

NO.	PARAMETER		CV_{DD} = 1.3 V CV_{DD} = 1.05 V MIN	TYP	MAX	UNIT
1	$t_{C(SCLC)}$	Cycle time, ADC internal conversion clock			2	MHz
3	$t_{d(CONV)}$	Delay time, ADC conversion time			$32t_{C(SCLC)}$	ns
4	S_{DNL}	Static differential non-linearity error (DNL measured for 9 bits)		±0.6		LSB
5	S_{INL}	Static integral non-linearity error		±1		LSB
6	Z_{set}	Zero-scale offset error			2	LSB
7	F_{set}	Full-scale offset error			2	LSB
8		Analog input impedance	1			MΩ
9		Signal-to-noise ratio		54		dB

6.16 Serial Port Interface (SPI)

The VC5505 serial port interface (SPI) is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI supports multi-chip operation of up to four SPI slave devices. The SPI can operate as a master device only, slave mode is not supported.

The SPI is normally used for communication between the DSP and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EEPROMs, and analog-to-digital converters.

The SPI has the following features:

- Programmable divider for serial data clock generation
- Four pin interface (SPI_CLK, SPI_CSn, SPI_RX, and SPI_TX)
- Programmable data length (1 to 32 bits)
- 4 external chip select signals
- Programmable transfer or frame size (1 to 4096 characters)
- Optional interrupt generation on character completion
- Programmable SPI_CSn to SPI_TX delay from 0 to 3 SPI_CLK cycles
- Programmable signal polarities
- Programmable active clock edge
- Internal loopback mode for testing

6.16.1 SPI Peripheral Register Description(s)

Table 6-40 shows the SPI registers.

Table 6-40. SPI Module Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
3000h	SPICDR	Clock Divider Register
3001h	SPICCR	Clock Control Register
3002h	SPIDCR1	Device Configuration Register 1
3003h	SPIDCR2	Device Configuration Register 2
3004h	SPICMD1	Command Register 1
3005h	SPICMD2	Command Register 2
3006h	SPISTAT1	Status Register 1
3007h	SPISTAT2	Status Register 2
3008h	SPIDAT1	Data Register 1
3009h	SPIDAT2	Data Register 2

6.16.2 SPI Electrical Data/Timing

Table 6-41. Timing Requirements for SPI input (see Figure 6-34 through Figure 6-37)

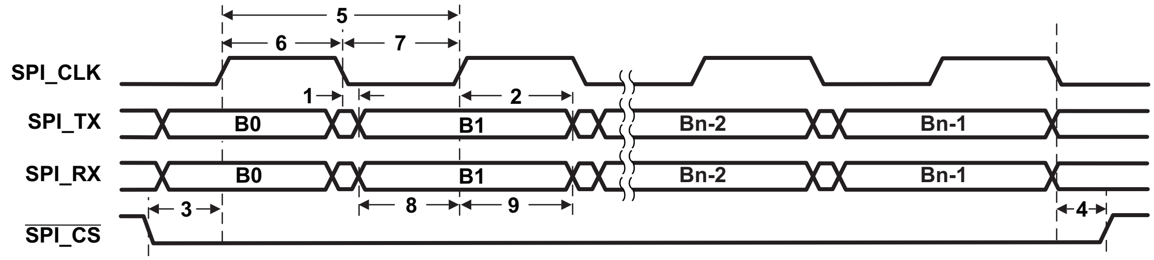
NO.			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
5	$t_{C(SCLK)}$	Cycle time, SPI_CLK	66.4 or 4P (1) (2)		40 or 4P (1) (2)		ns
6	$t_{w(SCLKH)}$	Pulse duration, SPI_CLK high	30		19		ns
7	$t_{w(SCLKL)}$	Pulse duration, SPI_CLK low	30		19		ns
8	$t_{su(SRXV-SCLK)}$	Setup time, SPI_RX valid before SPI_CLK high, SPI Mode 0	15		13		ns
		Setup time, SPI_RX valid before SPI_CLK low, SPI Mode 1	15		13		ns
		Setup time, SPI_RX valid before SPI_CLK high, SPI Mode 2	15		13		ns
		Setup time, SPI_RX valid before SPI_CLK high, SPI Mode 3	15		13		ns
9	$t_{h(SCLK-SRXV)}$	Hold time, SPI_RX vaild after SPI_CLK high, SPI Mode 0	0		0		ns
		Hold time, SPI_RX vaild after SPI_CLK low, SPI Mode 1	0		0		ns
		Hold time, SPI_RX vaild after SPI_CLK low, SPI Mode 2	0		0		ns
		Hold time, SPI_RX vaild after SPI_CLK high, SPI Mode 3	0		0		ns

(1) P = SYSCLK period in ns. For example, when running parts at 100 MHz, use P = 10 ns.
(2) Use whichever value is greater.

Table 6-42. Switching Characteristics Over Recommended Operating Conditions for SPI Outputs (see Figure 6-34 through Figure 6-37)

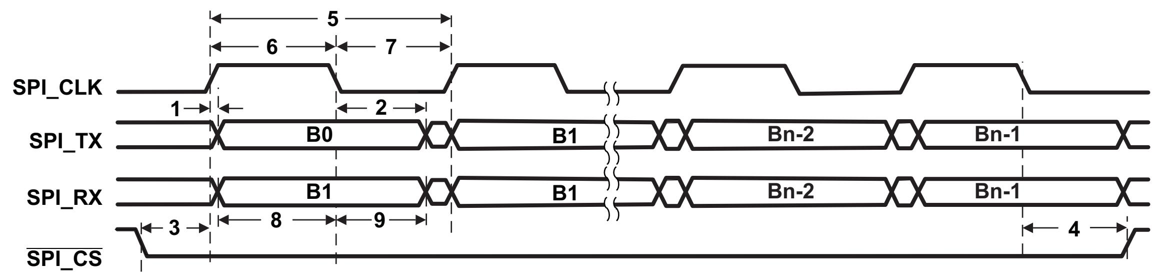
NO.	PARAMETER		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(SCLK-STXV)}$	Delay time, SPI_CLK low to SPI_TX vaild, SPI Mode 0		8		5	ns
		Delay time, SPI_CLK high to SPI_TX vaild, SPI Mode 1		8		5	ns
		Delay time, SPI_CLK high to SPI_TX vaild, SPI Mode 2		8		5	ns
		Delay time, SPI_CLK low to SPI_TX vaild, SPI Mode 3		8		5	ns
2	$t_{oh(SCLK-STXIV)}$	Output hold time, SPI_CLK high to SPI_TX invaild, SPI Mode 0	$t_{w(SCLKH)} - 4$		$t_{w(SCLKH)} - 4.5$		ns
		Output hold time, SPI_CLK low to SPI_TX invaild, SPI Mode 1	$t_{w(SCLKL)} - 4$		$t_{w(SCLKL)} - 4.5$		ns
		Output hold time, SPI_CLK low to SPI_TX invaild, SPI Mode 2	$t_{w(SCLKL)} - 4$		$t_{w(SCLKL)} - 4.5$		ns
		Output hold time, SPI_CLK high to SPI_TX invaild, SPI Mode 3	$t_{w(SCLKH)} - 4$		$t_{w(SCLKH)} - 4.5$		ns
3	$t_{d(SPICS-SCLK)}$	Delay time, $\overline{\text{SPI\_CS}}$ active to SPI_CLK active		t_C - 8 + D (1)		t_C - 8 + D (1)	ns
4	$t_{oh(SCLKI-SPICSI)}$	Output hold time, $\overline{\text{SPI\_CS}}$ inactive to SPI_CLK inactive	$0.5t_C - 2$		$0.5t_C - 2$		ns

(1) D is the programable data delay in ns. Data delay can be programmed to 0, 1, 2, or 3 SPICLK clock cycles.



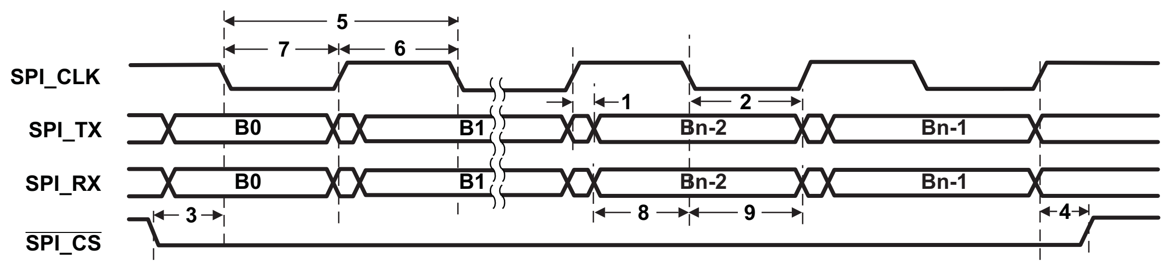
A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 6-34. SPI Mode 0 Transfer (CKP*n* = 0, CKPH*n* = 0)



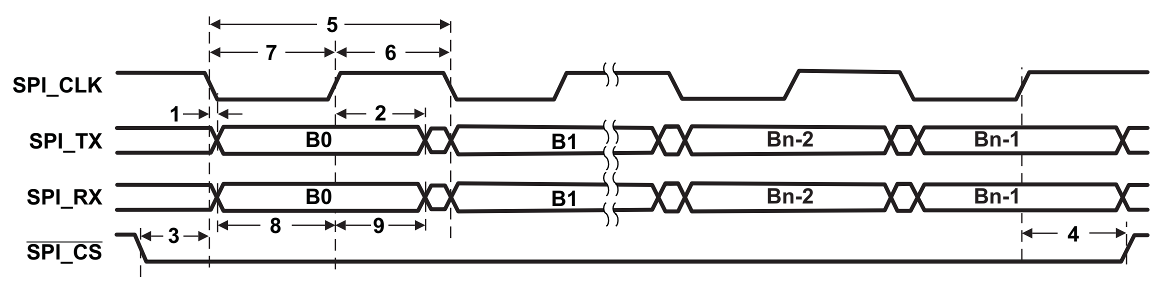
A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 6-35. SPI Mode 1 Transfer (CKP*n* = 0, CKPH*n* = 1)



A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 6-36. SPI Mode 2 Transfer (CKP*n* = 1, CKPH*n* = 0)



A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 6-37. SPI Mode 3 Transfer (CKP*n* = 1, CKPH*n* = 1)

6.17 Universal Serial Bus (USB) 2.0 Controller

The VC5505 USB2.0 peripheral supports the following features:

- USB 2.0 peripheral at speeds high-speed (480 Mb/s) and full-speed (12 Mb/s)
- All transfer modes (control, bulk, interrupt, and isochronous asynchronous mode)
- 4 Transmit (TX) and 4 Receive (RX) Endpoints in addition to Control Endpoint 0
- FIFO RAM
  - 4K endpoint
  - Programmable size
- Integrated USB 2.0 High Speed PHY
- RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB

The USB2.0 peripheral on this device, does *not* support:

- Host Mode (Peripheral/Device Modes supported *only*)
- On-Chip Charge Pump
- On-the-Go (OTG) Mode

6.17.1 USB2.0 Peripheral Register Description(s)

Table 6-43 lists of the USB2.0 peripheral registers.

Table 6-43. Universal Serial Bus (USB) Registers(1)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
8000h	REVID1	Revision Identification Register 1
8001h	REVID2	Revision Identification Register 2
8004h	CTRLR	Control Register
8008h	STATR	Status Register
800Ch	EMUR	Emulation Register
8010h	MODER1	Mode Register 1
8011h	MODER2	Mode Register 2
8014h	AUTOREQ	Auto Request Register
8018h	SRPFIXTIME1	SRP Fix Time Register 1
8019h	SRPFIXTIME2	SRP Fix Time Register 2
801Ch	TEARDOWN1	Teardown Register 1
801Dh	TEARDOWN2	Teardown Register 2
8020h	INTSRCR1	USB Interrupt Source Register 1
8021h	INTSRCR2	USB Interrupt Source Register 2
8024h	INTSETR1	USB Interrupt Source Set Register 1
8025h	INTSETR2	USB Interrupt Source Set Register 2
8028h	INTCLRR1	USB Interrupt Source Clear Register 1
8029h	INTCLRR2	USB Interrupt Source Clear Register 2
802Ch	INTMSKR1	USB Interrupt Mask Register 1
802Dh	INTMSKR2	USB Interrupt Mask Register 2
8030h	INTMSKSETR1	USB Interrupt Mask Set Register 1
8031h	INTMSKSETR2	USB Interrupt Mask Set Register 2
8034h	INTMSKCLRR1	USB Interrupt Mask Clear Register 1
8035h	INTMSKCLRR2	USB Interrupt Mask Clear Register 2
8038h	INTMASKEDR1	USB Interrupt Source Masked Register 1

(1) Before reading or writing to the USB registers, be sure to set the BYTEMODE bits to "00b" in the USB system control register to enable word accesses to the USB registers .

Table 6-43. Universal Serial Bus (USB) Registers (1) (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
8039h	INTMASKEDR2	USB Interrupt Source Masked Register 2
803Ch	EOIR	USB End of Interrupt Register
8040h	INTVECTR1	USB Interrupt Vector Register 1
8041h	INTVECTR2	USB Interrupt Vector Register 2
8050h	GREP1SZR1	Generic RNDIS EP1Size Register 1
8051h	GREP1SZR2	Generic RNDIS EP1Size Register 2
8054h	GREP2SZR1	Generic RNDIS EP2 Size Register 1
8055h	GREP2SZR2	Generic RNDIS EP2 Size Register 2
8058h	GREP3SZR1	Generic RNDIS EP3 Size Register 1
8059h	GREP3SZR2	Generic RNDIS EP3 Size Register 2
805Ch	GREP4SZR1	Generic RNDIS EP4 Size Register 1
805Dh	GREP4SZR2	Generic RNDIS EP4 Size Register 2
Common USB Registers		
8400h	FADDR_POWER	Function Address Register, Power Management Register
8401h	INTRTX	Interrupt Register for Endpoint 0 plus Transmit Endpoints 1 to 4
8404h	INTRRX	Interrupt Register for Receive Endpoints 1 to 4
8405h	INTRTXE	Interrupt enable register for INTRTX
8408h	INTRRXE	Interrupt Enable Register for INTRRX
8409h	INTRUSB_INTRUSBE	Interrupt Register for Common USB Interrupts, Interrupt Enable Register
840Ch	FRAME	Frame Number Register
840Dh	INDEX_TESTMODE	Index Register for Selecting the Endpoint Status and Control Registers, Register to Enable the USB 2.0 Test Modes
USB Indexed Registers		
8410h	TXMAXP_INDX	Maximum Packet Size for Peripheral/Host Transmit Endpoint. (Index register set to select Endpoints 1-4)
8411h	PERI_CSR0_INDX	Control Status Register for Endpoint 0 in Peripheral Mode. (Index register set to select Endpoint 0)
	PERI_TXCSR_INDX	Control Status Register for Peripheral Transmit Endpoint. (Index register set to select Endpoints 1-4)
8414h	RXMAXP_INDX	Maximum Packet Size for Peripheral/Host Receive Endpoint. (Index register set to select Endpoints 1-4)
8415h	PERI_RXCSR_INDX	Control Status Register for Peripheral Receive Endpoint. (Index register set to select Endpoints 1-4)
8418h	COUNT0_INDX	Number of Received Bytes in Endpoint 0 FIFO. (Index register set to select Endpoint 0)
	RXCOUNT_INDX	Number of Bytes in Host Receive Endpoint FIFO. (Index register set to select Endpoints 1- 4)
8419h	-	Reserved
841Ch	-	Reserved
841Dh	CONFIGDATA_INDC (Upper byte of 841Dh)	Returns details of core configuration. (index register set to select Endpoint 0)
USB FIFO Registers		
8420h	FIFO0R1	Transmit and Receive FIFO Register 1 for Endpoint 0
8421h	FIFO0R2	Transmit and Receive FIFO Register 2 for Endpoint 0
8424h	FIFO1R1	Transmit and Receive FIFO Register 1 for Endpoint 1
8425h	FIFO1R2	Transmit and Receive FIFO Register 2 for Endpoint 1
8428h	FIFO2R1	Transmit and Receive FIFO Register 1 for Endpoint 2
8429h	FIFO2R2	Transmit and Receive FIFO Register 2 for Endpoint 2
842Ch	FIFO3R1	Transmit and Receive FIFO Register 1 for Endpoint 3

Table 6-43. Universal Serial Bus (USB) Registers [(1)] (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
842Dh	FIFO3R2	Transmit and Receive FIFO Register 2 for Endpoint 3
8430h	FIFO4R1	Transmit and Receive FIFO Register 1 for Endpoint 4
8431h	FIFO4R2	Transmit and Receive FIFO Register 2 for Endpoint 4
	Dynamic FIFO Control Registers	
8460h	-	Reserved
8461h	TXFIFOSZ_RXFIFOSZ	Transmit Endpoint FIFO Size, Receive Endpoint FIFO Size (Index register set to select Endpoints 1-4)
8464h	TXFIFOADDR	Transmit Endpoint FIFO Address (Index register set to select Endpoints 1-4)
8465h	RXFIFOADDR	Receive Endpoint FIFO Address (Index register set to select Endpoints 1-4)
846Ch	-	Reserved
	Control and Status Register for Endpoint 0	
8500h	-	Reserved
8501h	PERI_CSR0	Control Status Register for Peripheral Endpoint 0
8504h	-	Reserved
8505h	-	Reserved
8508h	COUNT0	Number of Received Bytes in Endpoint 0 FIFO
8509h	-	Reserved
850Ch	-	Reserved
850Dh	CONFIGDATA (Upper byte of 850Dh)	Returns details of core configuration.
	Control and Status Register for Endpoint 1	
8510h	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
8511h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8514h	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
8515h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8518h	RXCOUNT	Number of Bytes in the Receiving Endpoint's FIFO
8519h	-	Reserved
851Ch	-	Reserved
851Dh	-	Reserved
	Control and Status Register for Endpoint 2	
8520h	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
8521h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8524h	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
8525h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8528h	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
8529h	-	Reserved
852Ch	-	Reserved
852Dh	-	Reserved
	Control and Status Register for Endpoint 3	
8530h	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
8531h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8534h	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
8535h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8538h	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
8539h	-	Reserved
853Ch	-	Reserved
853Dh	-	Reserved

Table 6-43. Universal Serial Bus (USB) Registers (1) (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
		Control and Status Register for Endpoint 4
8540h	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
8541h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8544h	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
8545h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8548h	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
8549h	-	Reserved
854Ch	-	Reserved
854Dh	-	Reserved
		CPPI DMA (CMDA) Registers
9000h	-	Reserved
9001h	-	Reserved
9004h	TDFDQ	CDMA Teardown Free Descriptor Queue Control Register
9008h	DMAEMU	CDMA Emulation Control Register
9800h	TXGCR1[0]	Transmit Channel 0 Global Configuration Register 1
9801h	TXGCR2[0]	Transmit Channel 0 Global Configuration Register 2
9808h	RXGCR1[0]	Receive Channel 0 Global Configuration Register 1
9809h	RXGCR2[0]	Receive Channel 0 Global Configuration Register 2
980Ch	RXHPCR1A[0]	Receive Channel 0 Host Packet Configuration Register 1 A
980Dh	RXHPCR2A[0]	Receive Channel 0 Host Packet Configuration Register 2 A
9810h	RXHPCR1B[0]	Receive Channel 0 Host Packet Configuration Register 1 B
9811h	RXHPCR2B[0]	Receive Channel 0 Host Packet Configuration Register 2 B
9820h	TXGCR1[1]	Transmit Channel 1 Global Configuration Register 1
9821h	TXGCR2[1]	Transmit Channel 1 Global Configuration Register 2
9828h	RXGCR1[1]	Receive Channel 1 Global Configuration Register 1
9829h	RXGCR2[1]	Receive Channel 1 Global Configuration Register 2
982Ch	RXHPCR1A[1]	Receive Channel 1 Host Packet Configuration Register 1 A
982Dh	RXHPCR2A[1]	Receive Channel 1 Host Packet Configuration Register 2 A
9830h	RXHPCR1B[1]	Receive Channel 1 Host Packet Configuration Register 1 B
9831h	RXHPCR2B[1]	Receive Channel 1 Host Packet Configuration Register 2 B
9840h	TXGCR1[2]	Transmit Channel 2 Global Configuration Register 1
9841h	TXGCR2[2]	Transmit Channel 2 Global Configuration Register 2
9848h	RXGCR1[2]	Receive Channel 2 Global Configuration Register 1
9849h	RXGCR2[2]	Receive Channel 2 Global Configuration Register 2
984Ch	RXHPCR1A[2]	Receive Channel 2 Host Packet Configuration Register 1 A
984Dh	RXHPCR2A[2]	Receive Channel 2 Host Packet Configuration Register 2 A
9850h	RXHPCR1B[2]	Receive Channel 2 Host Packet Configuration Register 1 B
9851h	RXHPCR2B[2]	Receive Channel 2 Host Packet Configuration Register 2 B
9860h	TXGCR1[3]	Transmit Channel 3 Global Configuration Register 1
9861h	TXGCR2[3]	Transmit Channel 3 Global Configuration Register 2
9868h	RXGCR1[3]	Receive Channel 3 Global Configuration Register 1
9869h	RXGCR2[3]	Receive Channel 3 Global Configuration Register 2
986Ch	RXHPCR1A[3]	Receive Channel 3 Host Packet Configuration Register 1 A
986Dh	RXHPCR2A[3]	Receive Channel 3 Host Packet Configuration Register 2 A
9870h	RXHPCR1B[3]	Receive Channel 3 Host Packet Configuration Register 1 B
9871h	RXHPCR2B[3]	Receive Channel 3 Host Packet Configuration Register 2 B

Table 6-43. Universal Serial Bus (USB) Registers (1) (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
A000h	DMA_SCHED_CTRL1	CDMA Scheduler Control Register 1
A001h	DMA_SCHED_CTRL2	CDMA Scheduler Control Register 1
A800h + 4 × *N*	ENTRYLSW[*N*]	CDMA Scheduler Table Word *N* Registers LSW (*N* = 0 to 63)
A801h + 4 × *N*	ENTRYMSW[*N*]	CDMA Scheduler Table Word *N* Registers MSW (*N* = 0 to 63)
	Queue Manager (QMGR) Registers	
C000h	-	Reserved
C001h	-	Reserved
C008h	DIVERSION1	Queue Manager Queue Diversion Register 1
C009h	DIVERSION2	Queue Manager Queue Diversion Register 2
C020h	FDBSC0	Queue Manager Free Descriptor/Buffer Starvation Count Register 0
C021h	FDBSC1	Queue Manager Free Descriptor/Buffer Starvation Count Register 1
C024h	FDBSC2	Queue Manager Free Descriptor/Buffer Starvation Count Register 2
C025h	FDBSC3	Queue Manager Free Descriptor/Buffer Starvation Count Register 3
C028h	FDBSC4	Queue Manager Free Descriptor/Buffer Starvation Count Register 4
C029h	FDBSC5	Queue Manager Free Descriptor/Buffer Starvation Count Register 5
C02Ch	FDBSC6	Queue Manager Free Descriptor/Buffer Starvation Count Register 6
C02Dh	FDBSC7	Queue Manager Free Descriptor/Buffer Starvation Count Register 7
C080h	LRAM0BASE1	Queue Manager Linking RAM Region 0 Base Address Register 1
C081h	LRAM0BASE2	Queue Manager Linking RAM Region 0 Base Address Register 2
C084h	LRAM0SIZE	Queue Manager Linking RAM Region 0 Size Register
C085h	-	Reserved
C088h	LRAM1BASE1	Queue Manager Linking RAM Region 1 Base Address Register 1
C089h	LRAM1BASE2	Queue Manager Linking RAM Region 1 Base Address Register 2
C090h	PEND0	Queue Manager Queue Pending 0
C091h	PEND1	Queue Manager Queue Pending 1
C094h	PEND2	Queue Manager Queue Pending 2
C095h	PEND3	Queue Manager Queue Pending 3
C098h	PEND4	Queue Manager Queue Pending 4
C099h	PEND5	Queue Manager Queue Pending 5
D000h + 16 × *R*	QMEMRBASE1[*R*]	Queue Manager Memory Region *R* Base Address Register 1 (*R* = 0 to 15)
D001h + 16 × *R*	QMEMRBASE2[*R*]	Queue Manager Memory Region *R* Base Address Register 2 (*R* = 0 to 15)
D004h + 16 × *R*	QMEMRCTRL1[*R*]	Queue Manager Memory Region *R* Control Register (*R* = 0 to 15)
D005h + 16 × *R*	QMEMRCTRL2[*R*]	Queue Manager Memory Region *R* Control Register (*R* = 0 to 15)
E000h + 16 × *N*	CTRL1A	Queue Manager Queue *N* Control Register 1A (*N* = 0 to 63)
E001h + 16 × *N*	CTRL2A	Queue Manager Queue *N* Control Register 2A (*N* = 0 to 63)
E004h + 16 × *N*	CTRL1B	Queue Manager Queue *N* Control Register 1B (*N* = 0 to 63)
E005h + 16 × *N*	CTRL2B	Queue Manager Queue *N* Control Register 2B (*N* = 0 to 63)
E008h + 16 × *N*	CTRL1C	Queue Manager Queue *N* Control Register 1C (*N* = 0 to 63)
E009h + 16 × *N*	CTRL2C	Queue Manager Queue *N* Control Register 2C (*N* = 0 to 63)
E00Ch + 16 × *N*	CTRL1D	Queue Manager Queue *N* Control Register 1D (*N* = 0 to 63)
E00Dh + 16 × *N*	CTRL2D	Queue Manager Queue *N* Control Register 2D (*N* = 0 to 63)
E800h + 16 × *N*	QSTAT1A	Queue Manager Queue *N* Status Register 1A (*N* = 0 to 63)
E801h + 16 × *N*	QSTAT2A	Queue Manager Queue *N* Status Register 2A (*N* = 0 to 63)
E804h + 16 × *N*	QSTAT1B	Queue Manager Queue *N* Status Register 1B (*N* = 0 to 63)
E805h + 16 × *N*	QSTAT2B	Queue Manager Queue *N* Status Register 2B (*N* = 0 to 63)
E808h + 16 × *N*	QSTAT1C	Queue Manager Queue *N* Status Register 1C (*N* = 0 to 63)

Table 6-43. Universal Serial Bus (USB) Registers [(1)] (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
E809h + 16 × *N*	QSTAT1C	Queue Manager Queue *N* Status Register 2C (*N* = 0 to 63)

6.17.2 USB2.0 Electrical Data/Timing

Table 6-44. Switching Characteristics Over Recommended Operating Conditions for USB2.0 (see Figure 6-38)

NO.	PARAMETER		CV_{DD} = 1.05 V, CV_{DD} = 1.3 V FULL SPEED 12 Mbps MIN	FULL SPEED 12 Mbps MAX	HIGH SPEED 480 Mbps(1) MIN	HIGH SPEED 480 Mbps(1) MAX	UNIT
1	$t_{r(D)}$	Rise time, USB_DP and USB_DM signals(2)	4	20	0.5		ns
2	$t_{f(D)}$	Fall time, USB_DP and USB_DM signals(2)	4	20	0.5		ns
3	t_{rfM}	Rise/Fall time, matching(3)	90	111	–	–	%
4	V_{CRS}	Output signal cross-over voltage(2)	1.3	2	–	–	V
7	$t_{w(EOPT)}$	Pulse duration, EOP transmitter(4)	160	175	–	–	ns
8	$t_{w(EOPR)}$	Pulse duration, EOP receiver(4)	82		–		ns
9	$t_{(DRATE)}$	Data Rate		12		480	Mb/s
10	Z_{DRV}	Driver Output Resistance	40.5	49.5	40.5	49.5	Ω
11	Z_{INP}	Receiver Input Impedance	100k		-	-	Ω

(1) For more detailed informaton, see the Universal Serial Bus Specification, Revision 2.0, Chapter 7.
(2) Full Speed and High Speed C_L = 50 pF
(3) $t_{RFM} = (t_r/t_f) \times 100$. [Excluding the first transaction from the Idle state.]
(4) Must accept as valid EOP

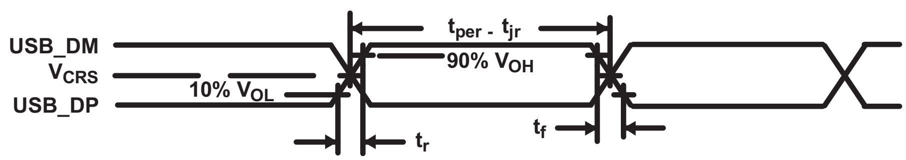


Figure 6-38. USB2.0 Integrated Transceiver Interface Timing

6.18 General-Purpose Timers

The VC5505 has three 32-bit software programmable Timers. Each timer can be used as a general- purpose (GP) timer. Timer2 can be configured as either a GP or a Watchdog (WD) or both. General-purpose timers are typically used to provide interrupts to the CPU to schedule periodic tasks or a delayed task. A watchdog timer is used to reset the CPU in case it gets into an infinite loop. The GP timers are 32-bit timers with a 13-bit prescaler that can divide the CPU clock and uses this scaled value as a reference clock. These timers can be used to generate periodic interrupts. The Watchdog Timer is a 16-bit counter with a 16-bit prescaler used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

The VC5505 Timers support the following:

- 32-bit Programmable Countdown Timer
- 13-bit Prescaler Divider
- Timer Modes:
  - 32-bit General-Purpose Timer
  - 32-bit Watchdog Timer (Timer2 only)
- Auto Reload Option
- Generates Single Interrupt to CPU (The interrupt is individually latched to determine which timer triggered the interrupt.)
- Generates Active Low Pulse to the Hardware Reset (Watchdog *only*)
- Interrupt can be Used for DMA Event

6.18.1 Timers Peripheral Register Description(s)

Table 6-45 through Table 6-48 show the Timer and Watchdog registers.

Table 6-45. Watchdog Timer Registers (Timer2 *only*)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1880h	WDKCKLK	Watchdog Kick Lock Register
1882h	WDKICK	Watchdog Kick Register
1884h	WDSVLR	Watchdog Start Value Lock Register
1886h	WDSVR	Watchdog Start Value Register
1888h	WDENLOK	Watchdog Enable Lock Register
188Ah	WDEN	Watchdog Enable Register
188Ch	WDPSLR	Watchdog Prescale Lock Register
188Eh	WDPS	Watchdog Prescale Register

Table 6-46. General-Purpose Timer 0 Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1810h	TCR	Timer 0 Control Register
1812h	TIMPRD1	Timer 0 Period Register 1
1813h	TIMPRD2	Timer 0 Period Register 2
1814h	TIMCNT1	Timer 0 Counter Register 1
1815h	TIMCNT2	Timer 0 Counter Register 2

Table 6-47. General-Purpose Timer 1 Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1850h	TCR	Timer 1 Control Register

Table 6-47. General-Purpose Timer 1 Registers (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1852h	TIMPRD1	Timer 1 Period Register 1
1853h	TIMPRD2	Timer 1 Period Register 2
1854h	TIMCNT1	Timer 1 Counter Register 1
1855h	TIMCNT2	Timer 1 Counter Register 2

Table 6-48. General-Purpose Timer 2 Registers

CPU WPRD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1890h	TCR	Timer 2 Control Register
1892h	TIMPRD1	Timer 2 Period Register 1
1893h	TIMPRD2	Timer 2 Period Register 2
1894h	TIMCNT1	Timer 2 Counter Register 1
1895h	TIMCNT2	Timer 2 Counter Register 2

6.19 General-Purpose Input/Output

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of the internal register. The GPIO can also be used to send interrupts to the CPU.

The VC5505 GPIO peripheral supports the following:

- Up to 26 GPIOs plus 1 general-purpose output (XF) and 4 Special-Purpose Outputs for Use With SAR
- All GPIO pins have internal pulldowns (IPDs) which can be individually disabled
- Output Set/Clear functionality through writing a single output data register
- All GPIOs can be configured to generate edge detected interrupts to the CPU on either the rising or falling edge

VC5505 GPIO pin functions are multiplexed with various other signals. For more detailed information on what signals are multiplexed with the GPIO and how to configure them, see Section 3.5, *Terminal Functions* and Section 4, *Device Configuration* of this document.

6.19.1 General-Purpose Input/Output Peripheral Register Description(s)

The external parallel port interface includes a 16-bit general purpose I/O that can be individually programmed as input or output with interrupt capability. Control of the general purpose I/O is maintained through a set of I/O memory-mapped registers shown in Table 6-49.

Table 6-49. GPIO Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
1C06h	IODIR1	GPIO Direction Register 1
1C07h	IODIR2	GPIO Direction Register 2
1C08h	IOINDATA1	GPIO Data In Register 1
1C09h	IOINDATA2	GPIO Data In Register 2
1C0Ah	IODATAOUT1	GPIO Data Out Register 1
1C0Bh	IODATAOUT2	GPIO Data Out Register 2
1C0Ch	IOINTEDG1	GPIO Interrupt Edge Trigger Enable Register 1
1C0Dh	IOINTEDG2	GPIO Interrupt Edge Trigger Enable Register 2
1C0Eh	IOINTEN1	GPIO Interrupt Enable Register 1
1C0Fh	IOINTEN2	GPIO Interrupt Enable Register 2
1C10h	IOINTFLG1	GPIO Interrupt Flag Register 1
1C11h	IOINTFLG2	GPIO Interrupt Flag Register 2

6.19.2 GPIO Peripheral Input/Output Electrical Data/Timing

Table 6-50. Timing Requirements for GPIO Inputs[(1)] (see Figure 6-39)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V MIN	MAX	UNIT
1	$t_{w(ACTIVE)}$	Pulse duration, GPIO input/external interrupt pulse active	2C[(1) (2)]		ns
2	$t_{w(INACTIVE)}$	Pulse duration, GPIO input/external interrupt pulse inactive	C[(1) (2)]		ns

(1) The pulse width given is sufficient to get latched into the GPIO_IFR register and to generate an interrupt. However, if a user wants to have the device recognize the GPIO changes through software polling of the GPIO Data In (GPIO_DIN) register, the GPIO duration must be extended to allow the device enough time to access the GPIO register through the internal bus.
(2) C = SYSCLK period in ns. For example, when running parts at 100 MHz, use C = 10 ns.

Table 6-51. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs (see Figure 6-39)

NO.	PARAMETER		CV_{DD} = 1.05 V CV_{DD} = 1.3 V MIN	MAX	UNIT
3	$t_{w(GPOH)}$	Pulse duration, GP[x] output high	3C[(1) (2)]		ns
4	$t_{w(GPOL)}$	Pulse duration, GP[x] output low	3C[(1) (2)]		ns

(1) This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.
(2) C = SYSCLK period in ns. For example, when running parts at 100 MHz, use C = 10 ns.

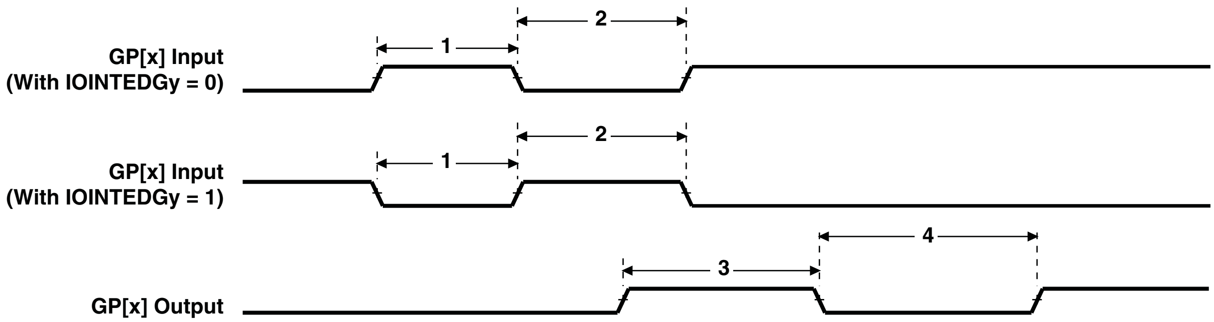


Figure 6-39. GPIO Port Timing

6.19.3 GPIO Peripheral Input Latency Electrical Data/Timing

Table 6-52. Timing Requirements for GPIO Input Latency(1)

NO.				CV_{DD} = 1.05 V CV_{DD} = 1.3 V		UNIT
				MIN	MAX	
1	$t_{L(GPI)}$	Latency, GP[x] input	Polling GPIO_DIN register	5		cyc
			Polling GPIO_IFR register	7		cyc
			Interrupt Detection	8		cyc

(1) The pulse width given is sufficient to generate a CPU interrupt. However, if a user wants to have VC5505 recognize the GP[x] input changes through software polling of the GPIO register, the GP[x] input duration must be extended to allow device enough time to access the GPIO register through the internal bus.

6.20 IEEE 1149.1 JTAG

The JTAG interface is used for Boundary-Scan testing and emulation of the VC5505 device.

$\overline{TRST}$ should only to be deasserted when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality.

The VC5505 includes an internal pulldown (IPD) on the $\overline{TRST}$ pin to ensure that $\overline{TRST}$ will always be asserted upon power up and the device's internal emulation logic will always be properly initialized. It is also recommended that an external pulldown be added to ensure proper device operation when an emulation or boundary scan JTAG controller is not connected to the JTAG pins. JTAG controllers from Texas Instruments actively drive $\overline{TRST}$ high. However, some third-party JTAG controllers may not drive $\overline{TRST}$ high but expect the use of a pullup resistor on $\overline{TRST}$. When using this type of JTAG controller, assert $\overline{TRST}$ to initialize the device after powerup and externally drive $\overline{TRST}$ high before attempting any emulation or boundary scan operations. The VC5505 device will not operate properly if $\overline{TRST}$ is not asserted low during powerup.

6.20.1 JTAG ID (JTAGID) Register Description(s)

Table 6-53. JTAG ID Register

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
N/A	JTAGID	JTAG Identification Register	Read-only. Provides 32-bit JTAG ID of the device.

The JTAG ID register is a read-only register that identifies to the customer the JTAG/Device ID. The register hex value for VC5505 is: 0x0009 702F. For the actual register bit names and their associated bit field descriptions, see Figure 6-40 and Table 6-54.

31-28	27-12	11-1	0
VARIANT (4-Bit)	PART NUMBER (16-Bit)	MANUFACTURER (11-Bit)	LSB
R-0000	R-0000 0000 1001 0111	R-0000 0010 111	R-1

LEGEND: R = Read, W = Write, n = value at reset

Figure 6-40. JTAG ID Register Description - VC5505 Register Value - 0x0009 702F

Table 6-54. JTAG ID Register Selection Bit Descriptions

BIT	NAME	DESCRIPTION
31:28	VARIANT	Variant (4-Bit) value. VC5505 value: 0000.
27:12	PART NUMBER	Part Number (16-Bit) value. VC5505 value: 0000 0000 1001 0111.
11:1	MANUFACTURER	Manufacturer (11-Bit) value. VC5505 value: 0000 0010 111.
0	LSB	LSB. This bit is read as a "1" for VC5505 .

6.20.2 JTAG Test_port Electrical Data/Timing

Table 6-55. Timing Requirements for JTAG Test Port (see Figure 6-41)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V		UNIT
			MIN	MAX	
2	$t_{c(TCK)}$	Cycle time, TCK	60		ns
3	$t_{w(TCKH)}$	Pulse duration, TCK high	24		ns
4	$t_{w(TCKL)}$	Pulse duration, TCK low	24		ns
5	$t_{su(TDIV-TCKH)}$	Setup time, TDI valid before TCK high	10		ns
6	$t_{su(TMSV-TCKH)}$	Setup time, TMS valid before TCK high	6		ns
7	$t_{h(TCKH-TDIV)}$	Hold time, TDI valid after TCK high	4		ns
8	$t_{h(TCKH-TDIV)}$	Hold time, TMS valid after TCK high	4		ns

Table 6-56. Switching Characteristics Over Recommended Operating Conditions for JTAG Test Port (see Figure 6-41)

NO.	PARAMETER		CV_{DD} = 1.05 V CV_{DD} = 1.3 V		UNIT
			MIN	MAX	
1	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid		28	ns

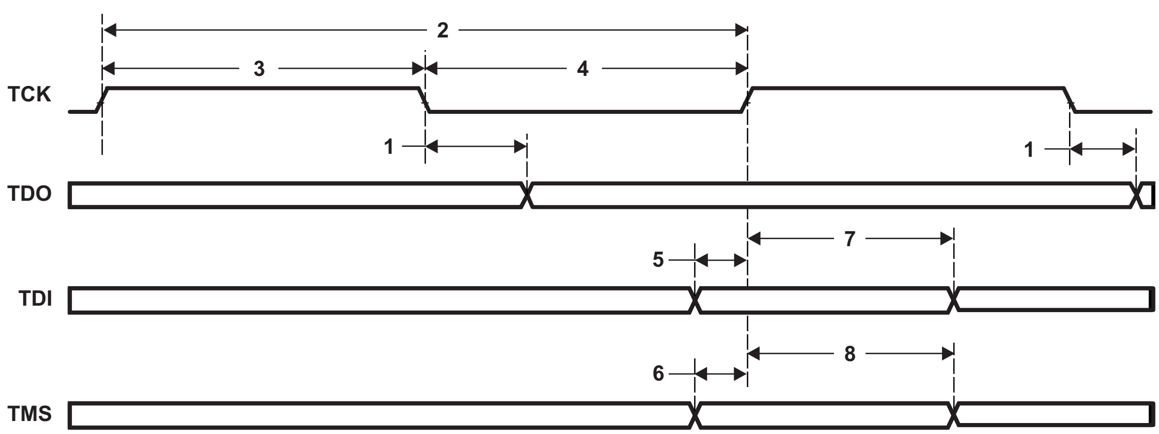


Figure 6-41. JTAG Test-Port Timing

7 Mechanical Packaging and Orderable Information

The following table(s) show the thermal resistance characteristics for the PBGA–ZCH mechanical package.

7.1 Thermal Data for ZCH

Table 7-1. Thermal Resistance Characteristics (PBGA Package) [ZCH]

NO.				°C/W(1)	AIR FLOW (m/s)(2)
1	$R\Theta_{JC}$	Junction-to-case	1S0P	6.74	N/A
2	$R\Theta_{JB}$	Junction-to-board	1S0P	14.5	N/A
			2S2P	13.8	
3	$R\Theta_{JA}$	Junction-to-free air	1S0P	57.0	0.00
			2S2P	33.4	
4	$R\Theta_{JMA}$	Junction-to-moving air			0.50
5					1.00
6					2.00
7					3.00
8	Psi_{JT}	Junction-to-package top		0.09	0.00
9					0.50
10					1.00
11					2.00
12					3.00
13	Psi_{JB}	Junction-to-board		13.7	0.00
14					0.50
15					1.00
16					2.00
17					3.00

(1) These measurements were conducted in a JEDEC defined 2S2P system and will change based on environment as well as application. For more information, see these EIA/JEDEC standards – EIA/JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)* and JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.

(2) m/s = meters per second

7.2 Packaging Information

The following packaging information and addendum reflect the most current data available for the designated device(s). This data is subject to change without notice and without revision of this document.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TMS320VC5505LZCH	OBSOLETE	NFBGA	ZCH	196		TBD	Call TI	Call TI	
TMS320VC5505ZCH	NRND	NFBGA	ZCH	196	184	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
TMX320VC5505AZCH	OBSOLETE	NFBGA	ZCH	196		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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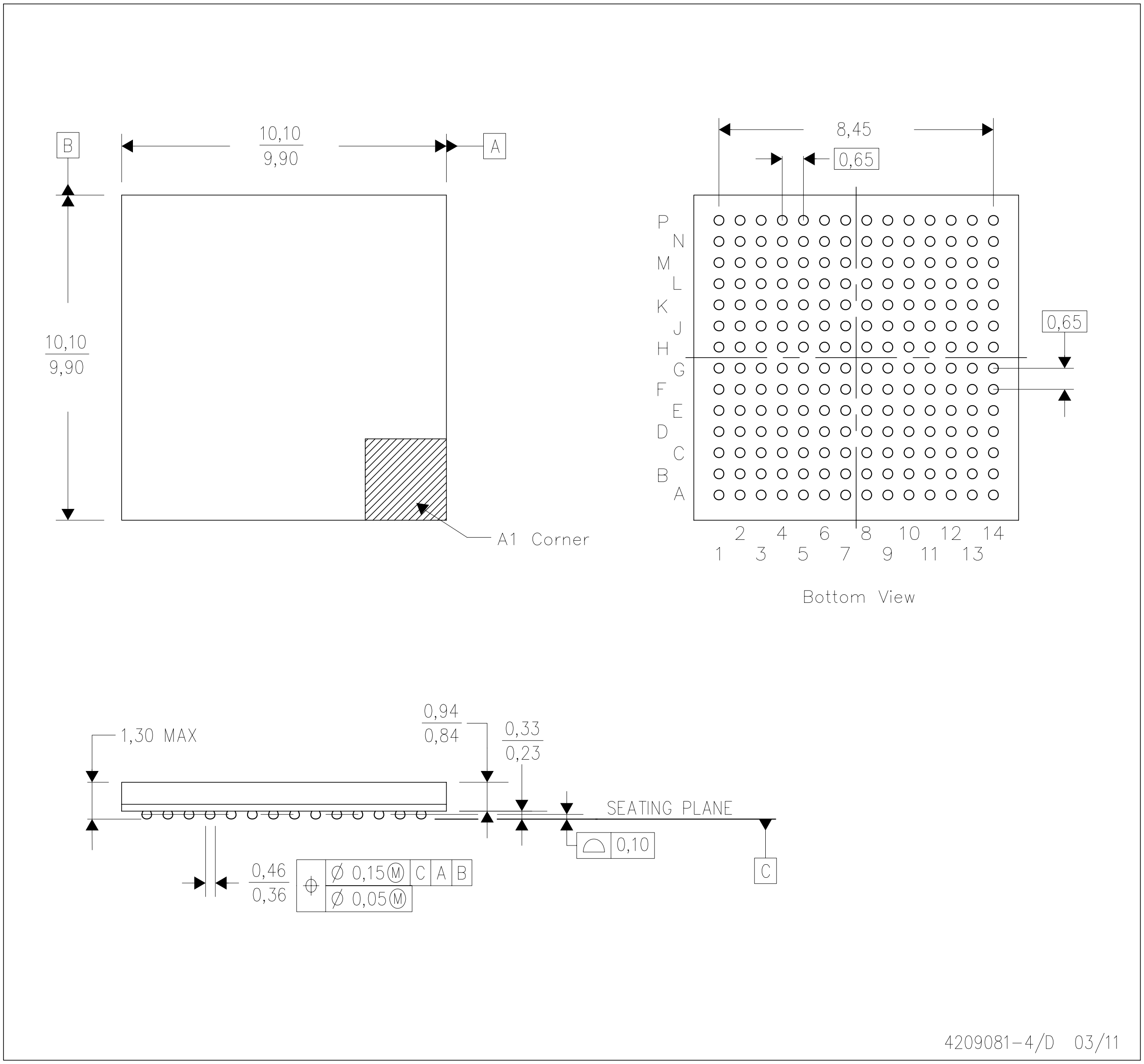
ZCH (S–PBGA–N196) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. nFBGA configuration
D. This is a Pb–free solder ball design.