

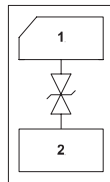
Features

- Ultra small package: 1.0x0.6x0.5mm
- Ultra low capacitance: 0.3pF typical
- Ultra low leakage: nA level
- Low operating voltage: $\pm 5V$
- Low clamping voltage
- 2-pin leadless package
- Complies with following standards:
 - IEC 61000-4-2 (ESD) immunity test
 - Air discharge: $\pm 20kV$
 - Contact discharge: $\pm 15kV$
 - IEC61000-4-5 (Lightning) 4A (8/20 μs)
- RoHS Compliant
- Lead Finish: NiPdAu

Mechanical Characteristics

- Package: DFN1006-2 (0402)
- Lead Finish: Matte Tin
- Case Material: "Green" Molding Compound.
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminal Connections: See Diagram Below

Circuit Diagram



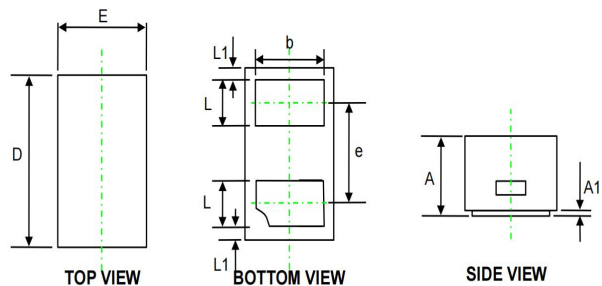
Applications

- Smart phones
- Display Ports
- MDDI Ports
- USB Ports
- Digital Video Interface (DVI)
- PCI Express and Serial SATA Ports

Ordering information

Device	MARKING
RCLAMP0521P	N

DFN1006-2



Symbol	Dimensions in Millimeters (mm)		
	Min.	Typ.	Max.
A	0.44	0.47	0.50
A1	0.00	0.03	0.05
D	0.95	1.00	1.08
E	0.55	0.60	0.68
b	0.40	0.50	0.60
e	-	0.65	-
L	0.20	0.25	0.30
L1	0.05 REF.		

Dimensions in inches and (millimeters)

Absolute Maximum Ratings (Tamb=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20 μs)	Ppk	80	W
Peak Pulse Current (8/20 μs)	Ipp	4	A
ESD per IEC 61000-4-2 (Air)	VESD	± 20	kV
ESD per IEC 61000-4-2 (Contact)		± 15	
Operating Temperature Range	TJ	-55 to +125	°C
Storage Temperature Range	Tstg	-55 to +150	°C

RCLAMP0521P

Electrical Characteristics (TA=25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	VRWM			5	V	
Breakdown Voltage	VBR	5.8	7.5	9	V	IT = 1mA
Reverse Leakage Current	IR			0.08	μA	VRWM = 5V
Clamping Voltage	VC			12	V	I _{PP} = 1A (8 x 20μs pulse)
Clamping Voltage	VC			21	V	I _{PP} = 4A (8 x 20us pulse)
Junction Capacitance	CJ		0.3		pF	VR = 0V, f = 1MHz IO to IO

RATING AND CHARACTERISTIC CURVES (PCLAMP0521P)

Fig1. 8/20 μ s Pulse Waveform

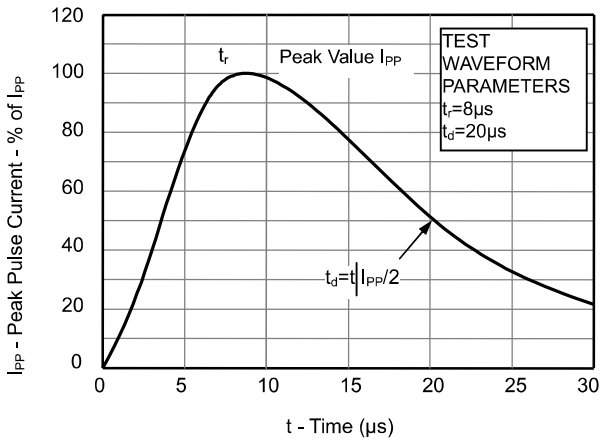


Fig2. ESD Pulse Waveform (according to IEC 61000-4-2)

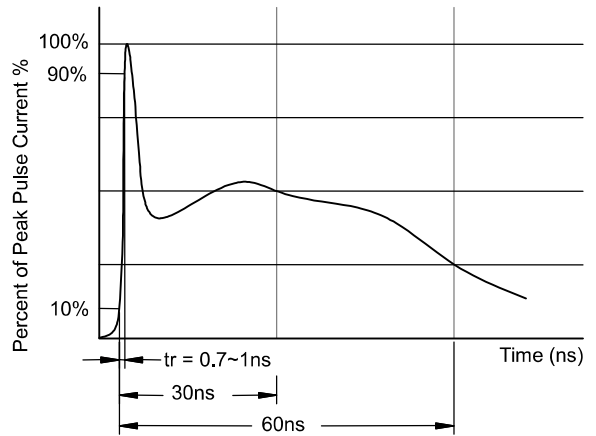


Fig3. Power Derating Curve

