TS31023/223

High Input Voltage Linear Regulator

TRIUNE PRODUCTS

Features

- Wide input supply operating range
  - TS31023 : 5V-16V
  - TS31223 : 5V-36V
- Adjustable output voltage from 1.25V to V_{IN} - $V_{dropout}$
- 60mA output current capability
- Enable control function

Applications

- Set-top Boxes
- Automotive
- Industrial
- Medical
- Energy harvesting systems
- Wireless Power

Description

The TS31x23 high voltage linear regulator consists of a low power amplifier with a high voltage p-channel pass gate.

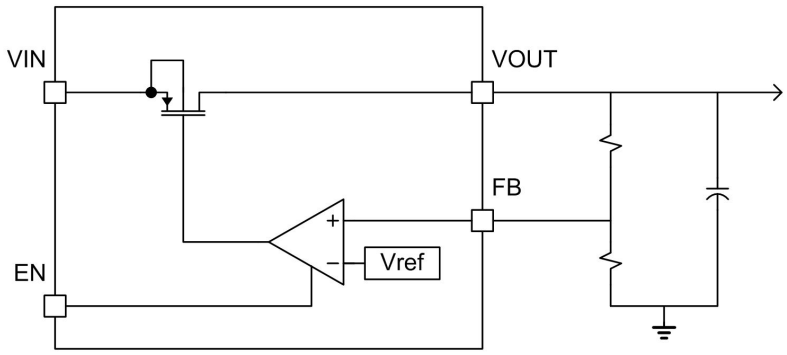
The linear regulator has a wide operating range, and is ideal for systems that may have large voltage transients and require the output load to remain regulated.

An analog current limit is used to limit output current and protect the regulator from external short circuits.

Summary Specification

- Ambient operating temperature 0C to 85C
- Packaged in a 8pin DFN (2x2)

Typical Application Circuit



Pin-out Configuration

Pin #	Pin Symbol	I/O/P	Description
1	GND	P	Ground
2	VOUT	O	Regulated Output Voltage
3	N/C		No Connect
4	N/C		No Connect
5	N/C		No Connect
6	FB	I	Feedback Voltage
7	VIN	P	Input Voltage
8	EN	I	ENABLE Input

Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted(1,2)

		Unit
VIN	-0.3 to 18 (TS31023) -0.3 to 40 (TS31223)	V
VOUT	-0.3 to 18 (TS31023) -0.3 to 40 (TS31223)	V
EN, FB	-0.3 to 6.0	V
Electrostatic Discharge – Human Body Model	2	kV
Maximum junction temperature, TJ	150	^{O}C
Storage temperature range, Tstg	-65 to 150	^{O}C
Lead Temperature (soldering, 10 seconds)	260	^{O}C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

Note 2: All voltage values are with respect to network ground terminal.

Thermal Characteristics

Package DFN	θ_{JA} (^{O}C/W) (See Note 4)	θ_{JC} (^{O}C/W) (See Note 5)
8 pin	73.1	10.7

Note 4: This assumes a FR4 board only.
Note 5: This assumes a 1oz. Copper JEDEC standard board with thermal vias. See Exposed Pad section and application note for more information.

Recommended Operating Conditions

Parameter	Min	Max	Units
Unregulated Supply Input Voltage (VIN)	5	16 (TS31023) 36 (TS31223)	V
Enable Input (EN)	0	5	V
Regulated Supply Output Voltage (VOUT)	1.25	VIN - $V_{dropout}$	V
Operating Junction Temperature, T_J	-40	125	^{O}C

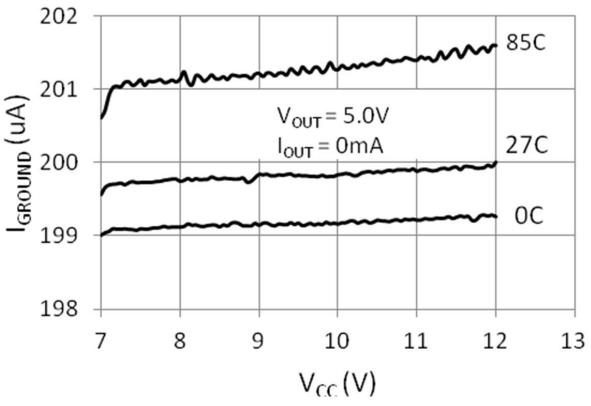
Electrical Characteristics (T=25^{O}C unless otherwise specified)

Electrical characteristics, VIN = 12V, T_J = 25C, unless otherwise noted

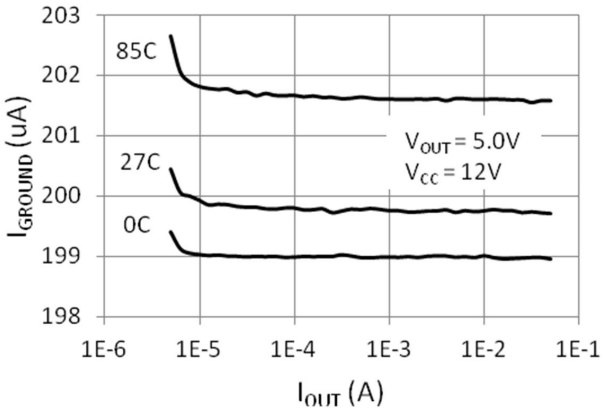
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Supply Voltage	VIN	TS31023	5		16	V
		TS31223	5		36	V
Output Voltage	VOUT		1.25		VIN - $V_{dropout}$	V
Feedback Voltage	FB	V_{IN} = 12V	1.10	1.20	1.30	V
Output Bypass Capacitor	C_{OUT}		1	2.2	4.7	uF
Disabled Current	$I_{off(VIN)}$	EN=0V, V_{IN}=12V		1		uA
Quiescent Current	$I_{qq(VIN)}$	EN=5V, I_{OUT} = 0		220		uA
Load Capability	I_{OUT}				60	mA
DC Line Regulation (TS31023)	V_{Line}	V_{IN} = 5.5V to 16V, V_{OUT}=5.0V, I_{OUT} = 5mA		0.1	0.6	%
DC Line Regulation (TS31223)		V_{IN} = 5.5V to 36V, V_{OUT}=5.0V, I_{OUT} = 5mA		0.1	0.6	%
DC Load Regulation (TS31023)	V_{Load}	V_{IN} = 12V, V_{OUT}=5.0V, I_{OUT} = 1mA to 60mA		0.02	0.35	%
		V_{IN} = 6V, Vout=5.0V, I_{OUT} = 1mA to 60mA		0.02	0.15	%
Current Limit	I_{Limit}	V_{IN} =12V		100		mA

Typical Performance Characteristics

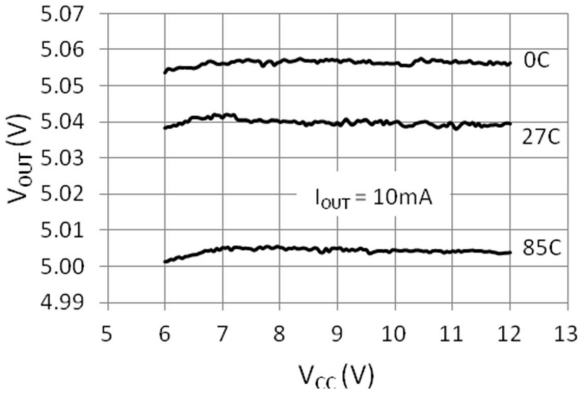
I_{qq} Performance vs. Supply Voltage



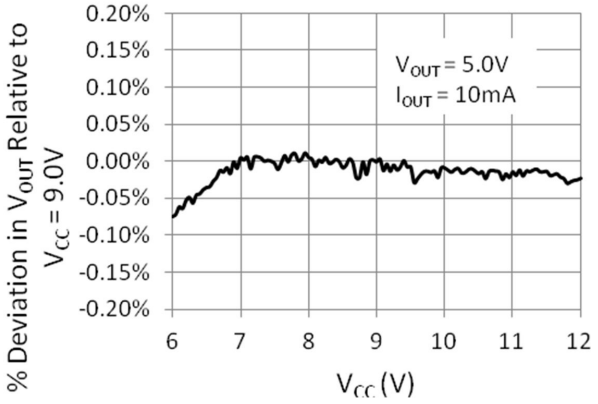
I_{qq} Performance vs. Load Current



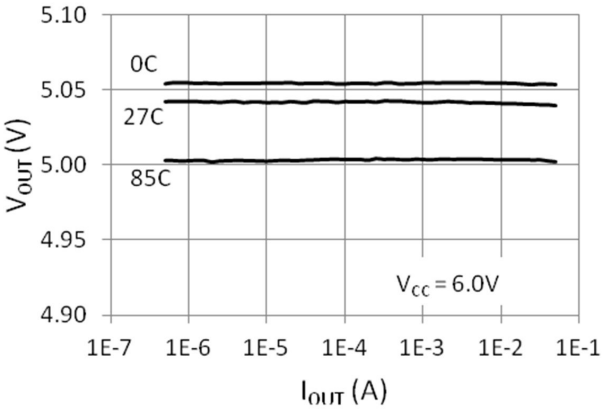
V_{OUT} Performance vs. V_{CC}



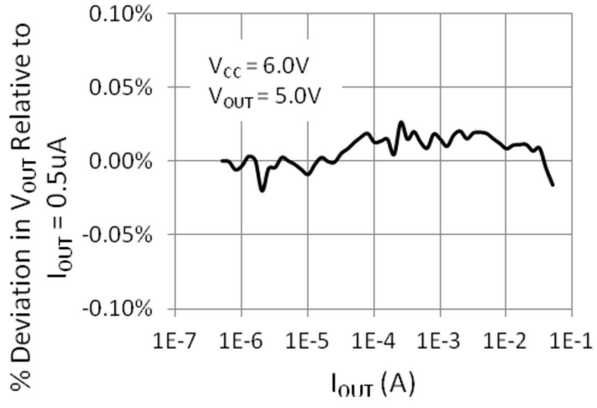
Line Regulation Performance



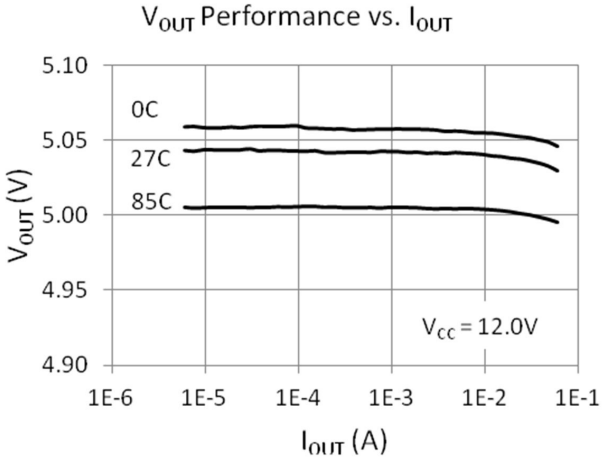
V_{OUT} Performance vs. I_{OUT}

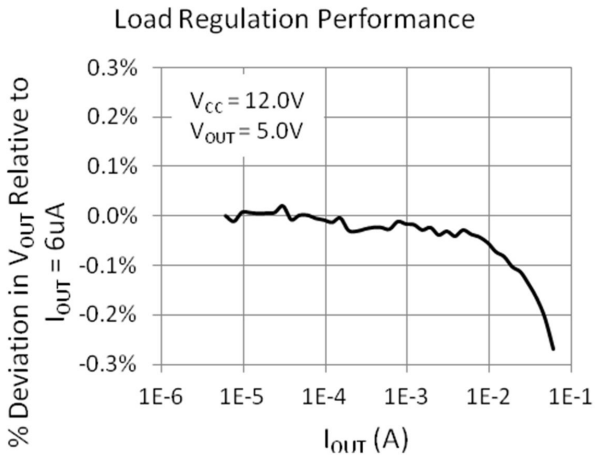


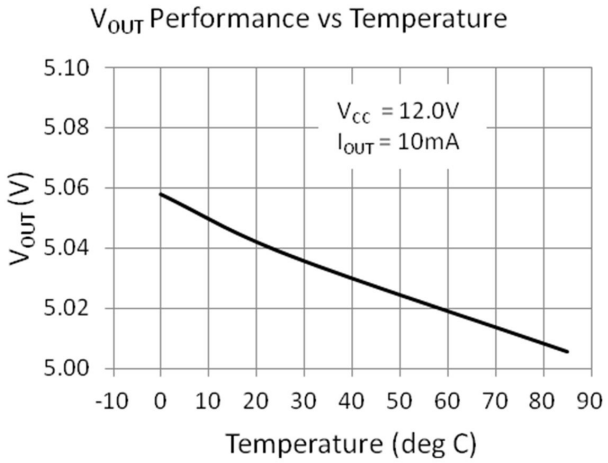
Load Regulation Performance

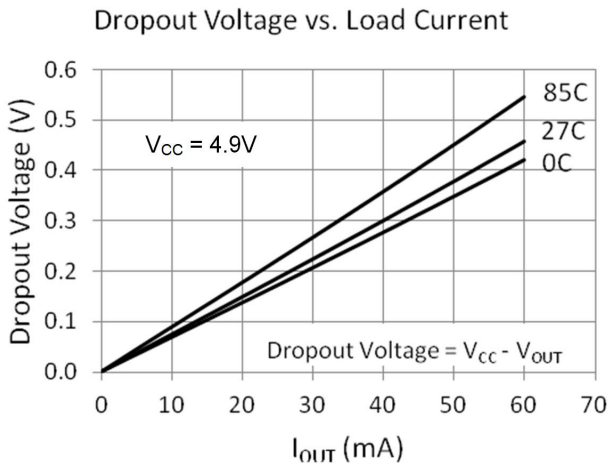


Typical Performance Characteristics continued

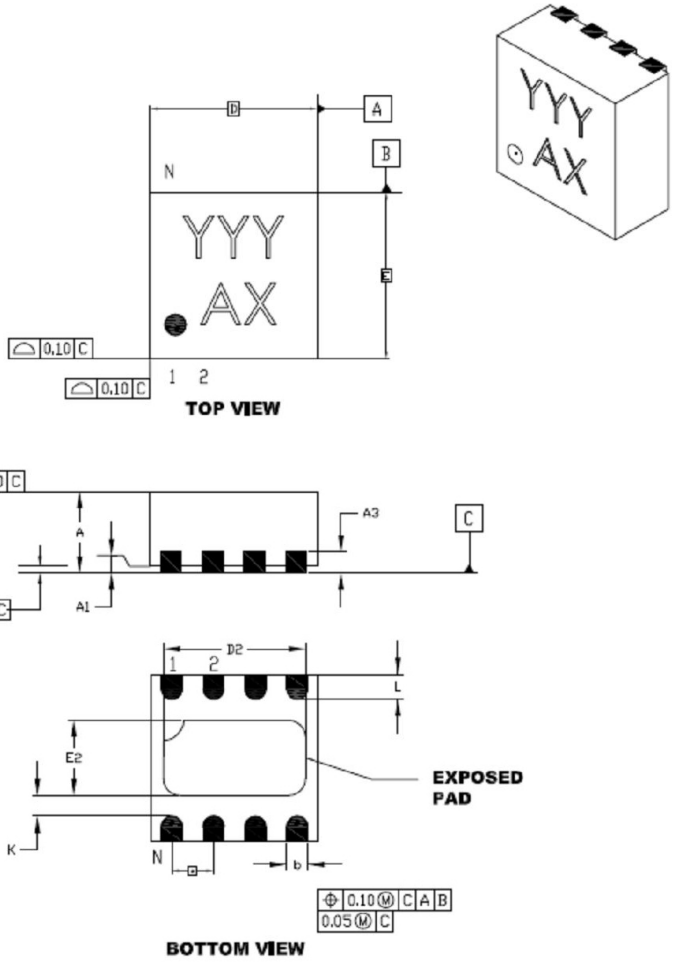






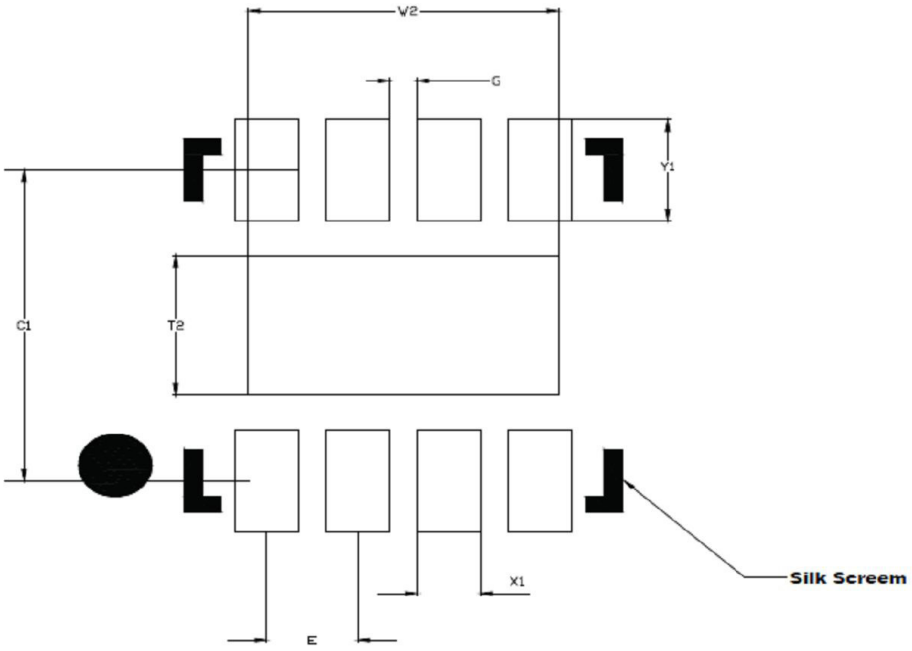


Package Mechanical Drawings (all dimensions in mm)



Units		Millimeters		
Dimensions Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Width	E2	0.75	0.90	1.00
Overall Width	E		2.00 BSC	
Exposed Pad Length	D2	1.55	1.70	1.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.20	0.30	0.40
Contact-to-Exposed Pad	K	0.20	-	-

Recommended PCB Land Pattern



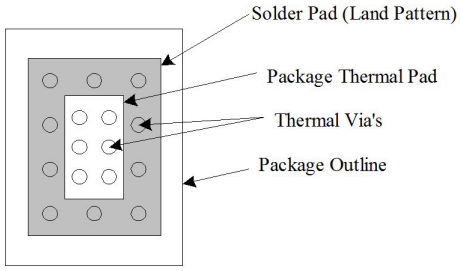
RECOMMENDED LAND PATTERN

Units		Millimeters		
Dimensions Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2	–	–	1.70
Optional Center Pad Length	T2	–	–	0.90
Contact Pad Spacing	C1	–	2.00	–
Contact Pad Width (X8)	X1	–	–	0.35
Contact Pad Length (X8)	Y1	–	–	0.65
Distance Between Pads	G	0.15	–	–

Application Using A Multi-Layer PCB

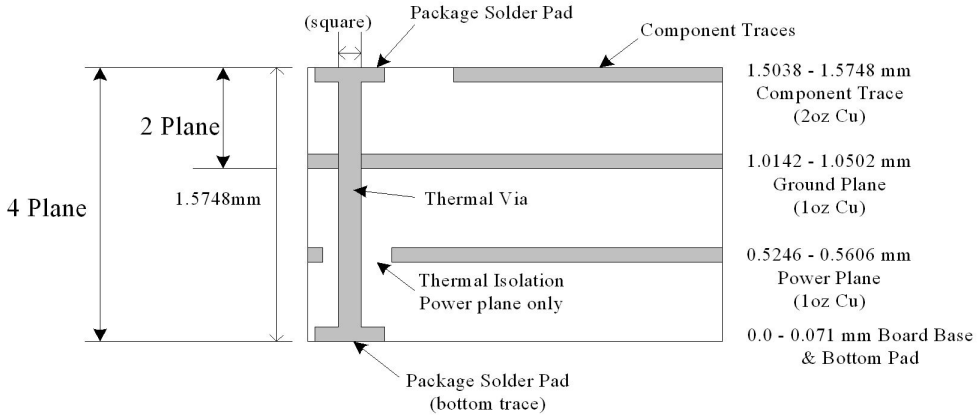
To maximize the efficiency of this package for application on a single layer or multi-layer PCB, certain guidelines must be followed when laying out this part on the PCB.

The following are guidelines for mounting the exposed pad IC on a Multi-Layer PCB with ground a plane.



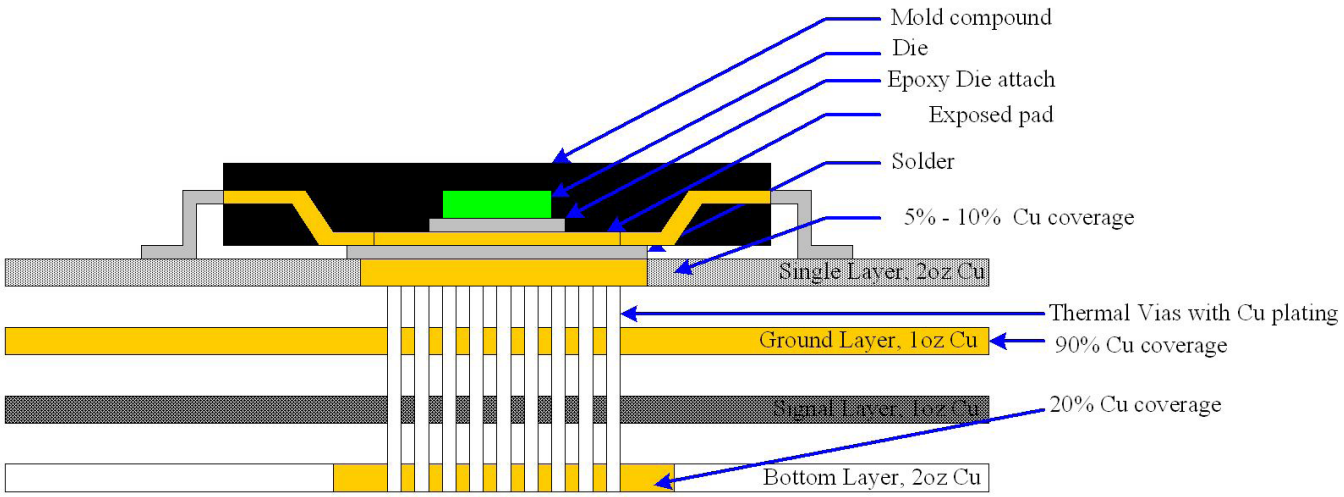
Package and PCB Land Configuration
For a Multi-Layer PCB

JEDEC standard FR4 PCB Cross-section:



Multi-Layer Board (Cross-sectional View)

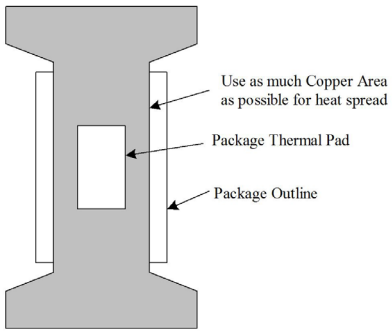
In a multi-layer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors, including die area, number of thermal vias, thickness of copper, etc.



Note: NOT to Scale

The above drawing is a representation of how the heat can be conducted away from the die using an exposed pad package. Each application will have different requirements and limitations and therefore the user should use sufficient copper to dissipate the power in the system. The output current rating for the linear regulators may have to be de-rated for ambient temperatures above 85C. The de-rate value will depend on calculated worst case power dissipation and the thermal management implementation in the application.

Application Using A Single Layer PCB



Layout recommendations for a Single Layer PCB: utilize as much Copper Area for Power Management. In a single layer board application the thermal pad is attached to a heat spreader (copper areas) by using low thermal impedance attachment method (solder paste or thermal conductive epoxy).

In both of the methods mentioned above it is advisable to use as much copper traces as possible to dissipate the heat.

Important:
If the attachment method is NOT implemented correctly, the functionality of the product is not guaranteed. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.

IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (Tsmax to Tp)	3 ^{O}C/second max.	3 ^{O}C/second max.
Preheat - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (Ts_{min} to Ts_{max}) (ts)	 100 ^{O}C 150 ^{O}C 60 - 120 seconds	 150 ^{O}C 200 ^{O}C 60 - 180 seconds
Time maintained above - Temperature (T_L) - Time (t_L)	 183 ^{O}C 60 - 150 seconds	 217 ^{O}C 60 - 150 seconds
Peak Temperature (Tp)	see table 4.1	see table 4.2
Time within 5 ^{O}C of actual Peak Temperature (tp)	10 - 30 seconds	20 - 40 seconds
Ramp-down Rate	6 ^{O}C/second max.	6 ^{O}C/second max.
Time 25 ^{O}C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5 ^{O}C of actual peak temperature (tp) specified for the reflow profiles is a "supplier" minimum and "user" maximum.

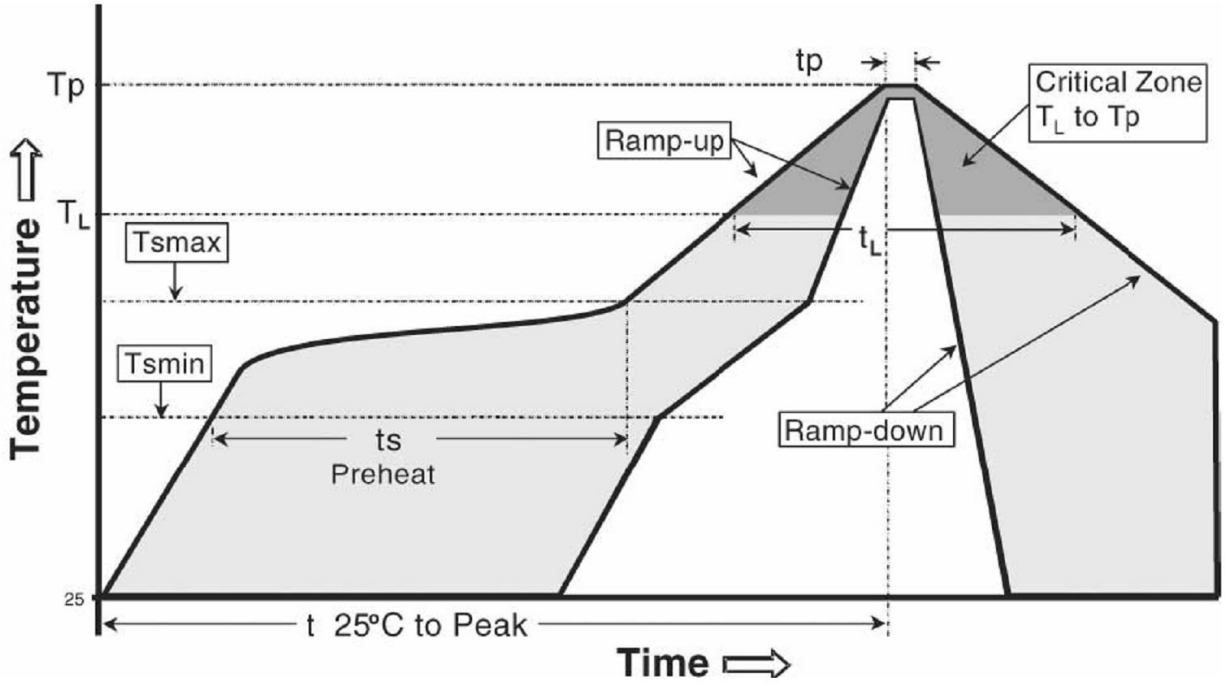


Table 4-1 SnPb Eutectic Process - Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5mm	240 +0/-5 °C	225 +0/-5 °C
≥ 2.5mm	225 +0/-5 °C	225 +0/-5 °C

Table 4-2 Pb-free Process - Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6mm	260 °C*	260 °C*	260 °C*
1.6mm - 2.5mm	260 °C*	250 °C*	245 °C*
> 2.5mm	250 °C*	245 °C*	245 °C*
* Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classified temperature at the rated MSL level			

Note 1: Package volume excludes external terminals (balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 2: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mas of SMD packages may still exist.

Note 3: Components intended for use in a "lead-free" assembly process shall be evaluated using the "lead-free" peak temperature and profiles defined in Tables 4-1, 4.2 and 5-2 whether or not lead free.

RoHS and Reach Compliance

Triune Systems is fully committed to environmental quality. All Triune Systems materials and suppliers are fully compliant with RoHS (European Union Directive 2011/65/EU), REACH SVHC Chemical Restrictions (EC 1907/2006), IPC-1752 Level 3 materials declarations, and their subsequent amendments. Triune Systems maintains certified laboratory reports for all product materials, from all suppliers, which show full compliance to restrictions on the following:

- Cadmium (Cd)
- Chlorofluorocarbons (CFCs)
- Chlorinate Hydrocarbons (CHCs)
- Halons
- Hexavalent Chromium (CrVI)
- Hydrobromofluorocarbons (HBFCs)
- Hydrochlorofluorocarbons (HCFCs)
- Lead (Pb)
- Mercury (Hg)
- Perfluorocarbons (PFCs)
- Polybrominated biphenyls (PBB)
- Polybrominated Diphenyl Ethers (PBDEs)

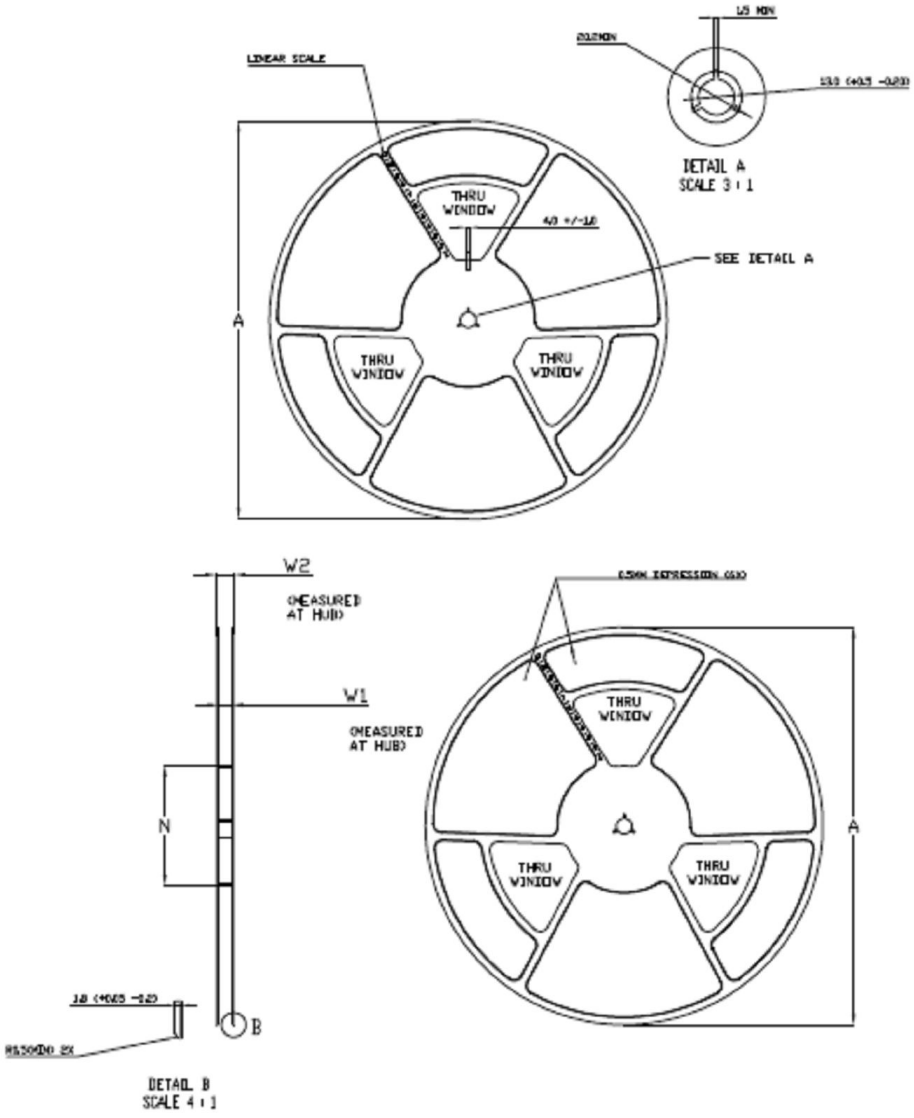
Ordering Information

Part Number:

TS31023-QFNR

TS31223-QFNR

Reel Dimensions (13 inch)

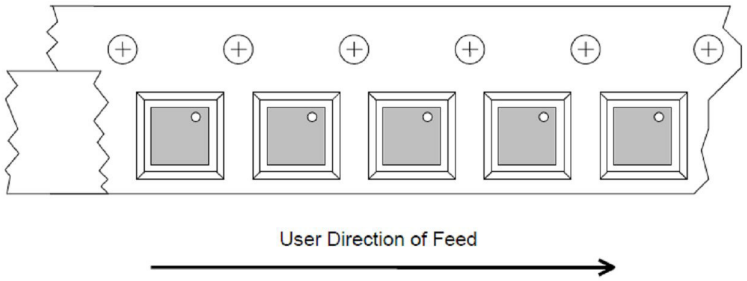


Product Specifications

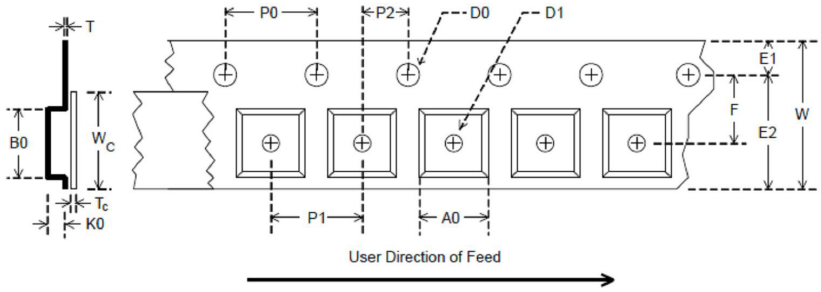
Tape Width	A (MAX)	N (MIN)	W1	W2
8mm	330	100	8.4	14.4
12mm	330	100	12.4	18.4
16mm	330	100	16.4	22.4

Carrier Tape Specification

All DFN and QFN packages will be oriented so that the index package locations will be on the upper right corner of the sprocket side of the carrier tape.



All carrier tape used for packaging Triune Components will be specifically formulated to provide protection from physical and electro-static discharge (ESD) damage during shipping and storage. Embossed carrier tape must be EIA standard-481-1 compliant and meet the mechanical characteristics shown in Table 3.



Dimensions are in millimeters

Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
2x2mm DFN	2.3	2.3	8.0 +/- 0.2	1.50 +/- 0.10	1.10 +/- 0.10	1.75 +/- 0.10	6.25 min	3.5 +/- 0.05	4	4	1.5	0.25 +/- 0.05	8	0.21 - 0.35
3x3mm QFN	3.3	3.3	12	1.50 +/- 0.10	1.10 +/- 0.10			3.5 +/- 0.05	8	8	1.1		4.5	0.21 - 0.35
4x4mm QFN	4.35	4.35	12	1.50 +/- 0.10	1.10 +/- 0.10			3.5 +/- 0.05	8	8	1.1		5.4	0.21 - 0.35
5x5mm QFN	5.25	5.25	12	1.50 +/- 0.10	1.10 +/- 0.10			3.5 +/- 0.05	8	8	1.1		9.2	0.21 - 0.35
6x6mm QFN	6.3 +/- 0.10	6.3 +/- 0.10	16 +/- 0.30	1.50 +/- 0.10	1.50 +/- 0.10	1.75 +/- 0.10	14.25	7.5 +/- 0.10	12	2	1.1	0.30 +/- 0.05	13.3	0.21 - 0.35

Contact Information

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