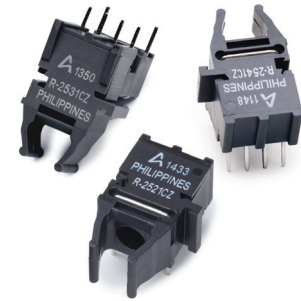


AFBR-25x1CZ

DC...5 Megabaud Versatile Link Fiber Optic Receiver
for 1mm POF and 200µm PCS



Data Sheet



Description

The AFBR-25x1CZ receiver consists of an IC with an integrated photodiode providing a TTL logic families compatible output. In combination with the Avago Technologies AFBR-15x9Z or AFBR-16x9Z transmitter any type of signal from DC up to 5MBd at distances up to 50 meters with 1mm 0.5NA POF and 500 meters with 200µm 0.37NA PCS is supported.

The receiver is a 4-pin device, packed in Versatile Link housing. Versatile Link components can be interlocked (N-plexed together) to minimize space and to provide dual connections with the duplex connectors. Various simplex and duplex connectors, as well as POF cables are available for Versatile Link components.

AFBR-25x1CZ devices have inverted output signals means that light_on will lead to Data_out low.

Available options

| | |
|----------------------|-------------|
| Horizontal Package | AFBR-2521CZ |
| Vertical Package | AFBR-2531CZ |
| Tilted (30°) Package | AFBR-2541CZ |

Features

- RoHS-compliant
- Data transmission at signal rates from DC up to 5MBd
- Receiver: integrated PIN diode and digitalizing IC with TTL output logic
- Power-on reset (POR)
- Up to 50 meter distance with 1mm Plastic Optical Fiber (POF); up to 500 meter distance with 200µm Polymer Cladding Silica (PCS) Fiber
- Operating temperature range of -40 °C to +85 °C
- Compatible with Avago Technologies' Versatile Link family of connectors, for easy termination of fiber

Applications

- Optical Receiver for 5MBd systems and below
- Industrial control and factory automation
- Extension of RS-232 and RS-485
- High voltage insulation
- Elimination of ground loops
- Reduces voltage transient susceptibility
- Drivers and Inverters

Application Literature

Application Note 1035 (Versatile Link) - AV02-0730EN

Package and Handling Information

The compact Versatile Link package is made of a flame retardant material and uses the same pad layout as a standard, eight-pin dual-in-line package. Horizontal, Vertical, and Tilted (30°) packages are available. These low profile Versatile Link packages are stackable and are enclosed to provide a dust-resistant seal. Snap action simplex, simplex latching, duplex, and duplex latching connectors are offered with simplex or duplex cables.

Package Housing Color

Versatile Link components and simplex connectors are color coded to eliminate confusion when making connections. Receiver packages are black and transmitters are in grey color respectively.

Package Orientation

Performance and pinouts for the horizontal, vertical, and tilted (30°) packages are identical. To provide additional attachment support for the vertical Versatile Link housing the designer has the option of using a self-tapping screw through a printed circuit board into a mounting hole at the bottom of the package. For most applications this is not necessary.

Handling

Versatile Link components are auto-insertable. When wave soldering is performed with Versatile Link components, the optical port plug should be left in to prevent contamination of the port. Do not use reflow solder processes (i.e., infrared reflow or vapor-phase reflow). Non-halogenated water soluble fluxes (i.e., 0% chloride), not rosin based fluxes, are recommended for use with Versatile Link components.

Versatile Link components are moisture sensitive devices and are shipped in a moisture sealed bag. If the components are exposed to air for an extended period of time, they may require a baking step before the soldering process. Refer to the special labeling on the shipping tube for details.

Recommended chemicals for Cleaning/Degreasing

Alcohols: methyl, isopropyl, isobutyl. Aliphatics: hexane, heptanes. Other: soap solution, naphtha.

Do not use partially halogenated hydrocarbons such as 1,1,1 trichloroethane, ketones such as MEK, acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride, or N-methylpyrrolidone. Avago Technologies does not recommend the use of cleaners that use halogenated hydrocarbons because of their potential environmental harm.

Interlocked (Stacked) Assemblies (refer to Figure 1)

Horizontal packages may be stacked by placing units with pins facing upward. Initially engage the interlocking mechanism by sliding the L bracket body from above into the L slot body of the lower package. Use a straight edge, such as a ruler, to bring all stacked units into uniform alignment. This technique prevents potential harm that could occur to fingers and hands of assemblers from the package pins. Stacked horizontal packages can be disengaged if necessary. Repeated stacking and unstacking causes no damage to individual units.

To stack vertical packages, hold one unit in each hand, with the pins facing away and the optical ports on the bottom. Slide the L bracket unit into the L slot unit. The straight edge used for horizontal package alignment is not needed.

Stacking Horizontal Modules

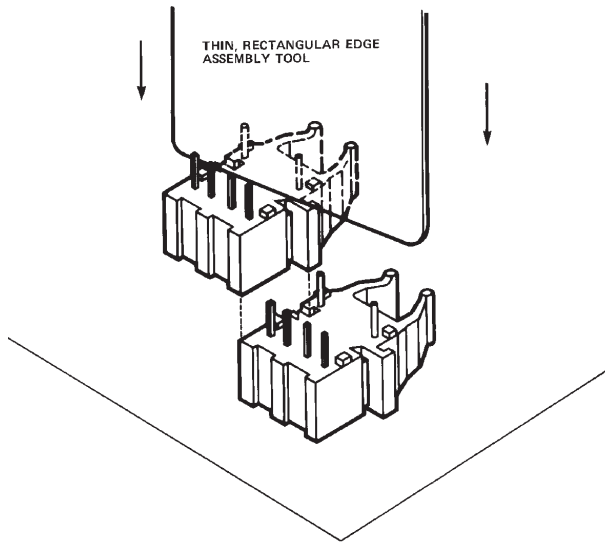


Figure 1a. Interlocked (stacked) Horizontal packages

Stacking Vertical Modules

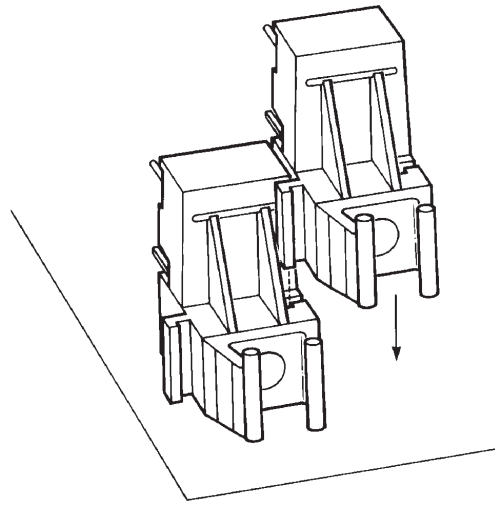


Figure 1b. Interlocked (stacked) Vertical packages

Tilted (30°) Module

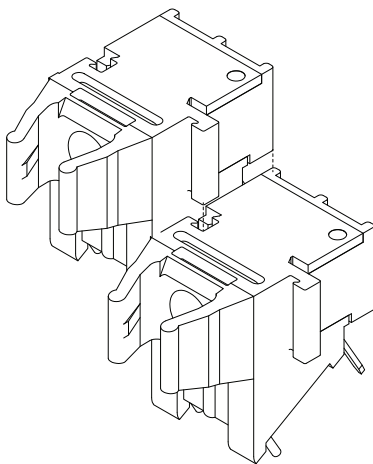


Figure 1c. Interlocked (stacked) Tilted (30°) packages

Mechanical Dimensions

Horizontal Module

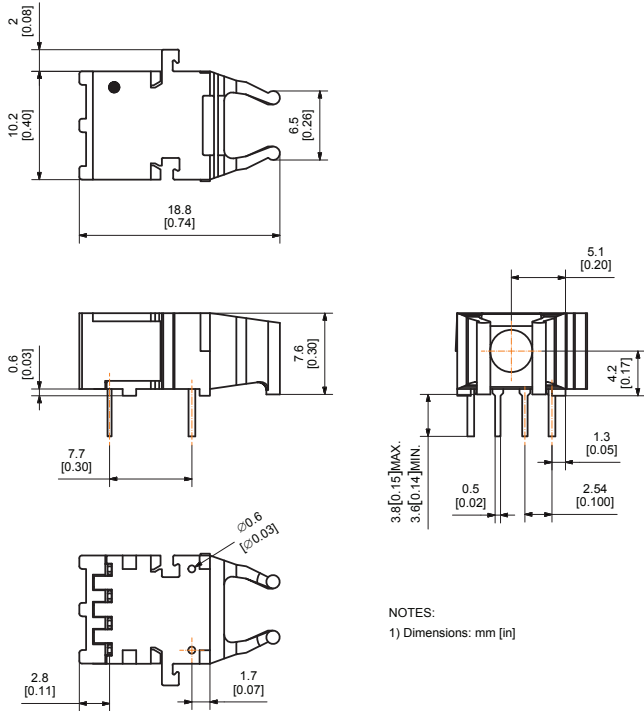


Figure 2a. Mechanical Dimensions - Horizontal packages

Vertical Module

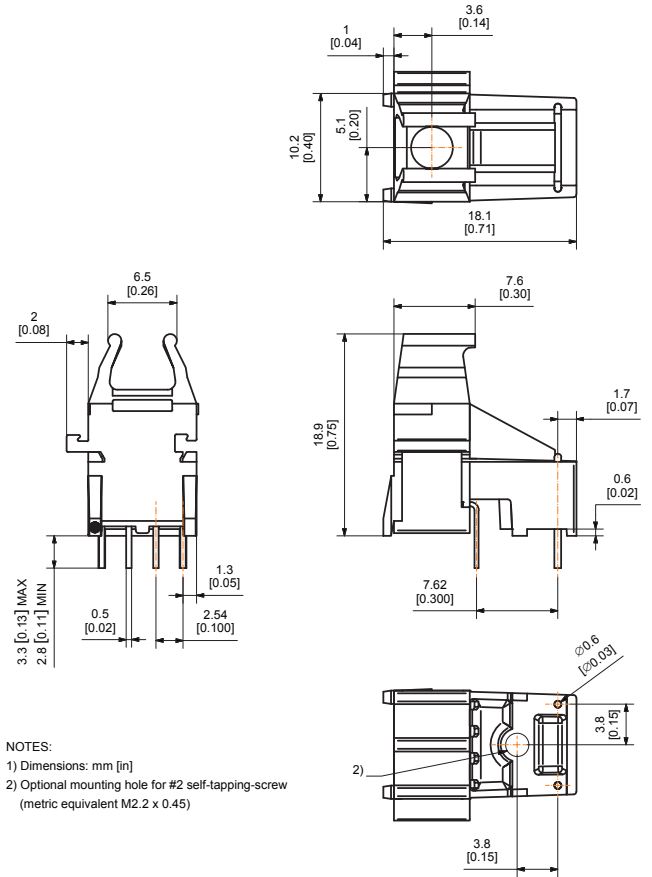


Figure 2b. Mechanical Dimensions - Vertical packages

Tilted (30°) Module

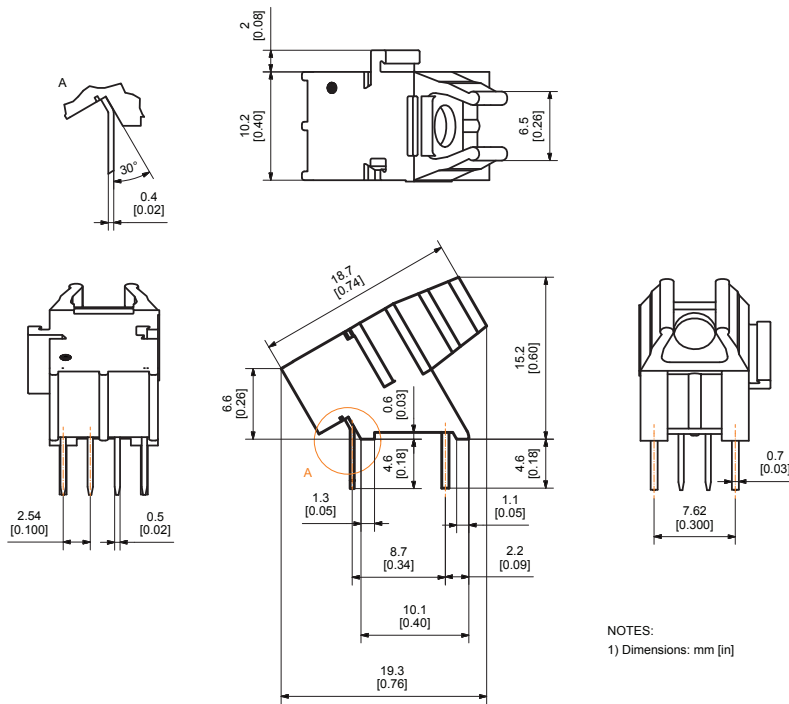
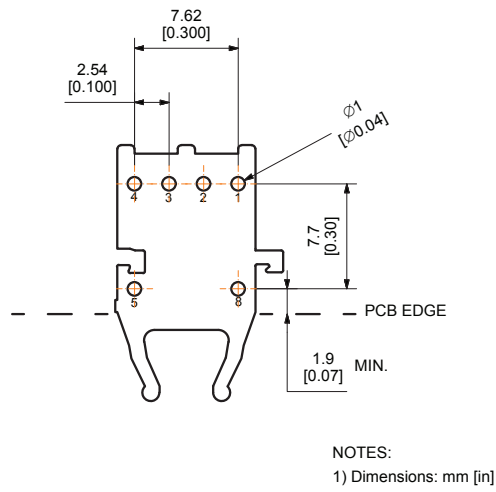


Figure 2c. Mechanical Dimensions - Tilted (30°) packages

Versatile Link Printed Board Layout Dimensions

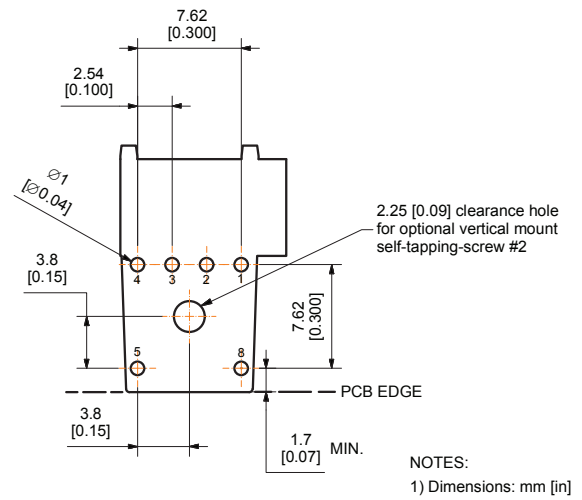
Horizontal Module



Footprint - TOP VIEW

Figure 3a. PCB Dimensions - Horizontal packages

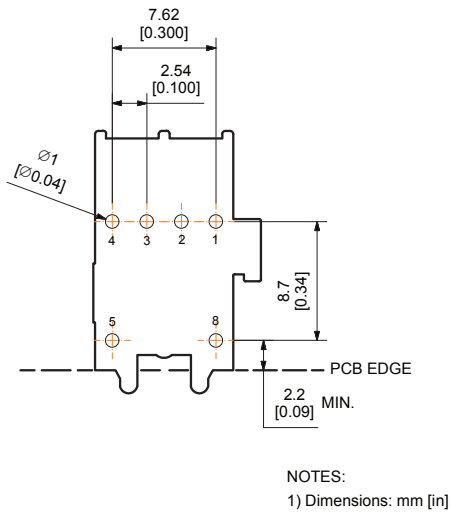
Vertical Module



Footprint - TOP VIEW

Figure 3b. PCB Dimensions - Vertical packages

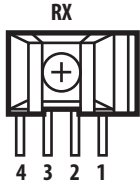
Tilted (30°) Module



Footprint - TOP VIEW

Figure 3c. PCB Dimensions - Tilted (30°) packages

Pin Description Receiver



Fiber port facing front, pins downward, 1 = Rightmost pin to 4 = Leftmost pin

| Pin | Name | Function/Description | Notes |
|-----|-----------------|---|-------|
| 1 | Data Out | Data Output | 1, 2 |
| 2 | V _{EE} | Ground | |
| 3 | V _{CC} | Power Supply 3.3V ± 5% or 5V ± 5% | |
| 4 | Pin | No function, physical pin is available, recommended to signal GND | 3 |
| 5 | Housing Pin | Physical pin is available, recommended to chassis GND | 4 |
| 8 | Housing Pin | Physical pin is available, recommended to chassis GND | 4 |

Notes:

1. TTL compatible data output
2. Light on at the receiver input will lead to a “low” output signal and light off to a “high” output signal.
3. It is recommended to connect this pin to signal GND
4. Pin 5 and 8 are for mounting and retaining purposes and should be connected to chassis GND.

Regulatory Compliance

| Feature | Test Method | Performance |
|---|-------------------------|---------------|
| Electrostatic Discharge (ESD) to the Electrical Pins Human Body Model | MIL-STD-883 Method 3015 | Min +/- 2000V |
| Eye Safety | IEC 60825-1,2 ,Class 1 | |

Specified Link Performance, T_A = -40 °C to +85 °C, 5 MBd

| Parameter | Min. | Max. | Unit | Condition | Notes |
|------------------------------|------|------|--------|----------------|-------|
| Link Distance with POF cable | 0.1 | 50 | meters | -40°C to +85°C | 5, 7 |
| Link Distance with PCS | 0.1 | 500 | meters | -40°C to +85°C | 6, 7 |

Notes:

5. HFBR-R/EXXYYYZ is the part number for 1mm POF. Worst case attenuation used (0.27dB/m for standard loss POF cable from -40°C to +85°C at 660nm).
6. PCS, worst case attenuation (12dB/km from -40°C to +85°C at 650nm)
7. The optical link performance is guaranteed only with transmitters AFBR-15x9Z (>20mA forward current) or AFBR-16x9Z

Recommended Application Circuit

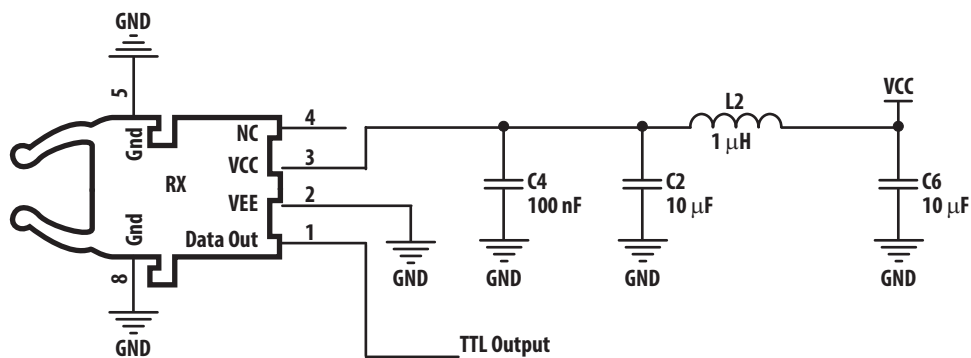


Figure 4. Recommended Application Circuit

Absolute Maximum Ratings

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---------------------|-----------------|------|------|------|------|-------|
| Storage Temperature | T _S | -40 | | 95 | °C | 1 |
| Ambient Temperature | T _C | -40 | | 85 | °C | 1 |
| Relative Humidity | RH | 0 | | 85 | % | 1 |
| Supply Voltage | V _{CC} | -0.5 | | 6 | V | 1 |
| Data Output Current | I _O | | | 10 | mA | 1 |
| Data Rate | | DC | | 5 | MBd | |

Notes:

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur if these limits are exceeded for other than a short period of time.

Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|----------------|-----------------|-------|------|-------|------|-------|
| Ambient Temp | T _A | -40 | 25 | 85 | °C | 2 |
| Supply Voltage | V _{CC} | 3.135 | 3.3 | 3.465 | V | 2 |
| | | 4.75 | 5 | 5.25 | V | 2 |

Notes:

2. Recommended operating conditions are those values outside of which functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time. See Reliability Data Sheet for specific reliability performance.

Process Compatibility

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|--------------------|-------------------|------|------|------|------|---------|
| Solder Environment | T _{SOLD} | | | 260 | °C | 3, 5, 6 |
| | t _{SOLD} | | | 10 | sec | 4, 5, 6 |

Notes:

3. Maximum temperature refers to peak temperature.
4. Maximum time refers to time spent at peak temperature.
5. Solder surface to be at least 1.6mm below lead frame stops.
6. Product is moisture sensitive level 3.

AFBR-25x1CZ Receiver

The AFBR-25x1CZ receiver consists of a digitalizing IC with integrated photodiode to produce an output level that is compatible with TTL logic. The integrated photodiode and the following amplifier use a fully differential approach with an active and a passive area for an improved EMI performance. Within the specified ranges the AFBR-25x1CZ devices support a BER <10E-9.

Receiver Electrical Characteristics

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 3.3\text{ V} \pm 5\%$ or $5\text{ V} \pm 5\%$)

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|-----------------------------|-----------------------|------|---------|--------------|---------------|------------|
| Supply Current | I_{CC} | | 6 | 10 | mA | 1 |
| Data Output Voltage – Low | V_{OL} | -0.3 | | 0.4 | V | 2 |
| Data Output Voltage – High | V_{OH} | 2.5 | | $V_{CC}+0.3$ | V | 2 |
| Rise Time (10%–90%) | t_R | | | 10 | ns | 3 |
| Fall Time (90%–10%) | t_F | | | 10 | ns | 3 |
| Pulse Width Distortion | PWD | -30 | | 30 | ns | 3, 4, 5, 6 |
| Propagation Delay | t_D | | | 60 | ns | 3, 4 |
| Propagation Skew | t_{skew} | | | 20 | ns | 3, 4, 7 |
| Vcc level to deactivate POR | V_{POR_DEACT} | | 2.8 | | V | 1, 8 |
| Vcc level to activate POR | V_{POR_ACT} | | 2.6 | | V | 1, 8 |
| POR deactivate delay time | $t_{POR_DEACT_DEL}$ | | 100 | | μs | 1, 8 |

Receiver Optical Characteristics

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 3.3\text{ V} \pm 5\%$ or $5\text{ V} \pm 5\%$)

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|-----------------------------------|---------------|-----|---------|-----|------|-------|
| Input Optical Power POF (Peak) | P_{IN} | -24 | | 1 | dBm | 9 |
| Input Optical Power PCS (Peak) | P_{IN} | -26 | | -2 | dBm | 10 |
| Input Optical Power Off-State POF | P_{IN_Off} | -40 | | | dBm | 9 |
| Input Optical Power Off-State PCS | P_{IN_Off} | -43 | | | dBm | 10 |
| Optical Spectrum Range | λ | 630 | | 685 | nm | |

Notes:

1. Typical values measured at 25°C and 5V
2. Standard TTL output.
3. Measured with $R_L = 1\text{ M}\Omega$ and $C_L = 20\text{ pF}$
4. Guaranteed only if optical input signal is generated by AFBR-15x9Z or AFBR-16x9Z, with ideal alignment to the photodiode using a 1mm POF (NA=0.5).
5. Optical input of 5MBaud PRBS-7 pattern and 50 % duty cycle. Input rise time (10%-90%) $\leq 20\text{ ns}$, Input fall time (90%-10%) $\leq 20\text{ ns}$
6. Pulse width is measured at 50% threshold using a rising edge trigger and PRBS-7 pattern.
7. Only valid for same input signal characteristics and environmental conditions. Optical input power has to be $\geq -21\text{ dBm}$
8. Power-on reset (POR) is active below V_{POR_DEACT} . Once V_{POR_DEACT} is reached the POR remains active for $t_{POR_DEACT_DEL}$. During power down POR starts at V_{POR_ACT} . Refer to figure 5 (next page).
9. Measured at the end of a 0.5m POF (1mm 0.5 NA) with a large area optical detector
10. Measured at the end of a 0.5m PCS (200 μm , 0.37 NA) with a large area optical detector

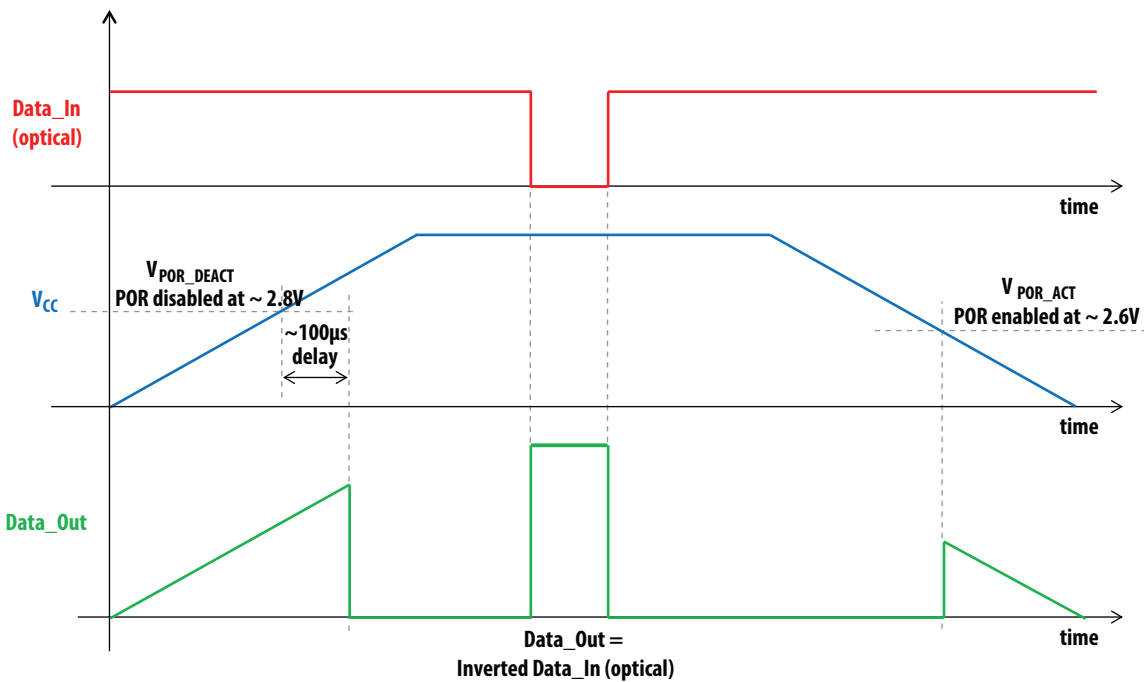


Figure 5. Typical functionality of Power-on reset (POR)

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