

- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 6-pF Channel Capacitance during Disconnect
- 100- μ A Supply Current in Disconnect Mode
- Meets SCSI Hot Plugging
- -400-mA Sourcing Current for Termination
- +400-mA Sinking Current for Active Negation Drivers
- Logic Command Disconnects all Termination Lines
- Trimmed Termination Current to 3%
- Trimmed Impedance to 3%
- Negative Clamping on all Signal Lines
- Current Limit and Thermal Shutdown Protection

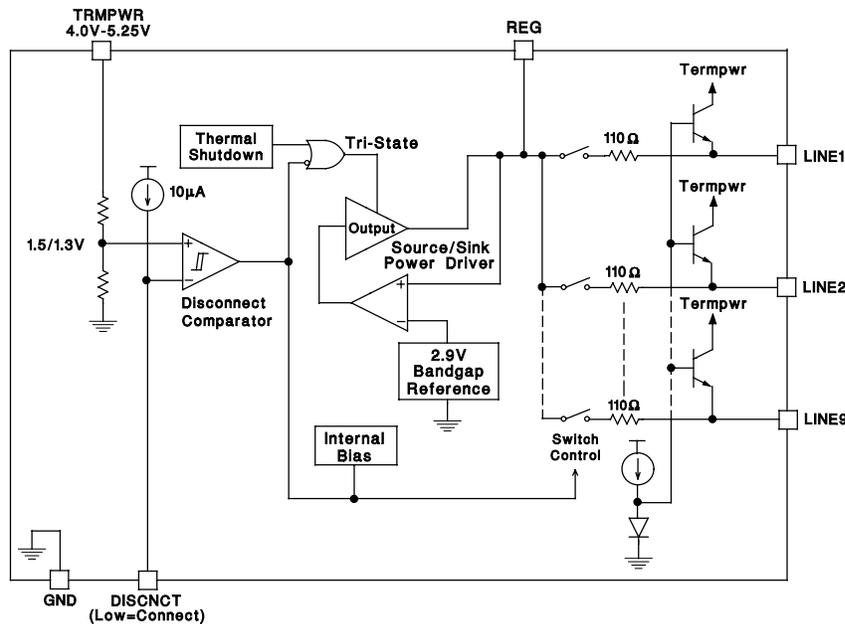
description

The UC5603 provides 9 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The UC5603 provides a disconnect feature which, when opened or driven high, will disconnect all terminating resistors, and disables the regulator; greatly reducing standby power. The output channels remain high impedance even without Tempwr applied. A low channel capacitance of 6 pF allows units at interim points of the bus to have little to no effect on the signal integrity.

Functionally the UC5603 is similar to its predecessor, the UC5601 – 18 line Active Terminator. Several electrical enhancements were incorporated in the UC5603, such as a sink/source regulator output stage to accommodate all signal lines at 5 V, while the regulator remains at its nominal value, reduced channel capacitance to 6 pF typical, and as with the UC5601, custom power packages are utilized to allow normal operation at full power conditions (1.2 watts).

functional block diagram



UDG-94049



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

UC5603

9-LINE SCSI ACTIVE TERMINATOR

SLUS195B – MARCH 1997 – REVISED NOVEMBER 2003

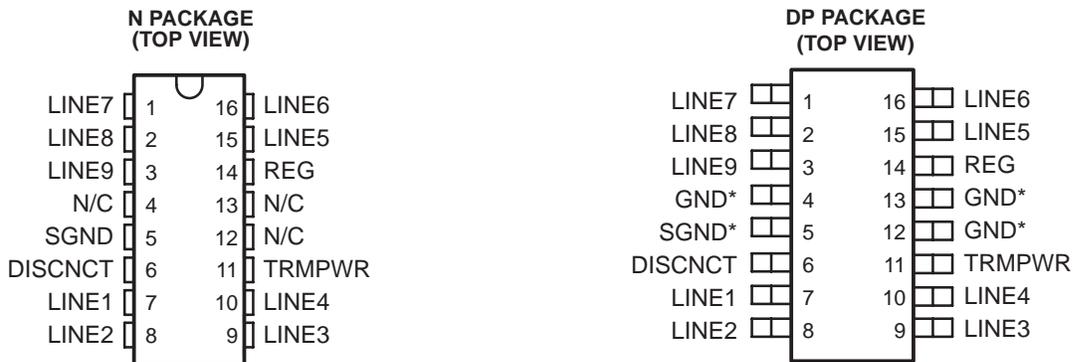
description (continued)

Internal circuit trimming is utilized, first to trim the impedance to a 3% tolerance, and then most importantly, to trim the output current to a 3% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include negative clamping on all signal lines to protect external circuitry from latch-up, thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC.

connection diagrams



* DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.

ORDERING INFORMATION

| T _A = T _J | Packaged Devices | |
|---------------------------------|------------------|---------------|
| | DIL -16(N) | SOIC-16 (DP)† |
| 0°C to 70°C | UC5603N | UCUC5603DP |

† DP (SOIC-16) packages are available taped and reeled. Add TR suffix to device type (e.g. UC5603DPTR) to order quantities of 2000 devices per reel.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)^{†‡}

| | |
|---|----------------|
| Tempwr voltage | 7 V |
| Signal line voltage | 0V to 7 V |
| Regulator output current | 0.5 A |
| Storage temperature | –65°C to 150°C |
| Operating temperature | –55°C to 150°C |
| Lead temperature (soldering, 10 sec.) | 300°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

recommended operating conditions

| | |
|------------------------------------|-----------------|
| Tempwr voltage | 3.8 V to 5.25 V |
| Signal line voltage | 0 V to 5 V |
| Disconnect input voltage | 0 V to Tempwr |

electrical characteristics, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75 V DISCNCT = 0 V, T_A = T_J, (unless otherwise stated)

supply current section

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------|-------------------------------|-----|-----|-----|-------|
| Tempwr supply current | All termination lines = Open | | 12 | 18 | mA |
| | All termination lines = 0.5 V | | 200 | 220 | mA |
| Power down mode | DISCNCT = Open | | 100 | 150 | µA |

output section (terminator lines)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS | | |
|----------------------|--|--|--|-------|-------|-------|----|
| Terminator impedance | $\Delta I_{LINE} = -5 \text{ mA to } -15 \text{ mA}$ | 107 | 110 | 113 | Ω | | |
| Output high voltage | $V_{TRMPWR} = 4 \text{ V}$, See Note 1 | 2.7 | 2.9 | | V | | |
| Max output current | $V_{LINE} = 0.5 \text{ V}$ | $T_J = 25^\circ\text{C}$ | -21.1 | -21.9 | -22.4 | mA | |
| | | $0^\circ\text{C} < T_J < 70^\circ\text{C}$ | -20.5 | -21.9 | -22.4 | mA | |
| Max output current | $V_{LINE} = 0.5 \text{ V}$, See Note 1 | TRMPWR = 4 V, | $T_J = 25^\circ\text{C}$ | -20.3 | -21.9 | -22.4 | mA |
| | | | $0^\circ\text{C} < T_J < 70^\circ\text{C}$ | -19.8 | -21.9 | -22.4 | mA |
| | $V_{LINE} = 0.2 \text{ V}$, | TRMPWR = 4.0 V to 5.25 V | $0^\circ\text{C} < T_J < 70^\circ\text{C}$ | -22.0 | -24.0 | -25.4 | mA |
| Output clamp level | $I_{LINE} = -30 \text{ mA}$ | -0.2 | -0.05 | 0.1 | V | | |
| Output leakage | DISCNCT = 4 V | TRMPWR = 0 V to 5.25, VREG = 0 V | $V_{LINE} = 0 \text{ to } 4 \text{ V}$ | 10 | 400 | nA | |
| | | | $V_{LINE} = 5.25 \text{ V}$ | | 100 | µA | |
| | | TRMPWR = 0 V to 5.25 V, $V_{LINE} = 0 \text{ V to } 5.25 \text{ V}$ | REG = Open | 10 | 400 | nA | |
| Output capacitance | DISCNCT = Open | See Note 2 | DP Package | 6 | 8 | pF | |

NOTES: 1. Measuring each termination line while other 8 are low (0.5 V).
2. Ensured by design. Not production tested.

UC5603 9-LINE SCSI ACTIVE TERMINATOR

SLUS195B – MARCH 1997 – REVISED NOVEMBER 2003

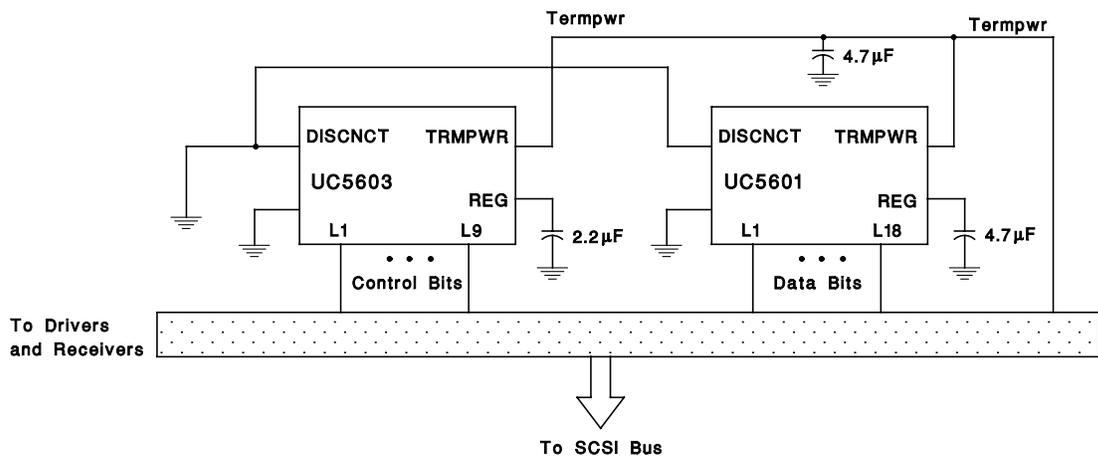
regulator section

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------|--------------------------------------|------|------|------|-------|
| Regulator output voltage | | 2.8 | 2.9 | 3 | V |
| Regulator output voltage | All termination lines = 5 V | 2.8 | 2.9 | 3 | V |
| Line regulation | TRMPWR = 4 V to 6 V | | 10 | 20 | mV |
| Load regulation | I _{REG} = 100 mA to -100 mA | | 20 | 50 | mV |
| Drop out voltage | All termination lines = 0.5 V | | 0.7 | 1 | V |
| Short circuit current | V _{REG} = 0 V | -200 | -400 | -600 | mA |
| Sinking current capability | V _{REG} = 3.5 V | 200 | 400 | 600 | mA |
| Thermal shutdown | | | 170 | | °C |
| Thermal shutdown hysteresis | | | 10 | | °C |

disconnect section

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------|-----------------|-----|-----|-----|-------|
| Disconnect threshold | | 1.3 | 1.5 | 1.7 | V |
| Threshold hysteresis | | 100 | 160 | 250 | mV |
| Input current | DISCNECT = 0 V | | 10 | 15 | mA |

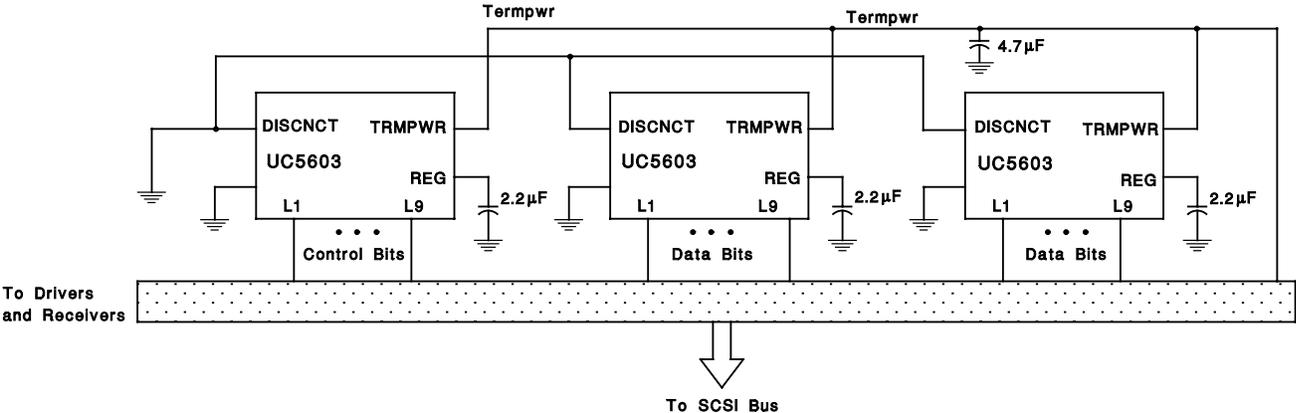
APPLICATION INFORMATION



UDG-94050

Figure 1. Typical Wide SCSI Bus Configurations Utilizing 1 UC5601 and 1 UC5603 Device

APPLICATION INFORMATION



UDG-94051

Figure 2. Typical Wide SCSI Bus Configurations Utilizing 3 UC5603 Devices

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|-------------------------|----------------------|--------------|-------------------------|---------|
| UC5603DP | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | 0 to 70 | UC5603DP | |
| UC5603DPG4 | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | 0 to 70 | UC5603DP | |
| UC5603DPR | NRND | SOIC | D | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| UC5603DPRTR | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| UC5603DPTR | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | 0 to 70 | UC5603DP | |
| UC5603DPTRG4 | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| UC5603J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| UC5603QPTR | OBSOLETE | PLCC | FN | 28 | | TBD | Call TI | Call TI | 0 to 70 | UC5603QP | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

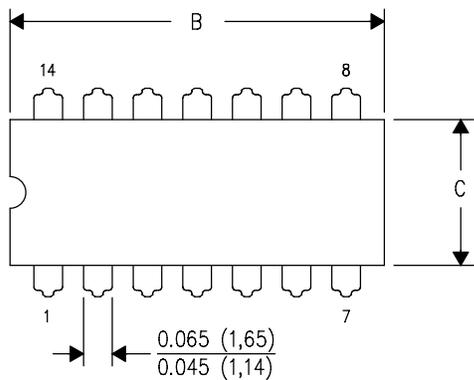
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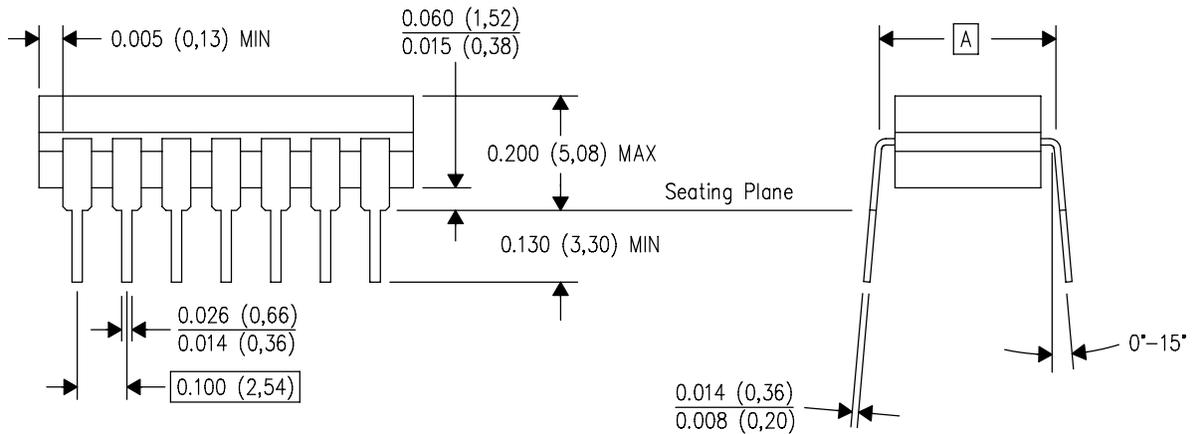
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

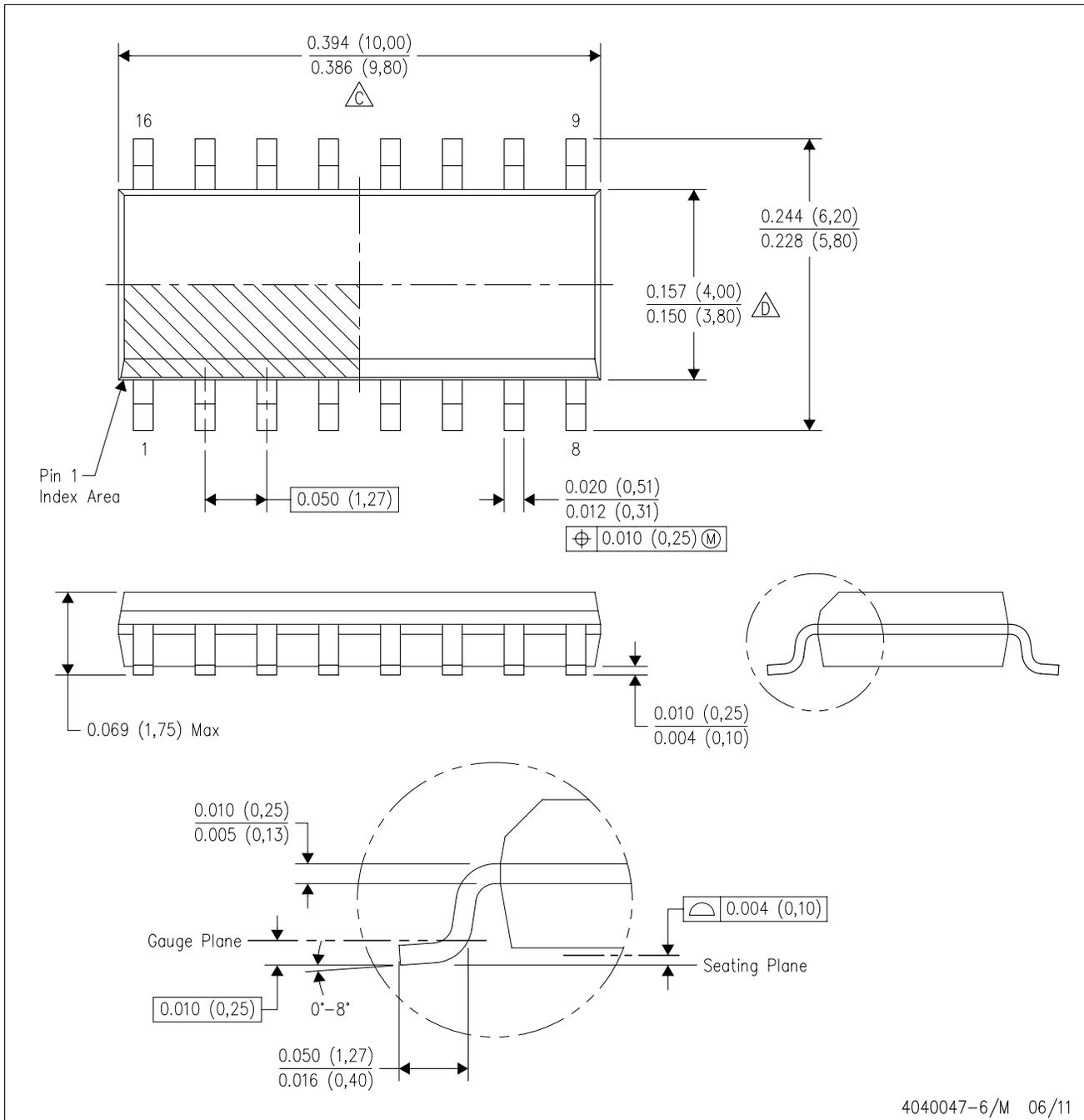


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- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

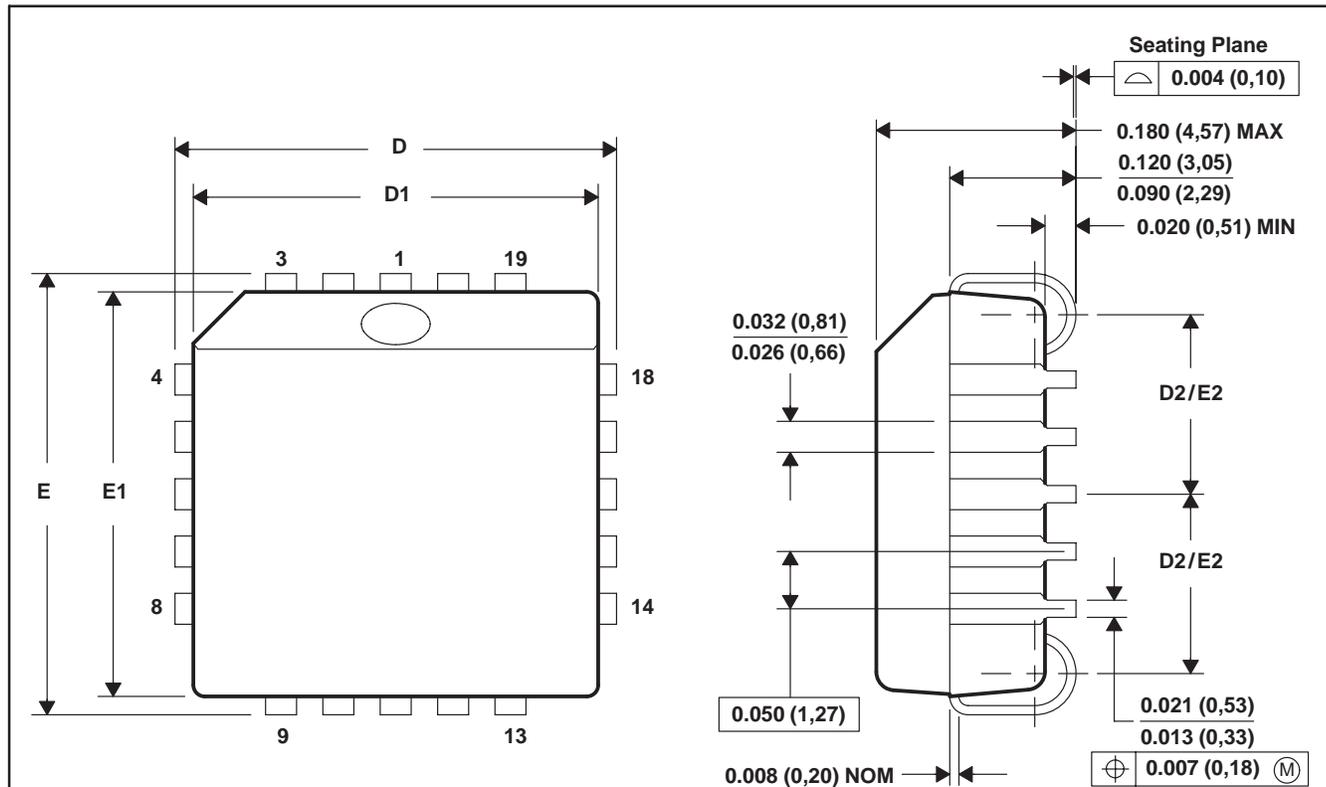


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



| NO. OF PINS ** | D/E | | D1/E1 | | D2/E2 | |
|----------------|---------------|---------------|---------------|---------------|---------------|---------------|
| | MIN | MAX | MIN | MAX | MIN | MAX |
| 20 | 0.385 (9,78) | 0.395 (10,03) | 0.350 (8,89) | 0.356 (9,04) | 0.141 (3,58) | 0.169 (4,29) |
| 28 | 0.485 (12,32) | 0.495 (12,57) | 0.450 (11,43) | 0.456 (11,58) | 0.191 (4,85) | 0.219 (5,56) |
| 44 | 0.685 (17,40) | 0.695 (17,65) | 0.650 (16,51) | 0.656 (16,66) | 0.291 (7,39) | 0.319 (8,10) |
| 52 | 0.785 (19,94) | 0.795 (20,19) | 0.750 (19,05) | 0.756 (19,20) | 0.341 (8,66) | 0.369 (9,37) |
| 68 | 0.985 (25,02) | 0.995 (25,27) | 0.950 (24,13) | 0.958 (24,33) | 0.441 (11,20) | 0.469 (11,91) |
| 84 | 1.185 (30,10) | 1.195 (30,35) | 1.150 (29,21) | 1.158 (29,41) | 0.541 (13,74) | 0.569 (14,45) |

4040005/B 03/95

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

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