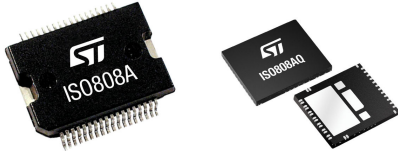


## Galvanic isolated octal high-side power solid state relay with SPI interface for high inductive loads



### Product status link

[ISO808A](#)

[ISO808A-1](#)

### Product label



### Features

- $V_{CC(AMR)} = 45\text{ V}$
- Wide process side op. range  $V_{CC} = 9.2\text{ to }36\text{ V}$
- $R_{DS(on)} = 0.125\ \Omega$  per channel (TYP)
- Fast demagnetization of inductive loads  $V_{DEMAG(TYP)} = V_{CC} - 54\text{ V}$
- Per channel process side op. current
  - ISO808A/ISO808AQ  $I_{OUT} < 0.7\text{ A}$
  - ISO808A-1/ISO808AQ-1  $I_{OUT} < 1\text{ A}$
- Low process and logic sides supply current
- Under-voltage shut down with auto restart and hysteresis
- Logic side 5 V and 3.3 V TTL/CMOS and MCU compatible I/Os
- Logic side SPI interface
- Common output enable/disable pin
- Reset function for IC outputs disable
- High common mode transient immunity
- Short circuit protection on output channels
  - ISO808A/ISO808AQ  $I_{LIM(MIN)} = 0.7\text{ A}$
  - ISO808A-1/ISO808AQ-1  $I_{LIM(MIN)} = 1\text{ A}$
- Per-channel over-temperature protection with thermal independence of separate channels
- Case over-temperature protection
- Over-voltage protection ( $V_{CC}$  clamping)
- Loss of GND and  $V_{CC}$  protections
- Common fault open drain diagnostic
- $V_{CC}$  Power Good open drain diagnostic for 24 V applications
- Designed to meet IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5 and IEC 61000-4-8
- UL1577 and UL508 certified
- Safety limits according to IEC 60747-17 (former VDE 0884-11)
- PowerSO-36 and TFQFPN32 Package

### Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- Drivers for all type of loads (resistive, capacitive, inductive)

## Description

The ISO808A, ISO808A-1 (PowerSO-36) and ISO808AQ, ISO808AQ-1 (TFQFPN32) are galvanic isolated 8-channel drivers featuring a low supply current. Each driver contains 2 independent galvanic isolated voltage domains ( $V_{CC}$  and  $V_{DD}$  for the Process and Control Logic stages, respectively). The ICs are intended for driving any kind of load with one side connected to ground.

The Control Logic Stage features an 8-bit Output Status Register (where the MCU sets the ON/OFF status of the output channels in the Process Stage), daisy chaining is allowed. The two stages communicate through the galvanic isolation channel by an ST proprietary protocol.

Active channel current limitation (OVL) combined with thermal shutdown (OVT), independent for each channel, protects the device against overload.

Built-in thermal shut down protects each channel from over-temperature and overload: each overheated channel automatically turns OFF after its junction temperature triggers the protection threshold ( $T_{JSD}$ ). The channel turns back ON if its junction temperature decreases lower than restart threshold ( $T_{JR}$ ).

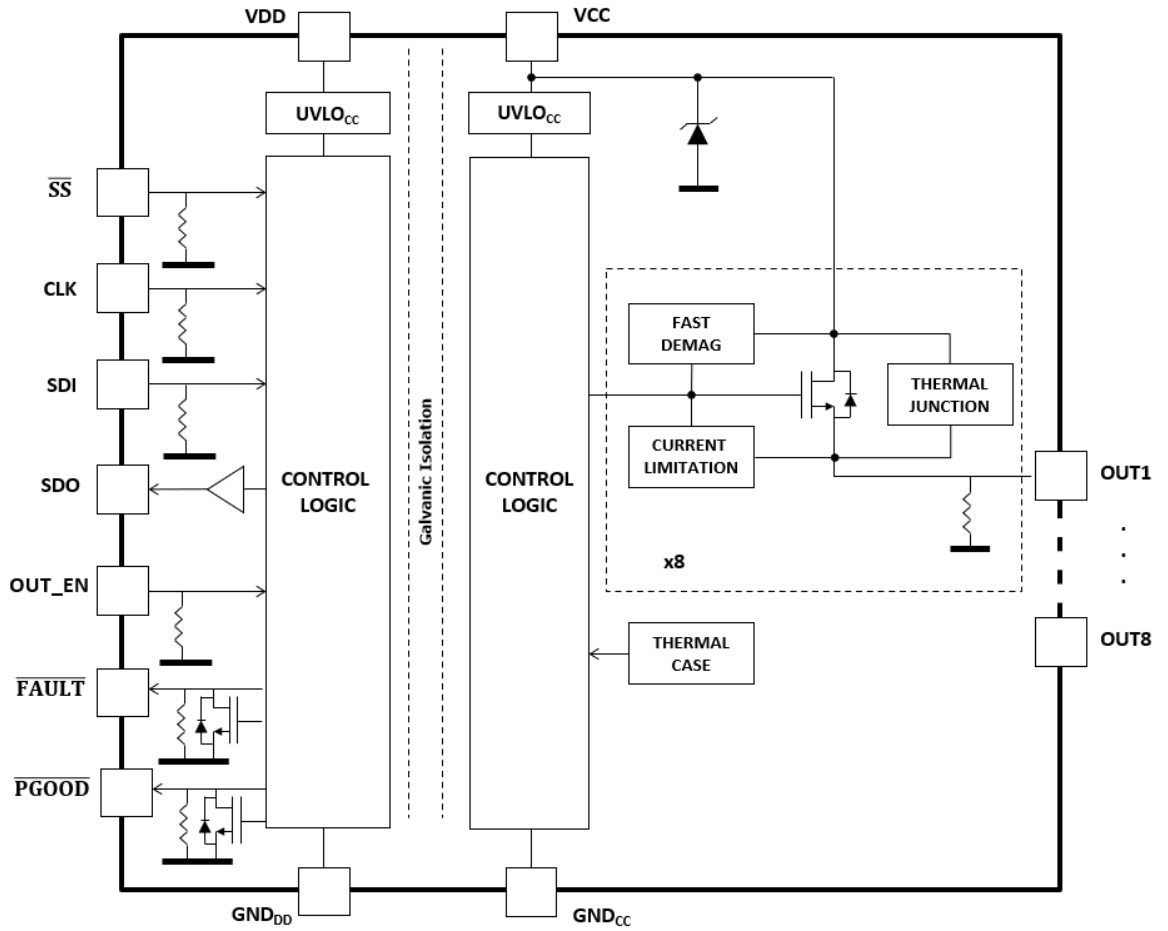
An additional case temperature sensor protects the whole chip against over-temperature (OVC event): if the case temperature triggers the  $T_{CSD}$  threshold then overloaded channels are turned OFF and will restart only when case temperature decreased down to the reset threshold ( $T_{CR}$ ). Non overloaded channels continue to operate normally.

Other embedded functions are loss of ground protection,  $V_{CC}$  and  $V_{DD}$  UVLOs (with hysteresis), watchdog and  $V_{CC}$  Power GOOD.

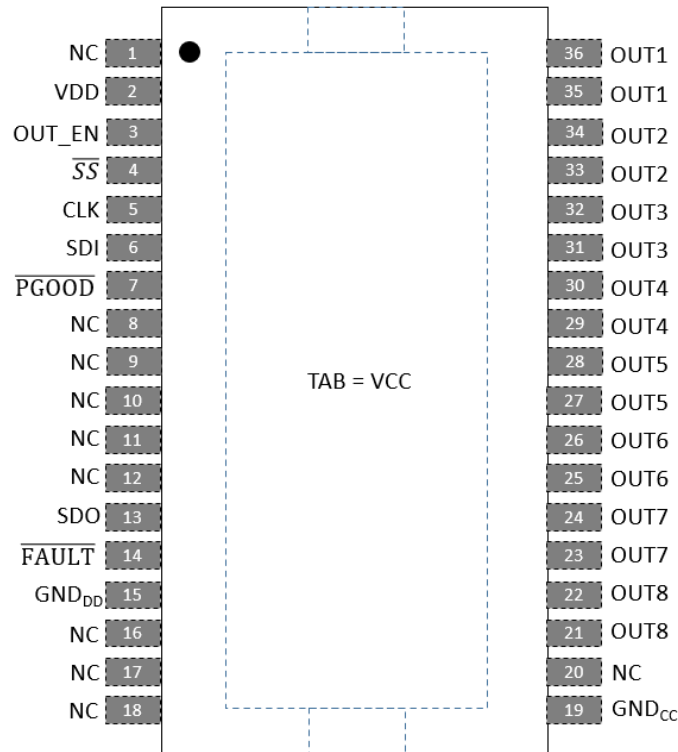
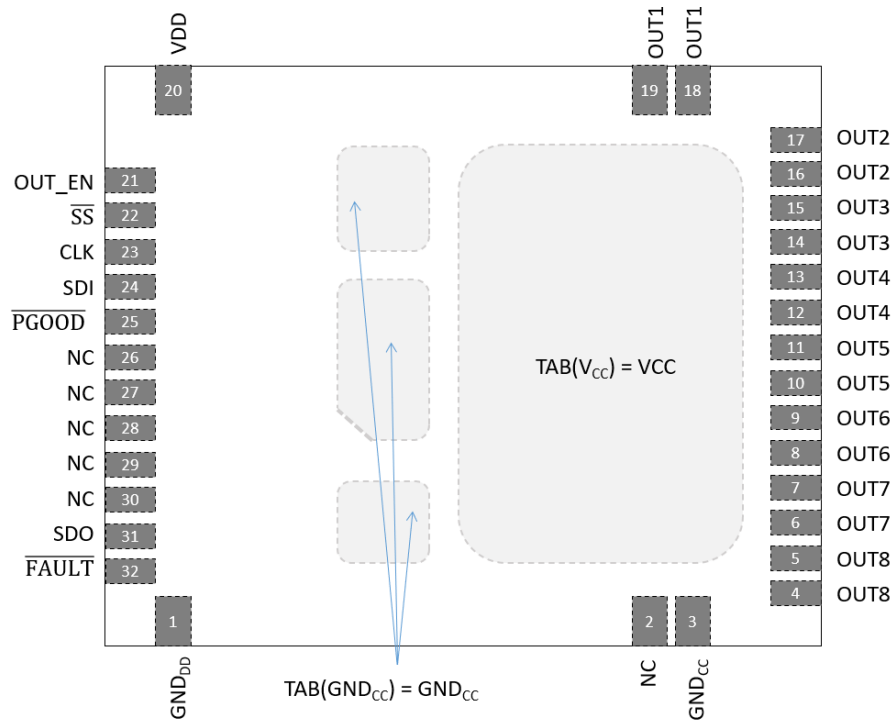
An internal circuit provides an OR-wired not latched common  $\overline{FAULT}$  indicator signaling the channel OVT. The PGOOD diagnostic pin is activated if  $V_{CC}$  goes below the power good threshold. Both  $\overline{FAULT}$  and PGOOD pins are open drain, active low, fault indication pins.

# 1 Block diagram

Figure 1. Block diagram



## 2 Pin connection

**Figure 2. Pin connection PowerSO-36 (top through view)**

**Figure 3. Pin connection TFQFPN32 (top through view)**


**Table 1. Pin description**

Pin		Name	Description
PowerSO-36	TFQFPN32		
1	-	N.C.	Not connected
2	20	V <sub>DD</sub>	Positive Control Logic Stage supply
3	21	OUT_EN	Output enable
4	22	$\overline{SS}$	Chip select
5	23	CLK	Serial Clock Digital Input
6	24	SDI	SPI device Input (MOSI)
7	25	$\overline{PGOOD}$	Power Good diagnostic pin - active low
8	26	NC	Not connected
9	27	NC	Not connected
10	28	NC	Not connected
11	29	NC	Not connected
12	30	NC	Not connected
13	31	SDO	SPI device Output (MOSI)
14	32	$\overline{FAULT}$	Common fault (OVT and Internal Communication Error) pin - active low
15	1	GND <sub>DD</sub>	Input logic ground, negative logic supply
16	-	NC	Not connected
17	-	NC	Not connected
18	2	NC	Not connected
19	3	GND <sub>CC</sub>	Output (process stage) power ground
-	TAB(GND <sub>CC</sub> )	TAB(GND <sub>CC</sub> )	Connect to GND <sub>CC</sub> on the application board
20	-	NC	Not connected
21	4	OUT8	Channel 8 power output <sup>(1)</sup>
22	5		
23	6	OUT7	Channel 7 power output <sup>(1)</sup>
24	7		
25	8	OUT6	Channel 6 power output <sup>(1)</sup>
26	9		
27	10	OUT5	Channel 5 power output <sup>(1)</sup>
28	11		
29	12	OUT4	Channel 4 power output <sup>(1)</sup>
30	13		
31	14	OUT3	Channel 3 power output <sup>(1)</sup>
32	15		
33	16	OUT2	Channel 2 power output <sup>(1)</sup>
34	17		
35	18	OUT1	Channel 1 power output <sup>(1)</sup>
36	19		
TAB	TAB(V <sub>CC</sub> )	V <sub>CC</sub>	Exposed tab internally connected to V <sub>CC</sub> positive Process Stage supply voltage

1. Connect the two pins on the same net of the application board

### 3 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Process Stage supply voltage	-0.3	+45	V
$V_{DD}$	Control Logic Stage supply voltage	-0.3	+6	V
$V_{IN}$	DC Input pins ( $\overline{SS}$ , CLK, SDI and OUT_EN) voltage	-0.3	$V_{DD}$	V
$V_{SDO}$	DC SDO pin voltage	-0.3	$V_{DD}$	V
$V_{FAULT}$ , $V_{PGOOD}$	$\overline{FAULT}$ and $\overline{PGOOD}$ pins voltage	-0.3	+6.0	V
$I_{GNDdd}$	DC digital ground Reverse Current		-25	mA
$I_{OUT}$	Channel Output Current (continuous)		Internally limited	A
$I_{GNDcc}$	DC Power Ground Reverse Current		-250	mA
$I_{RX}$	Reverse Output Current (from OUTx pins to $V_{CC}$ )		-6 <sup>(1)</sup>	A
$I_{IN}$	DC Input pins ( $\overline{SS}$ , CLK, SDI and OUT_EN) current	-10	+10	mA
$I_{FAULT}$ , $I_{PGOOD}$	$\overline{FAULT}$ and $\overline{PGOOD}$ pins current	-10	+10	mA
$V_{ESD}$	Electrostatic discharge with Human Body Model (R = 1.5 k $\Omega$ ; C = 100 pF)		2000	V
$V_{IO}$	Isolation DC voltage applied between GND <sub>DD</sub> and GND <sub>CC</sub> pins for PowerSO-36		180	V
	Isolation DC voltage applied between GND <sub>DD</sub> and GND <sub>CC</sub> pins for TFQFPN32		75	
EAS	Single pulse avalanche energy per channel, all channels driven simultaneously @ $T_{AMB}$ = 125 °C, $I_{OUT}$ = 0.6 A (PowerSO-36)		2.11	J
	Single pulse avalanche energy per channel, all channels driven simultaneously @ $T_{AMB}$ = 125 °C, $I_{OUT}$ = 0.6 A (TFQFPN32)		0.48	
$P_{TOT}$	Power dissipation		Internally limited <sup>(2)</sup>	W
$T_J$	Junction operating temperature		Internally limited <sup>(2)</sup>	°C
$T_{STG}$	Storage temperature		-40 to 150	°C

1. this value is intended with each couple of OUTx pins shorted on the application board

2. Protection functions are intended to avoid IC damage in fault conditions and are not intended for continuous operation. Continuous or repetitive operation of protection functions may reduce the IC lifetime.

## 4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value		Unit
		PowerSO-36	TFQFPN32	
$R_{th\ j-case}$	Thermal resistance, junction-to-case <sup>(1)</sup>	0.8	1	°C/W
$R_{th\ j-amb}$	Thermal resistance, junction-to-ambient <sup>(2)</sup>	16.9 <sup>(3)</sup>	25 <sup>(4)</sup>	

1.  $R_{th}$  between the die and the bottom case surface measured by cold plate as per JESD51-12.

2. JESD51-7.

3. Maximum power dissipation = 3.8W (@ $T_{amb} = 85^{\circ}C$ ,  $T_J < 150^{\circ}C$ )

4. Maximum power dissipation = 2.6W (@ $T_{amb} = 85^{\circ}C$ ,  $T_J < 150^{\circ}C$ )

## 5 Electrical characteristics

9.2 V ≤ V<sub>CC</sub> ≤ 36 V; 2.75 V ≤ V<sub>DD</sub> ≤ 5.5 V; -40 °C < T<sub>J</sub> < 125 °C, unless otherwise specified.

**Table 4. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Operating voltage range		9.2		36	V
V <sub>CC(THON)</sub>	V <sub>CC</sub> undervoltage turn-on threshold	V <sub>DD</sub> = 3.3 V, V <sub>CC</sub> increasing		8.4	9.2	V
V <sub>CC(THOFF)</sub>	V <sub>CC</sub> undervoltage turn-off threshold	V <sub>DD</sub> = 3.3 V, V <sub>CC</sub> decreasing	7.7	8.1		V
V <sub>CC(HYS)</sub>	V <sub>CC</sub> undervoltage hysteresis			0.15		V
V <sub>CCclamp</sub>	Clamp on VCC pin	I <sub>clamp</sub> = 20 mA	47	52	57	V
V <sub>CC(PGON)</sub>	V <sub>CC</sub> Power Good turn-on threshold	V <sub>DD</sub> = 3.3 V, V <sub>CC</sub> increasing		16.6	18.7	V
V <sub>CC(PGOFF)</sub>	V <sub>CC</sub> Power Good turn-off threshold	V <sub>DD</sub> = 3.3 V, V <sub>CC</sub> decreasing	14.5	16.1		V
V <sub>CC(PG- HYS)</sub>	V <sub>CC</sub> Power Good hysteresis			0.5		V
R <sub>DS(ON)</sub>	ON-state resistance (see Figure 4)	I <sub>OUT</sub> = 0.5 A, T <sub>J</sub> = 25 °C		0.125	0.16	Ω
		I <sub>OUT</sub> = 0.5 A, T <sub>J</sub> = 125 °C			0.26	
I <sub>CC</sub>	Power supply current	All channels in OFF-state, V <sub>CC</sub> = 36 V		5.5		mA
		All channels in ON-state, V <sub>CC</sub> = 36 V		16		
I <sub>LGND</sub>	Ground disconnection output current	V <sub>CC</sub> = V <sub>GND</sub> = 0 V V <sub>OUT</sub> = -24 V			500	μA
V <sub>OUT(OFF)</sub>	OFF-state output voltage	Channel OFF and I <sub>OUT</sub> = 0 A			3	V
I <sub>OUT(OFF)</sub>	OFF-state output current	Channel OFF and V <sub>OUT</sub> = 0 V			5	μA

**Table 5. Digital supply voltage**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operating voltage range		2.75		5.5	V
V <sub>DD(THON)</sub>	V <sub>DD</sub> undervoltage turn-on threshold	V <sub>CC</sub> = 24 V, V <sub>DD</sub> increasing	2.55		2.75	V
V <sub>DD(THOFF)</sub>	V <sub>DD</sub> undervoltage turn-off threshold	V <sub>CC</sub> = 24 V, V <sub>DD</sub> decreasing	2.45		2.65	V
V <sub>DD(HYS)</sub>	V <sub>DD</sub> undervoltage hysteresis		0.04	0.1		V
I <sub>DD</sub>	V <sub>DD</sub> supply current	V <sub>DD</sub> = 5 V and SPI not transmitting		4.5	6	mA
		V <sub>DD</sub> = 3.3 V and SPI not transmitting		4.4	5.9	mA



**Table 6. Diagnostic pin and output protection function**

Symbol	Parameter		Test conditions	Min.	Typ.	Max.	Unit
V <sub>FAULT</sub>	FAULT pin open drain voltage output low		I <sub>FAULT</sub> = 5 mA			0.4	V
I <sub>LFAULT</sub>	FAULT output leakage current		V <sub>FAULT</sub> = 5 V			1	μA
V <sub>PGOOD</sub>	PGOOD pin open drain voltage output low		I <sub>PGOOD</sub> = 5 mA			0.4	V
I <sub>LPGOOD</sub>	PGOOD output leakage current		V <sub>PGOOD</sub> = 5 V			1	μA
I <sub>PEAK</sub>	Maximum DC output current before limitation		V <sub>CC</sub> = 24 V; R <sub>LOAD</sub> = 0 Ω			2.3	A
I <sub>LIM</sub>	Short-circuit current limitation	ISO808A, ISO808AQ		0.7		1.9	A
		ISO808A-1, ISO808AQ-1		1			
Hyst	I <sub>LIM</sub> tracking limits				0.3		A
T <sub>JSD</sub>	Junction shutdown temperature			150	175	200	°C
T <sub>JR</sub>	Junction reset temperature				160		°C
T <sub>JHYST</sub>	Junction thermal hysteresis				15		°C
T <sub>CS</sub>	Case shutdown temperature			125	130	135	°C
T <sub>CR</sub>	Case reset temperature				115		°C
T <sub>CHYST</sub>	Case thermal hysteresis				15		°C
V <sub>DEMAG</sub>	Output voltage at turn-off		I <sub>OUT</sub> = 0.5 A; I <sub>LOAD</sub> ≥ 1 mH	V <sub>CC</sub> -50	V <sub>CC</sub> -54	V <sub>CC</sub> -58	V

**Table 7. Power switching characteristics (V<sub>CC</sub> = 24 V; R<sub>LOAD</sub> = 48 Ω; -40 °C < T<sub>J</sub> < 125 °C)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dV/dt(ON)	Turn-on voltage slope	(see Figure 5)		0.7		V/μs
t <sub>r</sub>	Rise time			19	32	μs
dV/dt(OFF)	Turn-off voltage slope			1.5		V/μs
t <sub>f</sub>	Fall time			7	23	μs
t <sub>d(ON)</sub>	Turn-ON delay time	(see Figure 6)		15	24	μs
t <sub>d(OFF)</sub>	Turn-OFF delay time			43	80	μs
t <sub>w(OUT_EN)</sub>	OUT_EN pulse width	(see Figure 11, Figure 12)	150			ns
t <sub>p(OUT_EN)</sub>	OUT_EN propagation delay			40	80	μs

Figure 4.  $R_{DS(on)}$  measurement

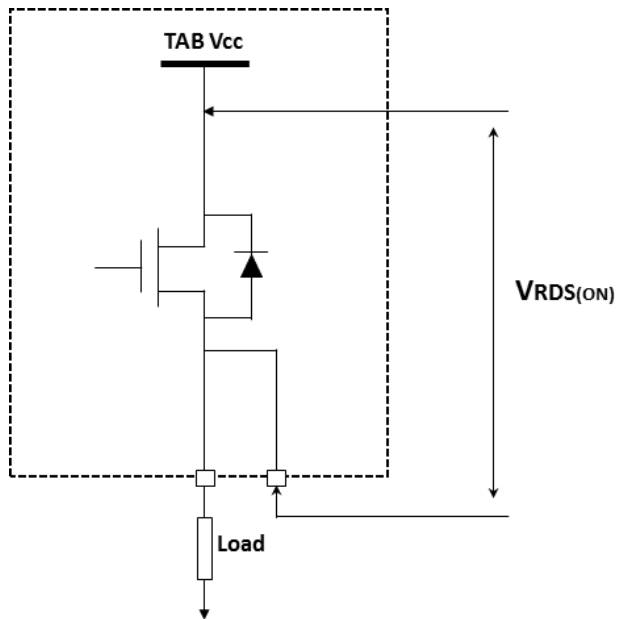


Figure 5.  $dV/dt$  definition

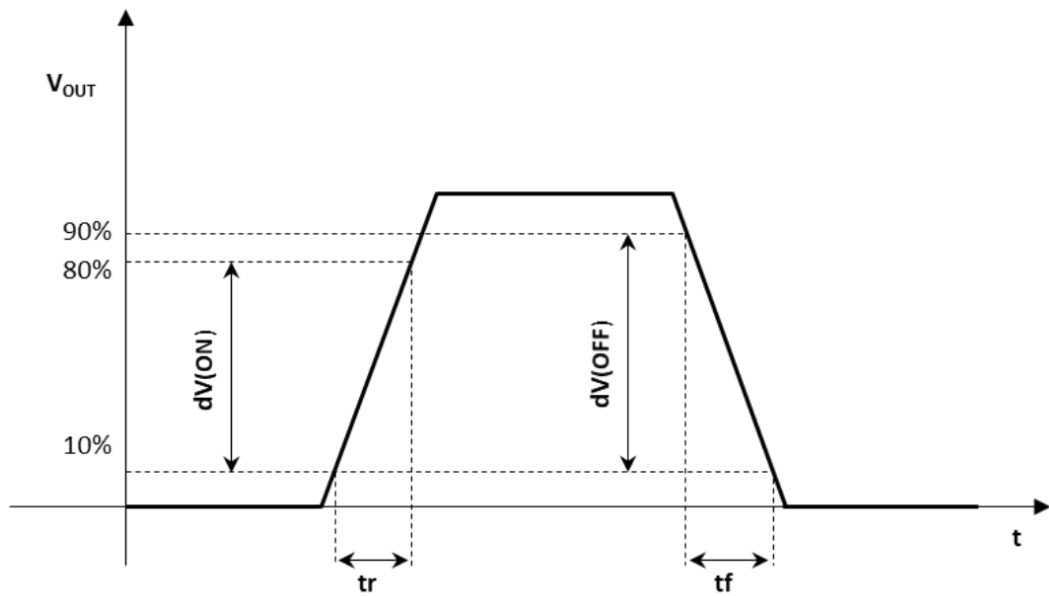


Figure 6. td(ON)-td(OFF) definition

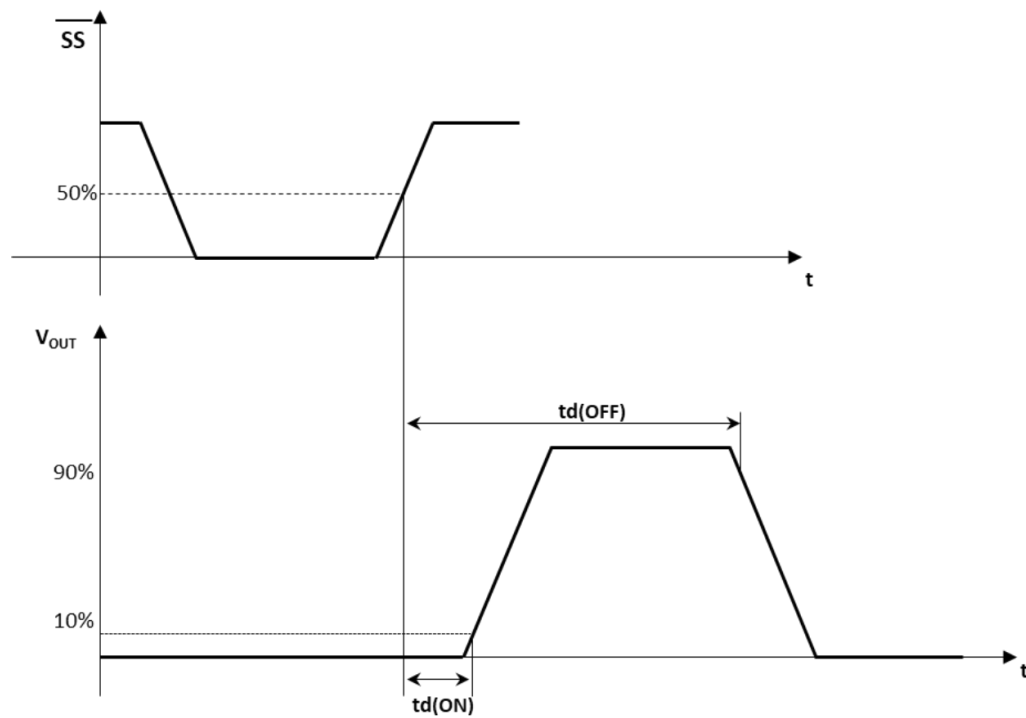


Table 8. Logic inputs and output

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	$\overline{SS}$ , CLK, SDI and OUT_EN low level voltage		-0.3		$0.3 \times V_{DD}$	V
$V_{IH}$	$\overline{SS}$ , CLK, SDI and OUT_EN high level voltage		$0.7 \times V_{DD}$		$V_{DD} + 0.3$	V
$V_{I(HYST)}$	$\overline{SS}$ , CLK, SDI and OUT_EN hysteresis	$V_{DD} = 5\text{ V}$		100		mV
$I_{IN}$	$\overline{SS}$ , CLK, SDI and OUT_EN current	$V_{IN} = 5\text{ V}$	10	55	90	$\mu\text{A}$
$V_{SDOH}$	SDO high level voltage	$I_{SDO} = -1\text{ mA}$	$V_{DD} - 0.2$			V
$V_{SDOL}$	SDO low level voltage	$I_{SDO} = +2\text{ mA}$			0.2	V

**Table 9. Serial interface timings ( $V_{DD} = 5\text{ V}$ ;  $V_{CC} = 24\text{ V}$ ;  $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$f_{CLK}$	SPI clock frequency				20	MHz
$T_{CLK}$	SPI clock period		50			ns
$t_r(CLK)$ $t_f(CLK)$	SPI clock rise/fall time (see Figure 8, Figure 9)				5	ns
$t_{su}(SS)$	SS setup time (see Figure 8, Figure 9)		80			ns
$t_{h}(SS)$	SS hold time (see Figure 8, Figure 9)		80			ns
$t_{c}(SS)$	SS disable time (see Figure 8, Figure 9)		20			$\mu\text{s}$
$t_w(CLK)$	CLK high time (see Figure 8, Figure 9)		15			ns
$t_{su}(SDI)$	Data input setup time (see Figure 8, Figure 9)		6			ns
$t_{h}(SDI)$	Data input hold time (see Figure 8, Figure 9)		6			ns
$t_a(SDO)$	Data output access time (see Figure 8, Figure 9)	$R_{PULL-DOWN} = 300\ \Omega$ $C_{LOAD} = 50\ \text{pF}$			25	ns
$t_{dis}(SDO)$	Data output disable time (see Figure 8, Figure 9)				20	ns
$t_v(SDO)$	Data output valid time (see Figure 8, Figure 9)				20	ns
$t_{JITTER}$	Jitter on single channel $t_{CYCLE(SS)} = 20\ \mu\text{s}$				6	$\mu\text{s}$
	Jitter on single channel $t_{CYCLE(SS)} < 20\ \mu\text{s}$				20	

**Table 10. Internal communication timings ( $V_{DD} = 5\text{ V}$ ;  $V_{CC} = 24\text{ V}$ ;  $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$f_{refresh}$	Refresh delay			15		kHz
$t_{WD}$	Watchdog time		272	320	400	$\mu\text{s}$

**Table 11. Insulation and safety-related specifications**

Symbol	Parameter	Test conditions	Value		Unit
			PowerSO36	TFQFPN32	
CLR <sup>(1)</sup>	Clearance (minimum external air gap)	Measured from input terminals to output terminals, shortest distance through air	2.6	3.3	mm
CPG <sup>(1)</sup>	Creepage (minimum external tracking)	Measured from input terminals to output terminals, shortest distance path along body	2.6	3.3	mm
CTI <sup>(2)</sup>	Comparative tracking index (tracking resistance)		$\geq 400$	$\geq 600$	V
	Isolation group	Material group	II	I	-

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standard of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the PCB do not reduce this distance.
2. When high voltage is applied across the isolator, electric discharges on or close to the surface of the package, can cause localized deterioration in the mold compound, resulting in a partially conducting path from one side of the isolator to the other. This phenomenon is called tracking. The ability of a material to withstand tracking is quantified by a comparative tracking index (CTI). Using a mold compound with a higher CTI allows the use of smaller packages and saves board space.

**Table 12. Insulation characteristics**

Symbol	Parameter	Test condition	Value		Unit
			PowerSO36	TFQFPN32	
<b>In accordance with IEC 60747-17</b>					
V <sub>PR</sub>	Input-to-output test voltage	Method a, type test, t <sub>m</sub> = 10 s partial discharge < 5 pC	1500	1500	V <sub>PEAK</sub>
		Method b, 100% production test, t <sub>m</sub> = 1 s partial discharge < 5 pC	1758	1758	V <sub>PEAK</sub>
V <sub>IOTM</sub>	Transient overvoltage	Type test; t <sub>ini</sub> = 60 s	3537	4245	V <sub>PEAK</sub>
V <sub>IOSM</sub>	Maximum surge insulation voltage	Type test	3537	4245	V <sub>PEAK</sub>
R <sub>IO</sub>	Insulation resistance	Type test V <sub>IO</sub> = 500 V, T <sub>STG</sub> = 60 s	>10 <sup>9</sup>	>10 <sup>9</sup>	Ω
<b>UL1577</b>					
V <sub>ISO</sub>	Insulation withstand voltage	1 min. type test	2000/2830	2500/3536	V <sub>RMS</sub> /V <sub>PEAK</sub>
V <sub>ISO test</sub>	Insulation withstand test	1 s 100% production	2500/3537	3000/4245	V <sub>RMS</sub> /V <sub>PEAK</sub>
<b>Common Mode Transient Immunity</b>					
dV <sub>ISO</sub> /dt	CMTI	Type test at V <sub>CM</sub> = 500 V	±25	±25	V/ns

**Table 13. Safety limits**

Symbol	Parameter	Test conditions	Value	Unit
<b>Input safety, Logic side</b>				
T <sub>SI</sub>	Safety temperature of Logic side	-	150	°C
P <sub>SI</sub>	Safety power of Logic side <sup>(1)</sup>	V <sub>DD</sub> ≤ 6.0 V, V <sub>LOGIC(x)</sub> ≤ 6.0 V, I <sub>LOGIC(x)</sub> ≤ 10 mA, T <sub>J</sub> ≤ T <sub>SI</sub>	0.9	W
<b>Output safety, Process side</b>				
T <sub>SO</sub>	Safety temperature of Process side	-	150	°C
P <sub>SO</sub>	Safety power of Process side <sup>(1)</sup>	V <sub>CC</sub> ≤ 36 V, I <sub>OUT(x)</sub> ≤ 1.5 A, T <sub>J</sub> ≤ T <sub>SO</sub>	5	W

1. The above limits are measured according to IEC 60747-17. Respecting the above limits prevents potential damage to the isolation barrier upon failure on logic or process side circuitry. The user should apply these values to protect the IC and ensure the safety of the embedded isolation barrier. LOGIC(x) stands for any pin on the logic side; OUT(x) stands for any of the 8 output pins on the process side.

## 6 Functional description

### 6.1 Serial interface

An integrated SPI peripheral provides a fast communication interface between an external micro-controller and the IC purposing to drive ON/OFF the Power Stage outputs. Daisy chaining is allowed.

It follows the timing requirement established by the synchronous serial communication standard and works up to 20 MHz communication speed.

The communication implemented expects 8-bit data communication; the frame sent by the micro-controller only contains the status of the channels (ON or OFF), while the frame received by the micro-controller is all "0" if no fault event is triggered or all "1" if at least one fault has been triggered on the output stage.

**Table 14. SDI frame**

MSB							LSB
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

**Table 15. SDO frame**

MSB							LSB
0	0	0	0	0	0	0	0

### 6.2 Serial data in (SDI)

This pin is the IC input of the serial command frame (MOSI). SDI is reading on CLK rising edges and , thus, the micro-controller must change SDI state during the CLK falling edges.

The bits sent through the SDI line are shifted in the internal Output Status Register. In daisy chaining communication, the micro-controller keeps the  $\overline{SS}$  low after the 8th bit to allow the shift of the Output Status Register to the SDO line. The bits in the Output Status Register are frozen by the internal logic when the  $\overline{SS}$  goes high.

### 6.3 Serial data out (SDO)

This pin is the IC output of the serial fault frame (MISO). The information on SDO is updated on CLK falling edges, whereas the micro-controller reads the SDO frame on CLK rising edges, as established by standard. At communication start-up, when the  $\overline{SS}$  falling edge is coming, only the first bit of the frame is just available.

SDO pin is tri-stated when the  $\overline{SS}$  signal is high.

In daisy chaining communication the SDO line will transfer the content of the internal Output Status Register after the 8th CLK pulse.

### 6.4 Serial data clock (CLK)

The CLK line is the IC input clock for serial data sampling. SDO is updated on CLK falling edges, and then sampled on the rising edge. The SDI line is sampled on SCK rising edges.

When the  $\overline{SS}$  signal is high (slave not selected), the micro-controller should drive the CLK low (settings for MCU SPI port are CPHA = 0 and CPOL = 0).

### 6.5 Slave select ( $\overline{SS}$ )

The slave select  $\overline{SS}$  signal is used to enable the serial communication shift register. Data is flushed in through the SDI pin and out from the SDO pin only when the  $\overline{SS}$  pin is low. On the  $\overline{SS}$  pin falling edge, the Fault Register (containing IC fault conditions) is frozen, so any changing on the channel status will be latched until the next  $\overline{SS}$  falling edge event, the SDO is enabled and the internal refresh is disabled too. On the  $\overline{SS}$  pin rising edge event, the 8 bits in the Output Status Register are frozen and the outputs of the Process Stage are driven accordingly. If more than 8 bits are flushed into the IC, only the last 8 are evaluated, the other ones are flushed out from the SDO pin after fault condition bits. In this way a proper communication is granted in a daisy chain configuration.

Figure 7. SPI mode diagram

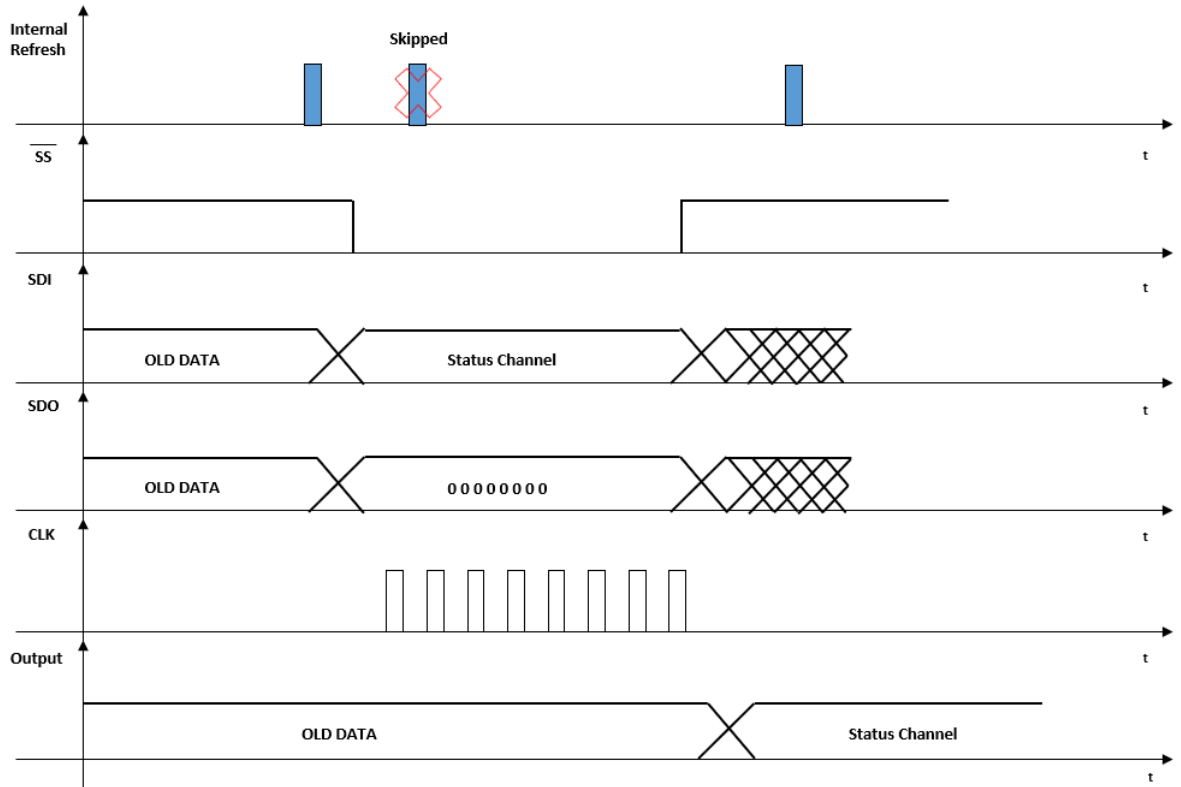


Figure 8. SPI input timing diagram

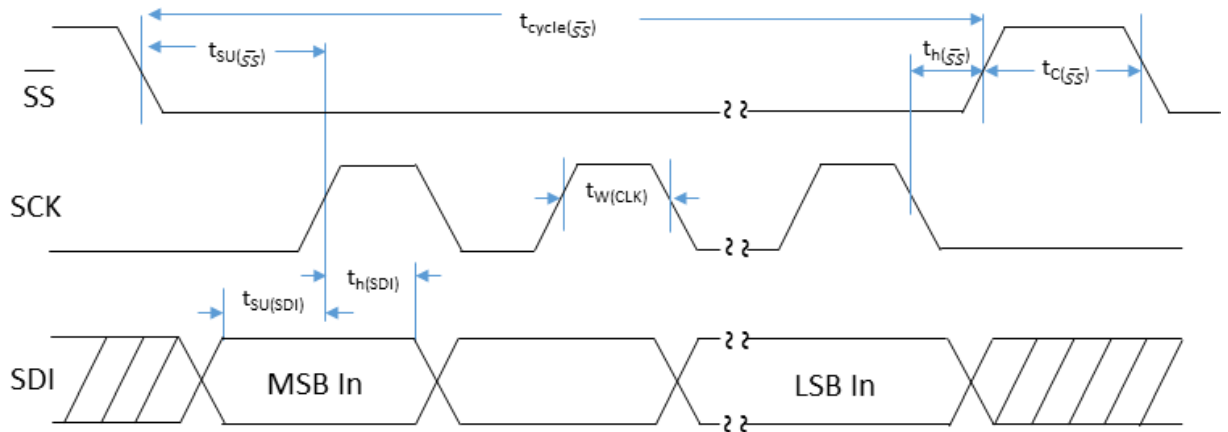
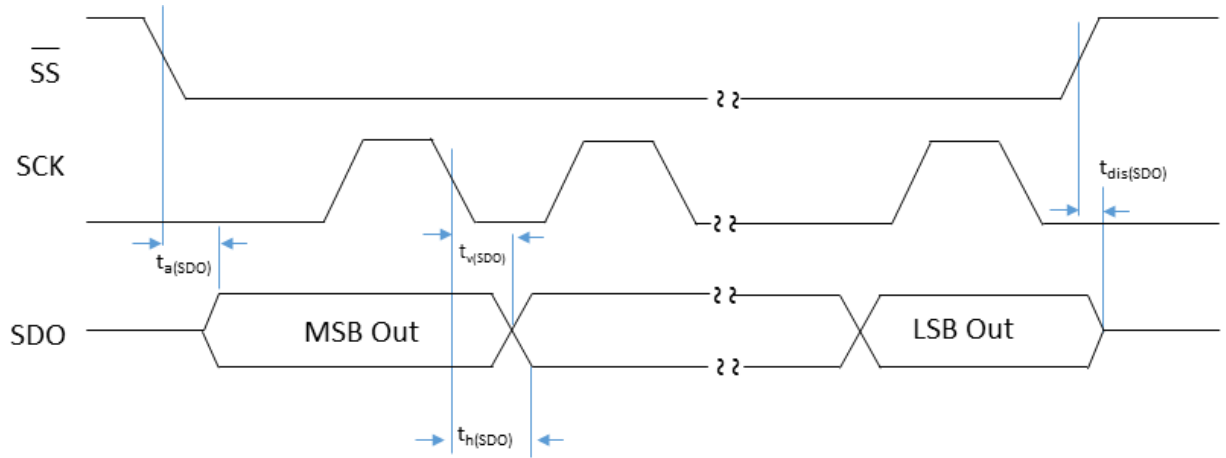


Figure 9. SPI output timing diagram



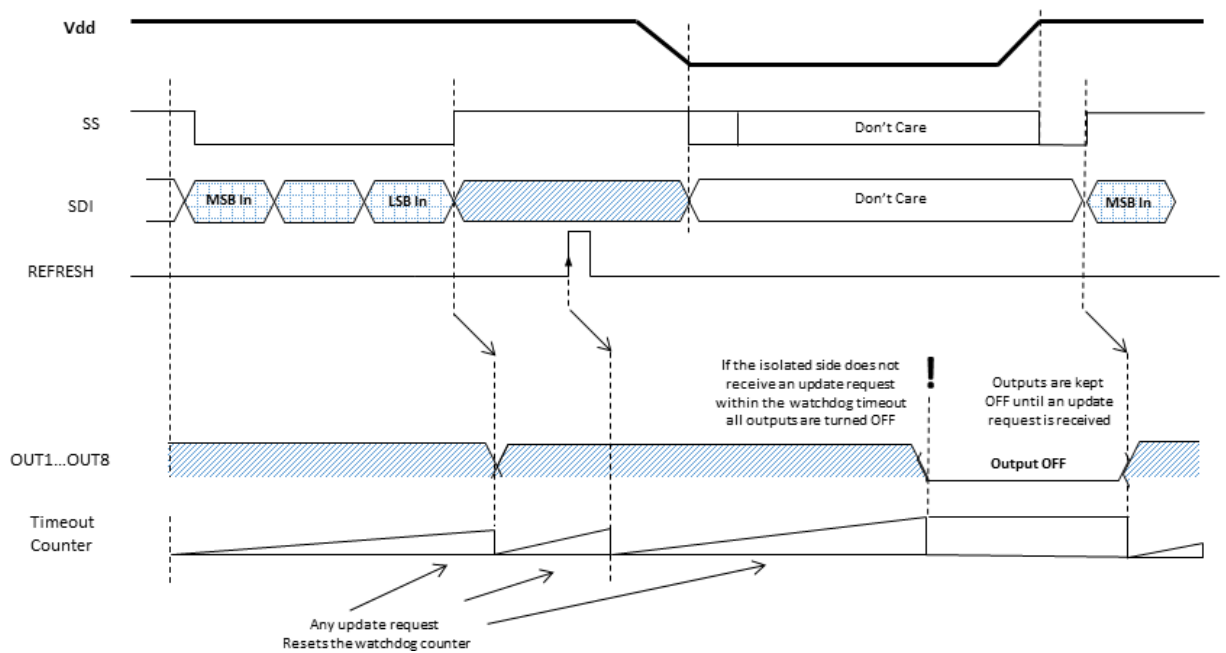
### 6.5.1 Watchdog

The IC is composed by two chips (Logic Stage and Process Stage) supplied by two independent and galvanic isolated sources ( $V_{DD}/GND_{DD}$  and  $V_{CC}/GND_{CC}$  pins, respectively).

The IC provides a watchdog function in order to guarantee a safe condition for the Process Stage when  $V_{DD}$  (or  $GND_{DD}$ ) supply voltage is missing. At the end of each SPI communication, the channel status register is transferred to the Process Stage that both reset an internal timeout counter and turns ON/OFF the outputs accordingly. If the Logic Stage does not update the output status within  $t_{WD}$ , all the outputs of the Process Stage are disabled until a new update request is received (this also happens if SS stays low for longer than  $t_{WD}$ ).

Independently of the SPI communication, the Logic Stage chip periodically sends a refresh signal to the Process Stage chip. The refresh signal is also considered a valid update signal to reset the timeout counter on the Process Stage, so the isolated side watchdog does not protect the system from a failure of the host controller (e.g., MCU freezing).

Figure 10. Watchdog behavior

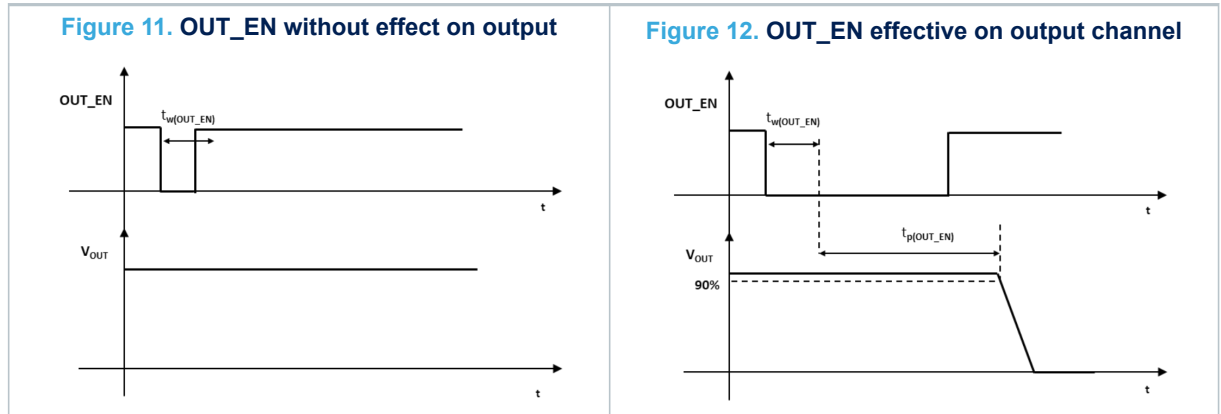




### 6.5.2 Output enable (OUT\_EN)

This pin provides a fast way to disable all the outputs simultaneously. When the OUT\_EN pin is driven low for at least  $t_{W(OUT\_EN)}$ , all eight outputs are disabled. This timing execution is compatible with an external reset push from the operator, safety requirements, and permits, in a PLC system, a micro-controller polling for obtain all internal information during a reset procedure.

Note that the OUT\_EN signal acts as a reset for the internal data register driving the output switches: when the OUT\_EN is low, SDO is pulled down and the output stage is forced OFF. To re-enable SDO, it is necessary to raise the OUT\_EN pin; to enable the output stage again, it is then necessary to raise the OUT\_EN pin and send the desired output configuration by an SPI command.



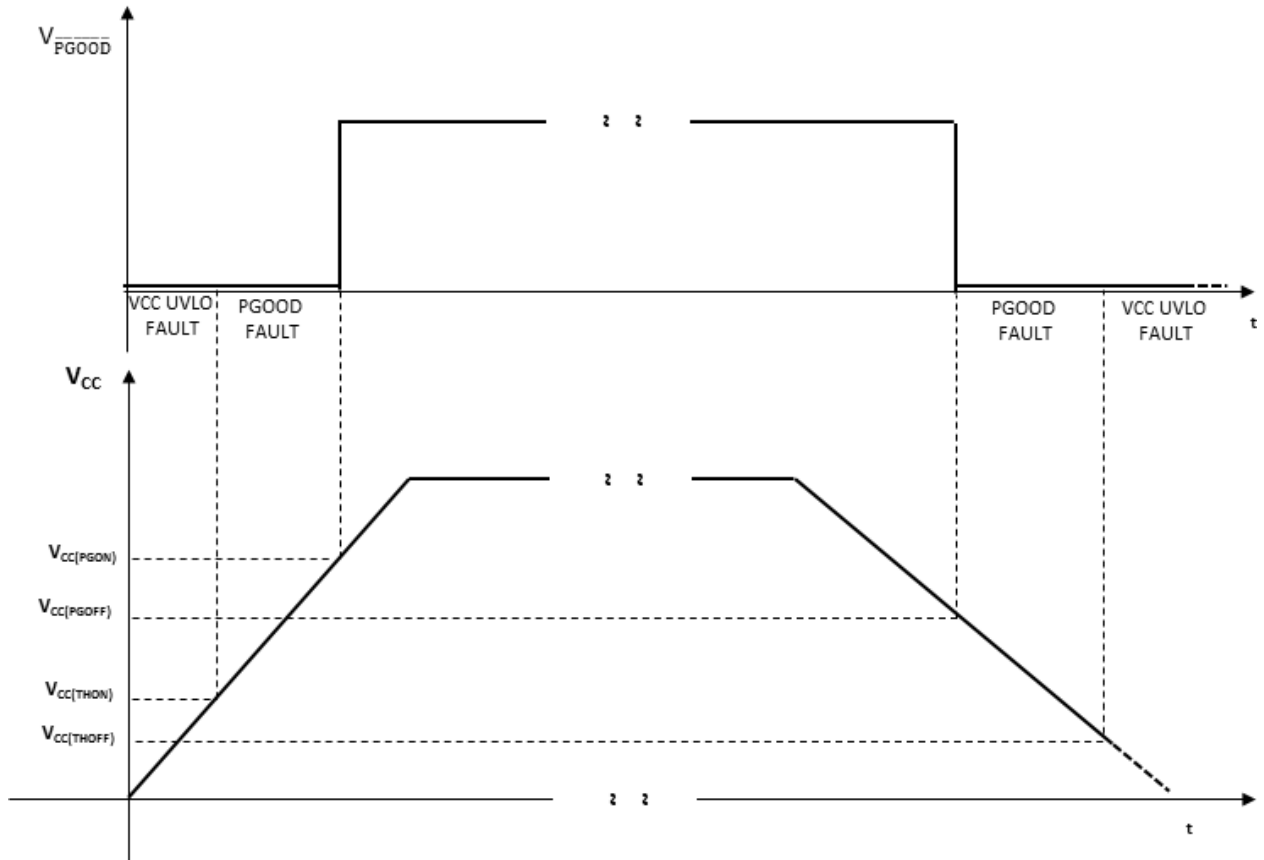
### 6.6 FAULT and PGOOD indications

The  $\overline{FAULT}$  pin is an active low open drain output indicating fault conditions. This pin is activated when at least one of the following conditions occurs:

- Junction over-temperature ( $T_{JX} > T_{JSD}$ ) of one or more channels of the Process Stage or case shut-down protection ( $T_c > T_{csd}$ ) is active.
- No module-8 SPI communication (the number of bits sent through the SDI is not a multiple of 8)
- Internal communication error. In fact, the IC is able to identify (and report to the micro-controller) if any errors occur in the data transmission between isolation. When it occurs, the output stage maintains the previous ON/OFF status.

The PGOOD pin is an active low open drain output indicating if the supply voltage of the Process Stage chip is lower than the internal threshold (see Figure 13).

*Note:* When  $\overline{SS}$  signal is low the transmission between Control Logic Stage and Process Stage is inhibited and the status of PGOOD is not refreshed (PGOOD refresh time < 120  $\mu$ s).

**Figure 13. Power GOOD pin behavior**


## 6.7 Truth table

**Table 16. Truth table**

x = maintain the previous condition.

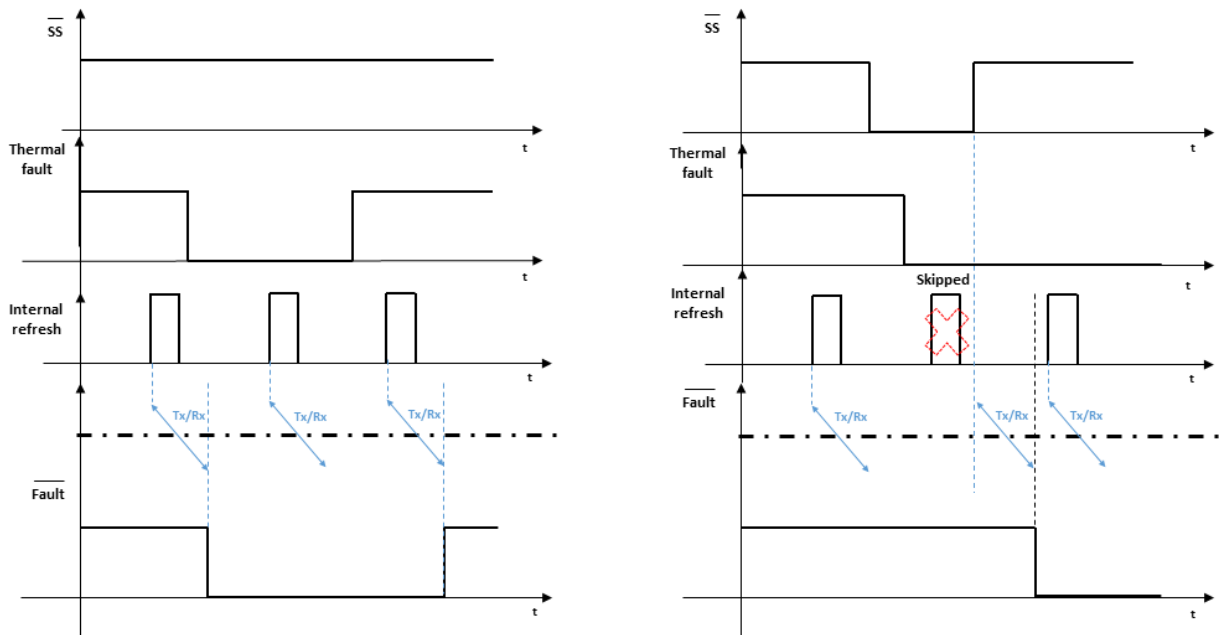
Condition	Status register BIT <sub>x</sub>	OUT <sub>x</sub>	Fault register BIT <sub>x</sub>	FAULT	PGOOD
Normal operation	1	ON	0	H (not active)	H (not active)
	0	OFF	0		
Thermal Junction ( $T_{JX} > T_{JSD}$ )	1	OFF	1	L (active)	Don't care
	0	OFF	1	H (not active)	
Thermal Case $T_C > T_{CSD}$	See Figure 21			H (not active) <sup>(1)</sup>	Don't care
$V_{CC}$ UVLO FAULT (Figure 13)	0	OFF	X	X	L (active)
	1				
POWER GOOD FAULT (Figure 13)	1	ON	Don't care	Don't care	L (active)
	0	OFF			
$V_{DD}$ UVLO (Watchdog)	X	OFF	X	H (not active)	H (not active)
SPI FAULT (module-8 violation)	X	X	Don't care	L (active)	Don't care
Internal communication error	X	X	X	L (active)	Don't care

1. Usually, the thermal case is consequence of thermal junction event latching the FAULT pin low until the thermal junction event resets. If the thermal case is triggered without any thermal junction event (for example in case of very high ambient temperature) then the FAULT pin is not activated

### 6.7.1 Junction over-temperature

The thermal status of the device is updated during each transmission sequence between the two isolated stages. When  $\overline{SS}$  is low, the communication between the two stages is disabled. In this case, the thermal status of the device cannot be updated, and the  $\overline{FAULT}$  indication could be different to the actual status. In any case, the thermal protections of the channel outputs in the Process Stage are always operative.

Figure 14. Thermal status update

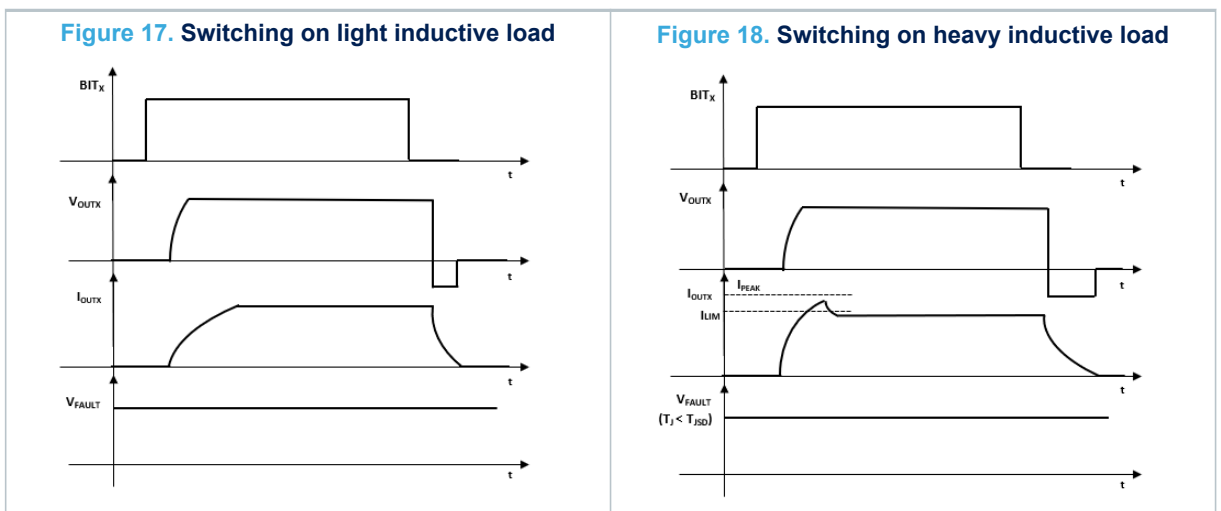
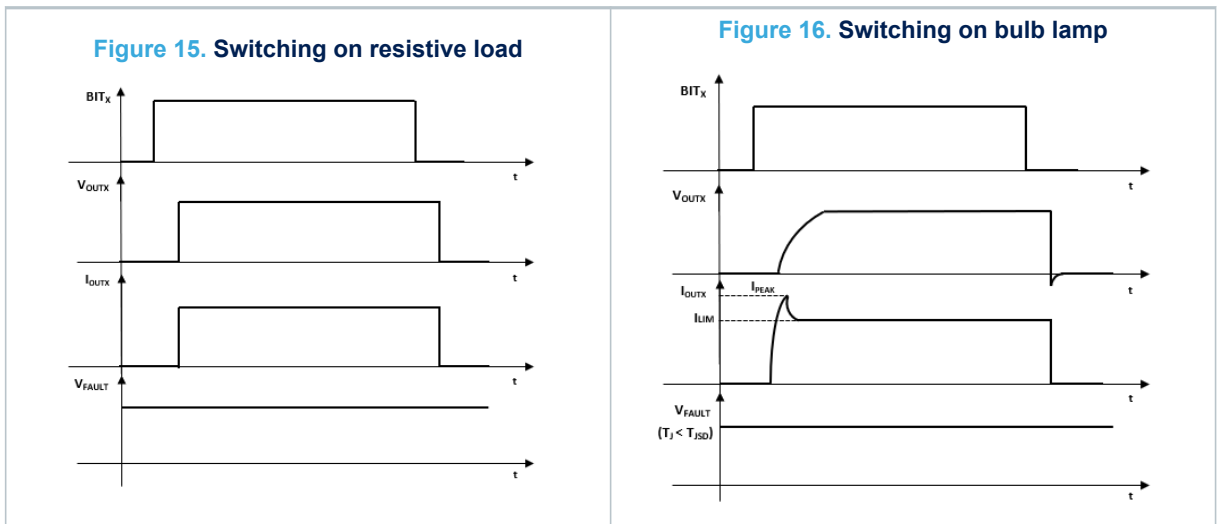


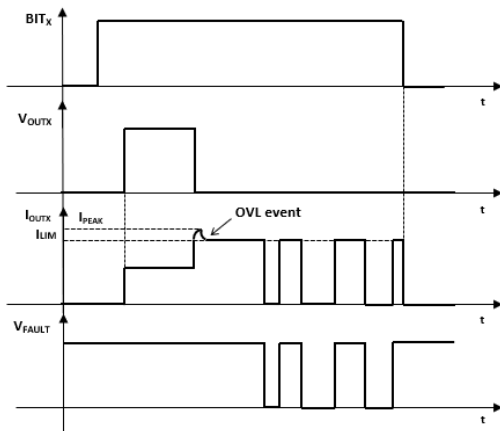
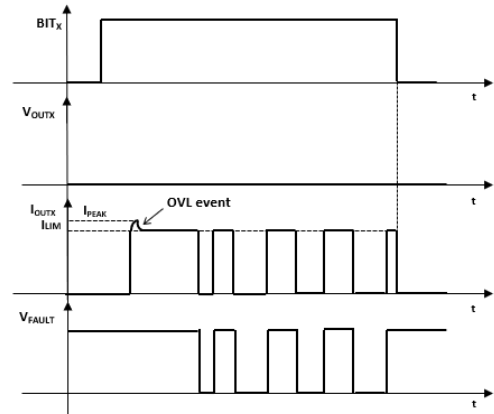
## 7 Power section

### 7.1 Current limitation

The current limitation process is activated when the current sense connected on the output stage measures a current value higher than a fixed threshold. When this condition is verified, the gate voltage is modulated to avoid output current increasing over the limitation value.

The following figures (where BIT<sub>X</sub> is intended as Xth bit of the Output Status Register) show typical output current waveforms with different load conditions.



**Figure 19. Short-circuit (with OVT) during ON state**

**Figure 20. Switching on short-circuit (with OVT)**


## 7.2 Thermal protection

The device is protected against overheating due to overload conditions. During driving period, if the output is overloaded, the device suffers two different thermal stresses, the first one related to the junction, and the second related to the case.

The two faults have different trigger thresholds: the junction protection threshold ( $T_{JSD}$ ) is higher than that of the case protection ( $T_{CSD}$ ). Generally, the first protection that is activated in thermal stress conditions is the junction thermal shutdown. The output is turned off when the temperature is higher than the related threshold and turned back on when it falls below the reset threshold ( $T_{JR}$ ). This behavior continues while the fault on the output is present.

If the thermal protection is active and the temperature of the package increases over the fixed case protection threshold, the case protection is activated, and the output is switched off and back on when the junction temperature of each channel in fault and case temperature are below the respective reset thresholds.

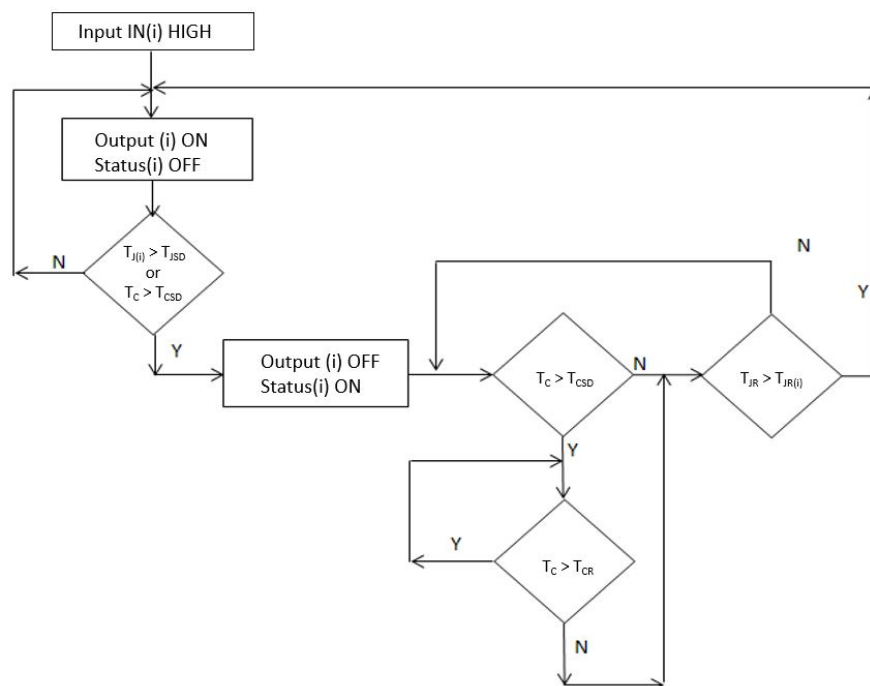
**Figure 21. Thermal protection flowchart**


Figure 22. Thermal protection and fault behavior ( $T_{JSD}$  triggered before  $T_{CSD}$ )

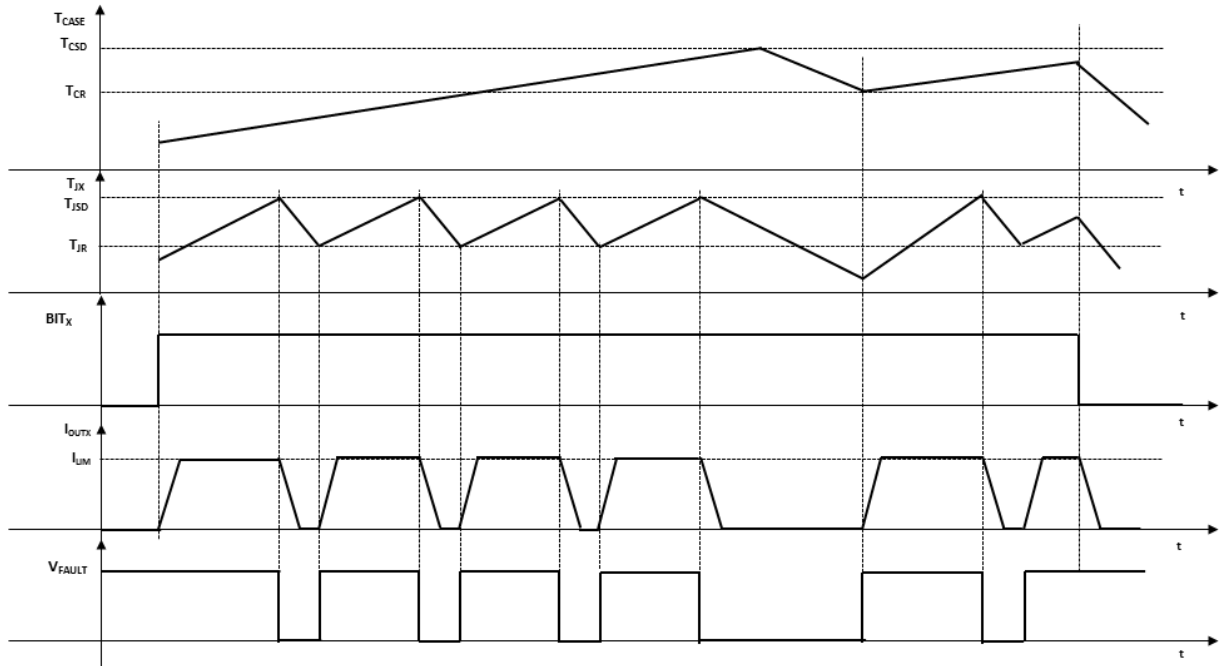
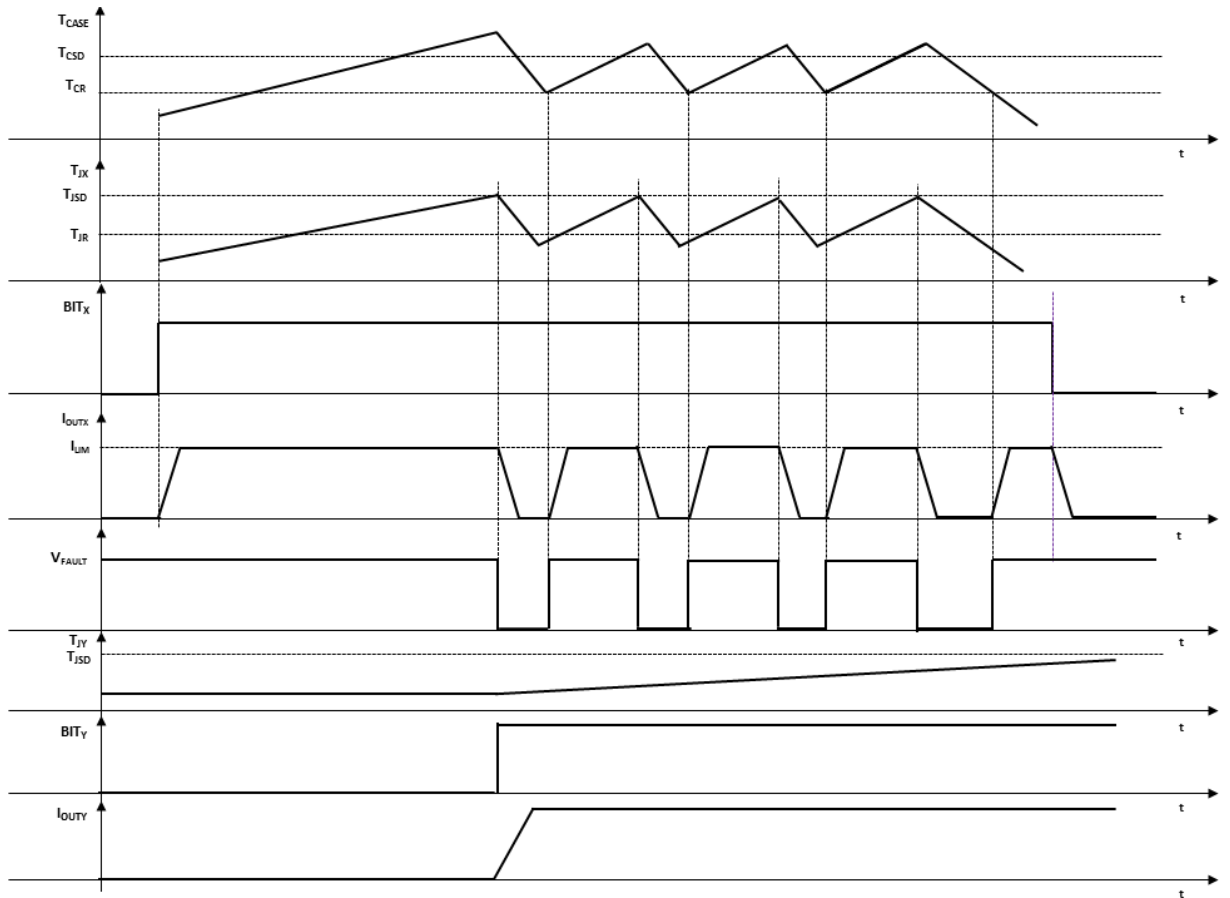


Figure 23. Thermal protection and fault behavior ( $T_{CSD}$  triggered before  $T_{JSD}$ )



## 8 Reverse polarity protection

Reverse polarity protection can be implemented on board using two different solutions (or both, which is recommended):

1. Placing a resistor ( $R_{GND}$ ) between IC GND pin and load GND
2. Placing a diode in parallel to a resistor between IC GND pin and load GND

If option 1 is selected, the minimum resistance value must be selected according to the following equation:

$$R_{GND} \geq \frac{V_{CC}}{I_{GNDCC}} \quad (1)$$

where  $I_{GNDCC}$  is the DC reverse ground pin current and can be found in [Table 2](#).

The power dissipated by  $R_{GND}$  during reverse polarity is:

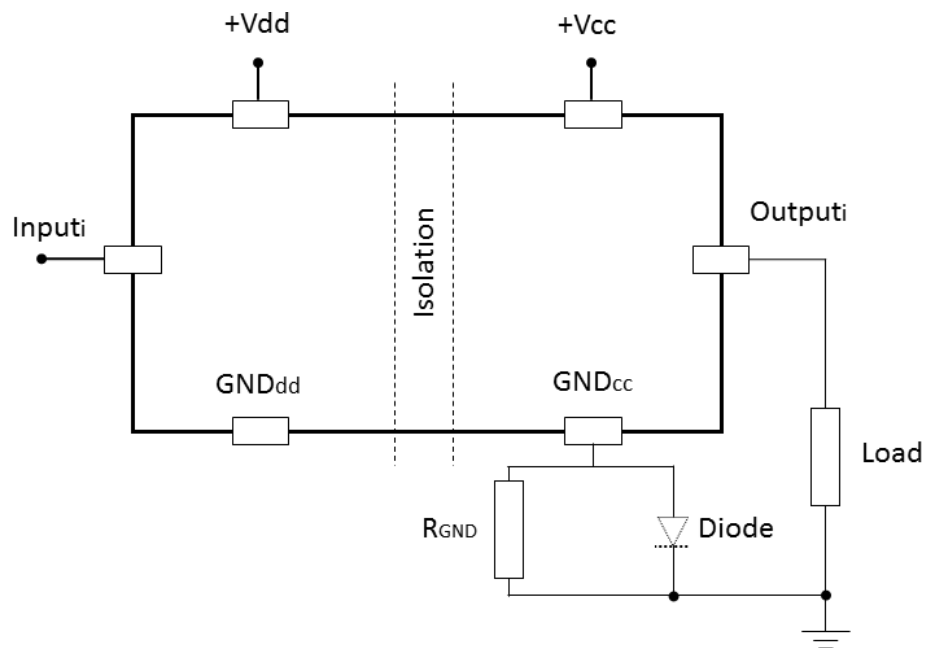
$$P_D = \frac{(V_{CC})^2}{R_{GND}} \quad (2)$$

If option 2 is selected, the diode has to be chosen by taking into account  $V_{RRM} > |V_{CC}|$  and its power dissipation capability:

$$P_D \geq I_S \times V_F \quad (3)$$

*Note:* In normal operation (no reverse polarity), there is a voltage drop ( $\Delta V$ ) between GND of the device and GND of the system. Using option 1,  $\Delta V = R_{GND} \times I_{CC}$ . Using option 2,  $\Delta V = V_F @ (I_F)$ .

**Figure 24. Reverse polarity protection**



*Note:* *Input(i)* is intended as any input pin on logic side.  
 This schematic can be used with any type of load.

## 9 Reverse polarity on VDD

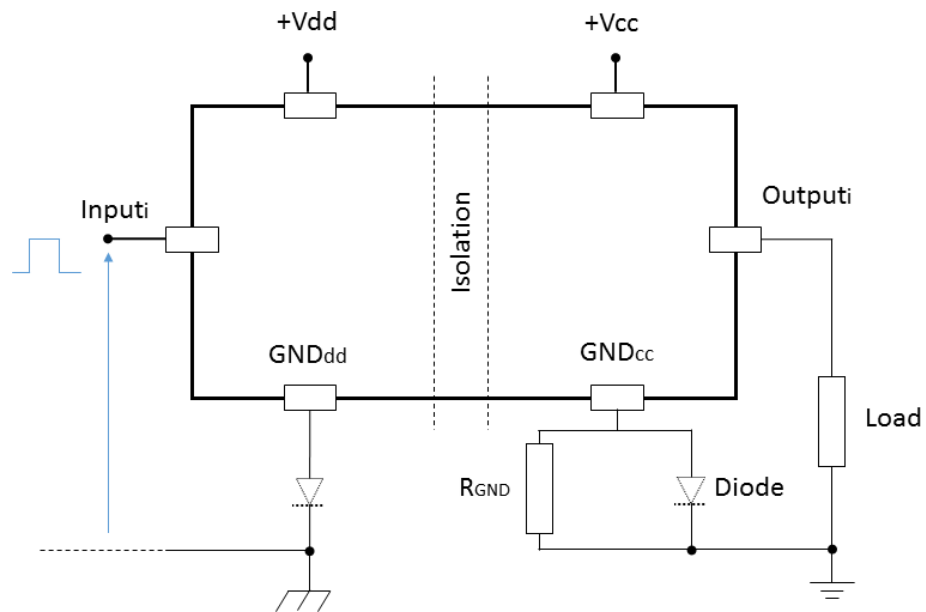
The reverse polarity on  $V_{DD}$  can be implemented on board by placing a diode between the  $GND_{DD}$  pin and GND digital ground.

The diode must be chosen by taking into account  $V_{RRM} > |V_{DD}|$  and its power dissipation capability:

$$P_D \geq I_{DD} \times V_F \quad (4)$$

*Note:* In normal operation (no reverse polarity), there is a voltage drop ( $\Delta V = V_F @ (I_{DD})$ ) between  $GND_{DD}$  of the device and digital ground of the system. In order to guarantee to proper triggering of the input signal,  $\Delta V(\text{max.})$  must result lower than  $V_{IH(\text{MIN})}$ .

**Figure 25.  $V_{DD}$  reverse polarity protection**



*Note:* Input(i) is intended as any input pin on logic side.



## 10 Demagnetization energy

Figure 26. Single pulse demagnetization energy vs. load current (Typical values at  $T_{AMB} = 125\text{ }^{\circ}\text{C}$ )

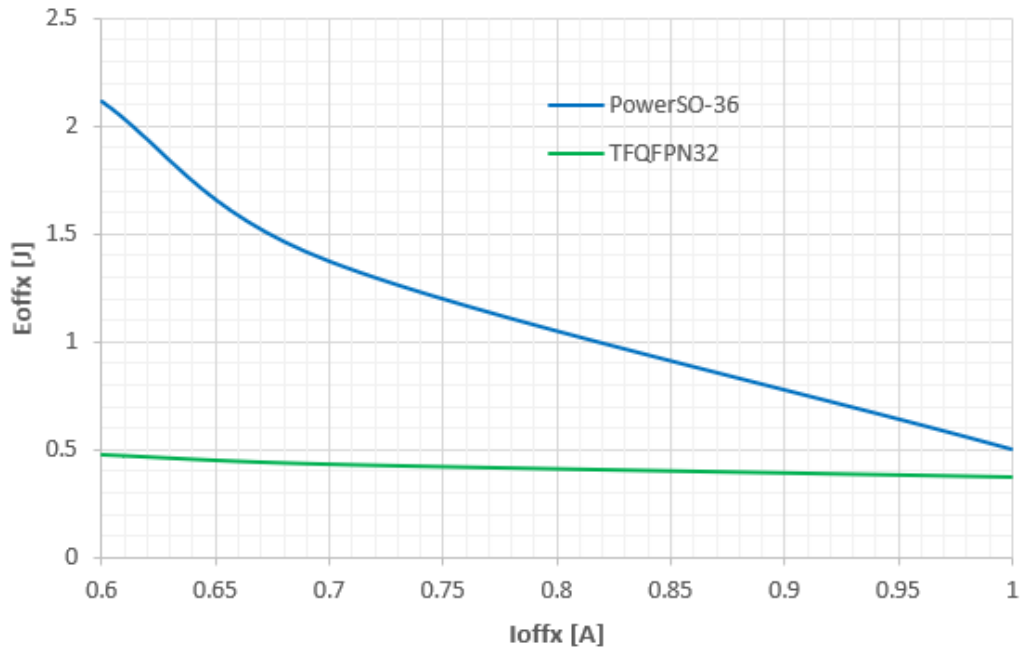


Figure 26 shows the single pulse (not repetitive) demagnetization capability per channel, all channels switched simultaneously

Figure 27. Single pulse inductive load capability vs. load current ( $T_{AMB} = 125\text{ }^{\circ}\text{C}$ )

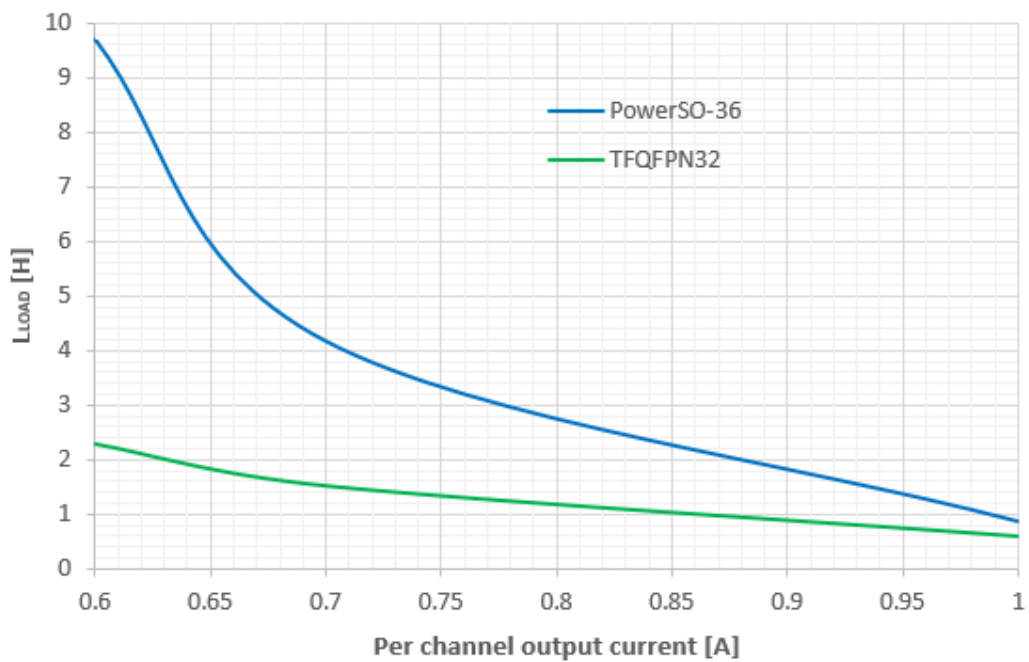
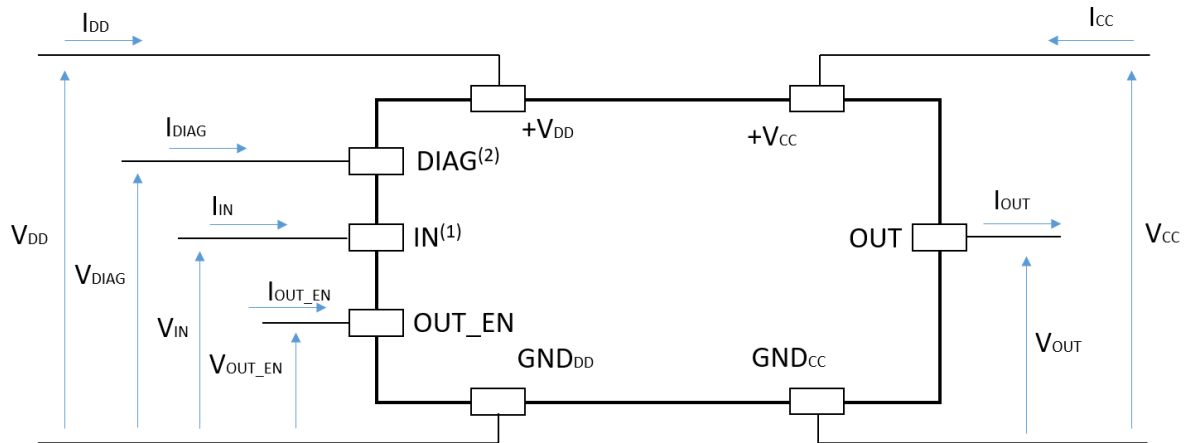


Figure 27 shows the single pulse (not repetitive) inductive load capability per channel, all channels switched simultaneously

## 11 Conventions

### 11.1 Supply voltage and power output conventions

Figure 28. Supply voltage and power output conventions

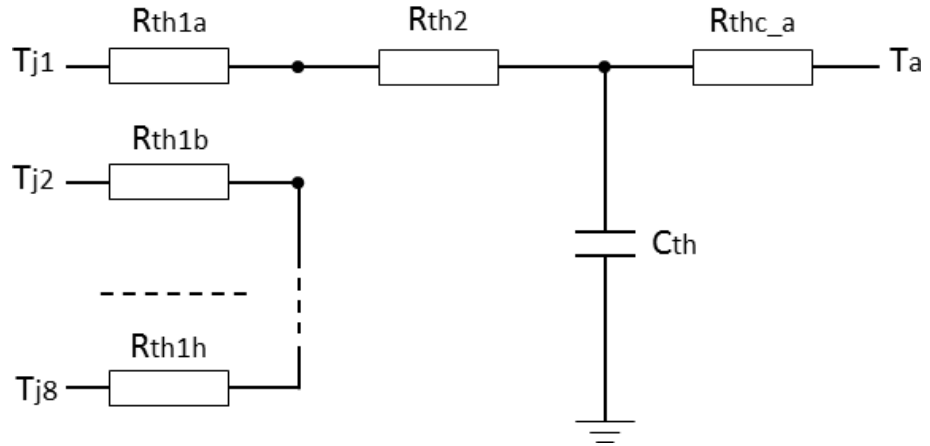


- (1): intended as any input pin on logic side
- (2): intended as any open drain pin on logic side

## 12 Thermal information

### 12.1 Thermal impedance

Figure 29. Simplified thermal model of the process stage

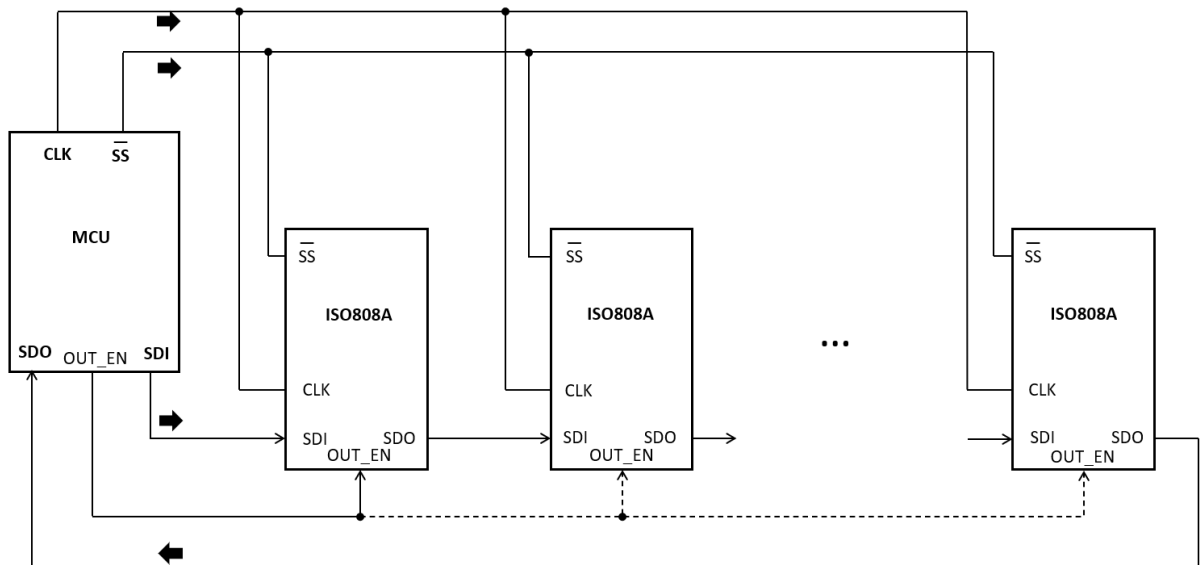


## 13 Daisy chaining

The ISO808A can be daisy-chained by connecting the MOSI port of the microcontroller to the SDI pin of the first IC of the chain; the SDO pin of the first IC of the chain to the SDI pin of the second (and similarly for the next ICs of chain); the SDO pin of the last IC of the chain to the MISO port of the microcontroller.

The  $t_{\text{cycle(SS)}}$  (see Figure 8) must take into account the internal communication timing ( $f_{\text{refresh}}$  and  $t_{\text{WD}}$ ): it is recommended  $t_{\text{cycle(SS)}} (\text{max.}) < 136 \mu\text{s}$ . The maximum number of ICs that can be daisy chained depends on the SPI clock frequency set by the microcontroller.

**Figure 30. Example of daisy-chaining connection**



## 14 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 14.1 PowerSO-36 package information

Figure 31. PowerSO-36 package outline

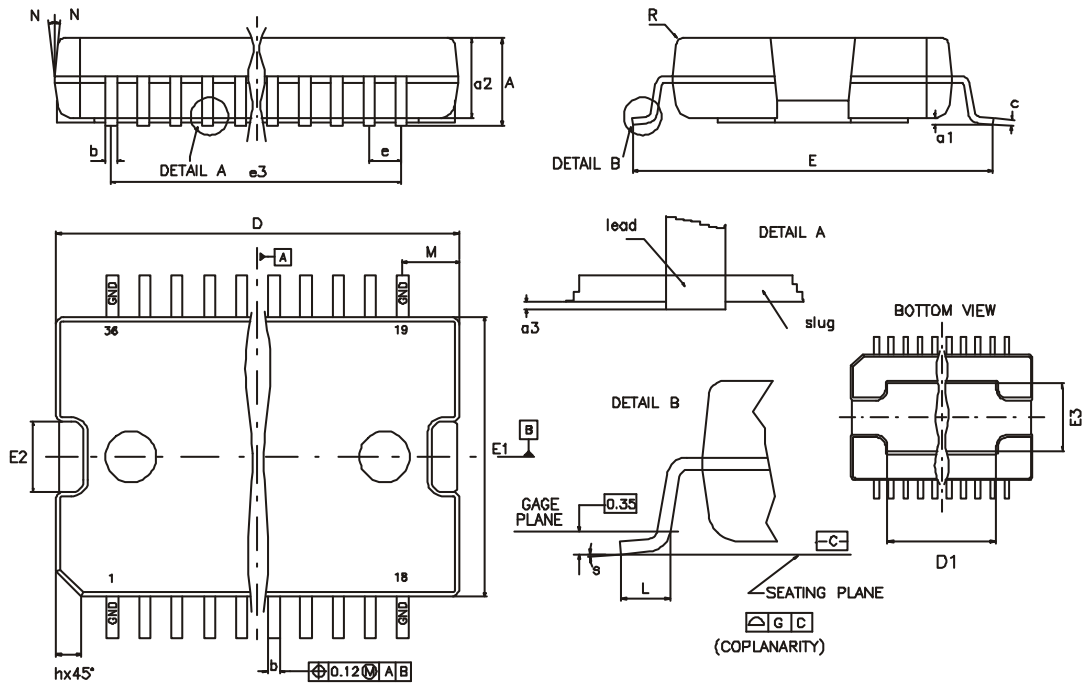


Table 17. PowerSO-36 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			3.6
a1	0.10		0.30
a2			3.30
b	0.22		0.38
c	0.23		0.32
D <sup>(1)</sup>	15.80		16.00
D1	9.40		9.80
E	13.90		14.50
E1 <sup>(1)</sup>	10.90		11.10
E2			2.90
E3	5.80		6.20
e		0.65	
e3		11.05	
G	0		0.10
H	15.50		15.90
h			1.10
L	0.80		1.10
N			10°
S	0°		8°

1. "D" and "E1" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.006"). Critical dimensions are "a3", "E" and "G"

Figure 32. PowerSO-36 suggested footprint

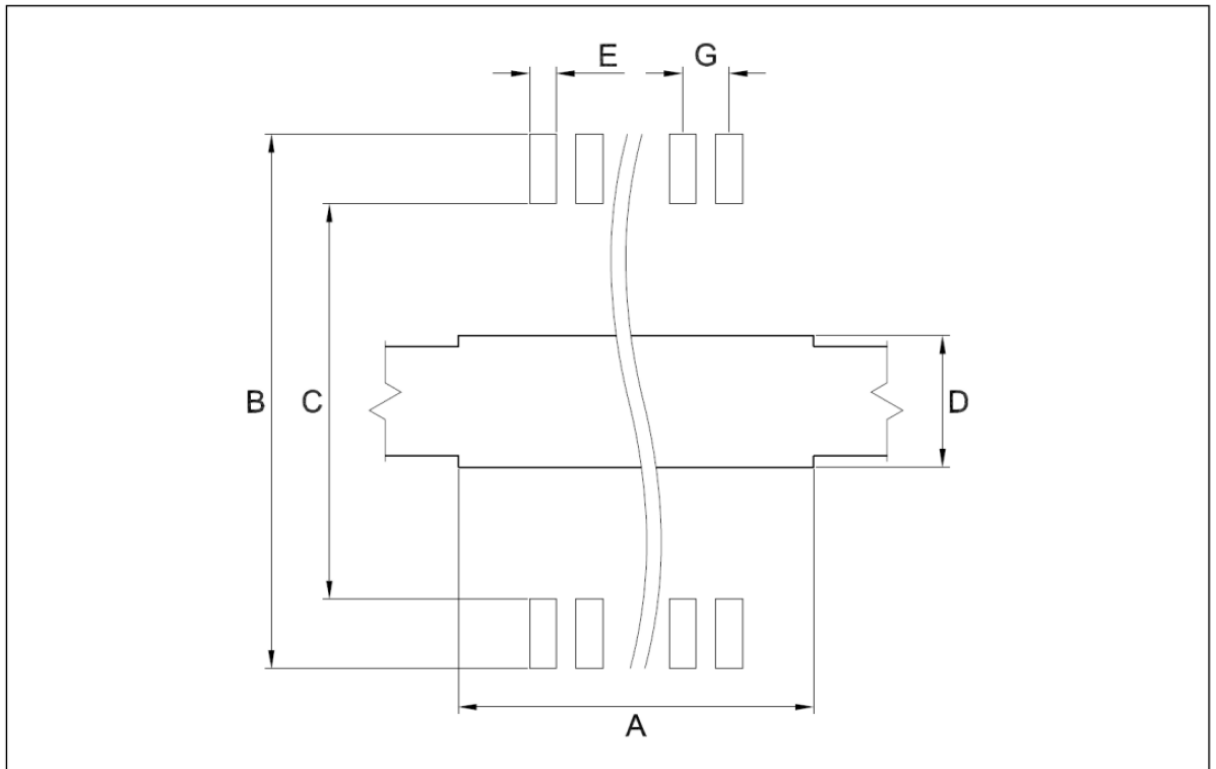


Table 18. PowerSO-36 footprint data

Dim	mm
A	9.5
B	14.7-15.0
C	12.5-12.7
D	6.3
E	0.42
G	0.65

## 14.2 TFQFPN32 package information

Figure 33. TFQFPN32 package outline

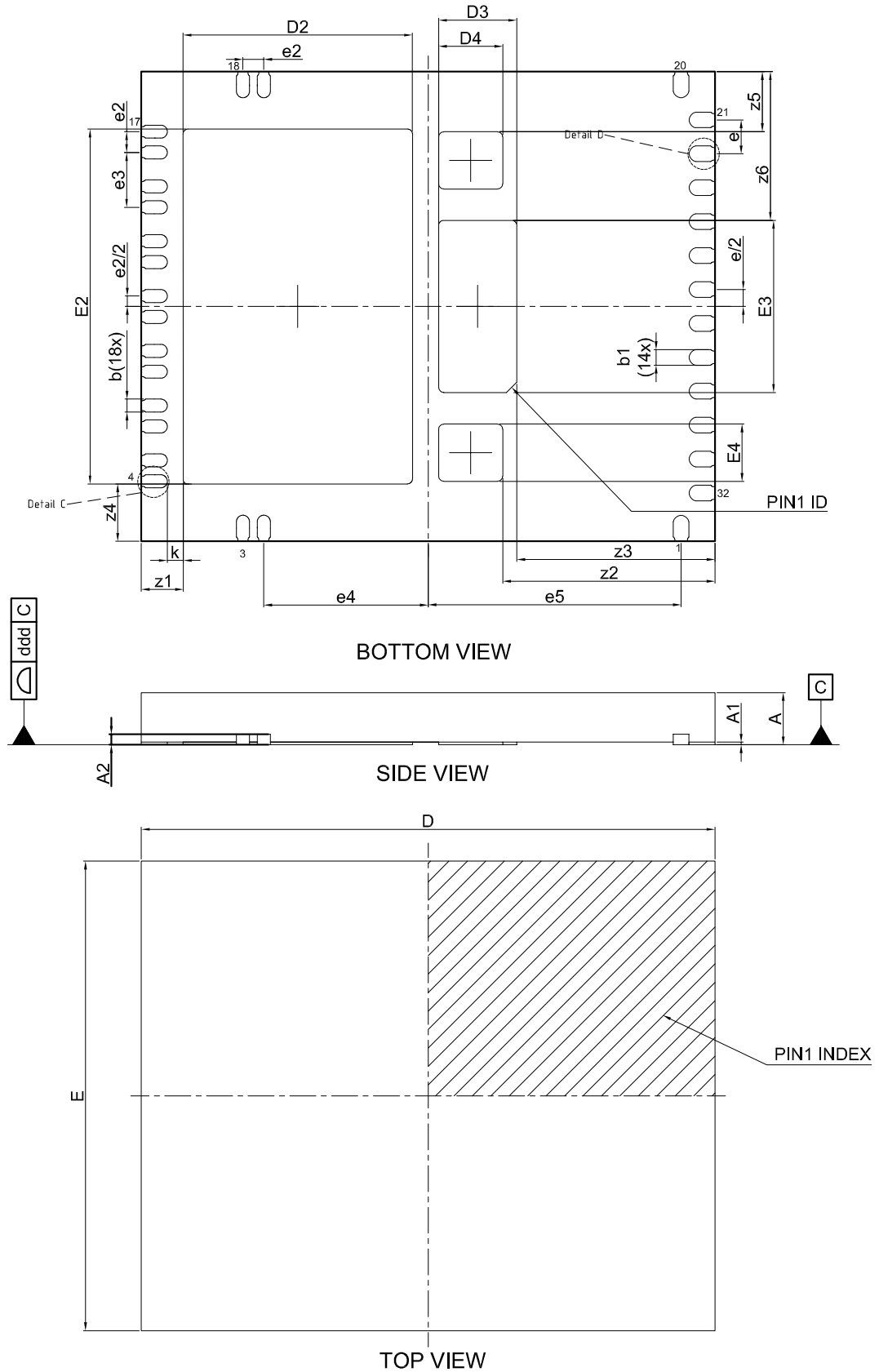




Figure 34. TFQFPN32 package detail outline

Section A-A  
not in scale

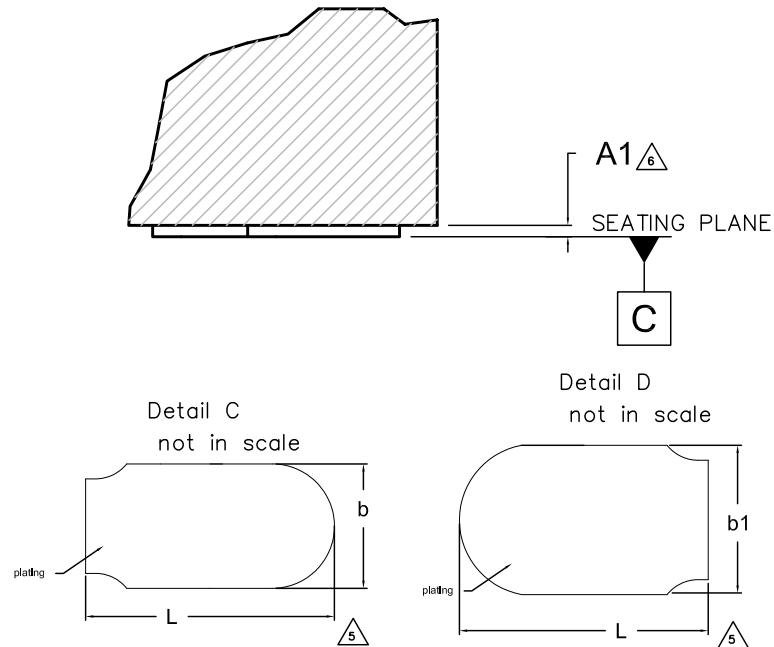
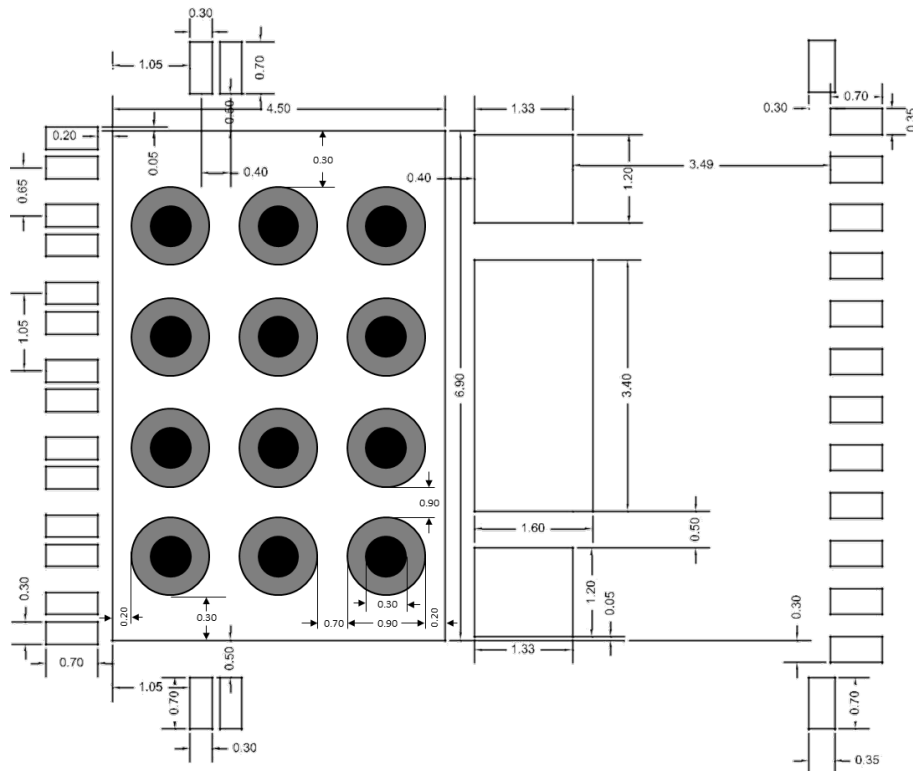


Figure 35. TFQFPN32 suggested footprint (measured in mm)



**Table 19. TFQFPN32 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.95	1.00	1.05
A1	0	-	0.05
A2	-	0.20 REF	-
b <sup>(1)</sup>	0.20	0.25	0.30
b1 <sup>(1)</sup>	0.25	0.30	0.35
D	10.90	11.0	11.10
E <sup>(1)</sup>	8.90	9.00	9.10
D2	4.30	4.40	4.50
E2	6.70	6.80	6.90
D3	1.40	1.50	1.60
E3	3.20	3.30	3.40
D4	1.13	1.23	1.33
E4	1.00	1.10	1.20
e	-	0.65	-
e2	-	0.40	-
e3	-	1.05	-
e4	-	3.15	-
e5	-	4.85	-
k	0	0.30	-
z1	-	0.80	-
z2	-	4.07	-
z3	-	3.80	-
z4	-	1.10	-
z5	-	1.15	-
z6	-	2.85	-
L <sup>(1)</sup>	0.45	0.50	0.55

1. Dimensions "b" and "L" are measured on terminal plating surface.

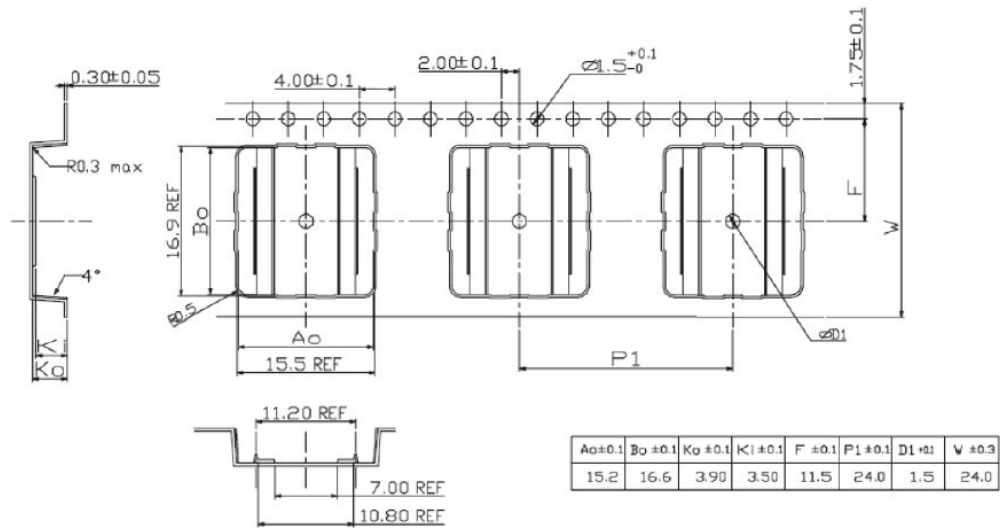
Table 20. Tolerance of form and position

Symbol	Tolerance of form and position	Definition	Notes
Aaa	0.15	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	-
Bbb	0.10	The tolerance that controls the position of the entire terminal pattern with respect to datums A and B. The center of the tolerance zone for each terminal is defined by the basic dimension "e" as related to datum's A and B.	-
Ccc	0.10	The tolerance located parallel to the seating plane in which the top surface of the package must be located.	-
ddd	0.08	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension "e".	This tolerance is normally compounded with tolerance zone defined by bbb.
eee	0.08	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the "coplanarity" of the package terminals.
fff	0.10	The tolerance that controls the position of the exposed metal heat feature. The center of the tolerance zone will be datum's defined by the centerlines of the package body.	-
REF	-	-	No tolerance for A2

## 15 Packing information

### 15.1 PowerSO-36 packing information

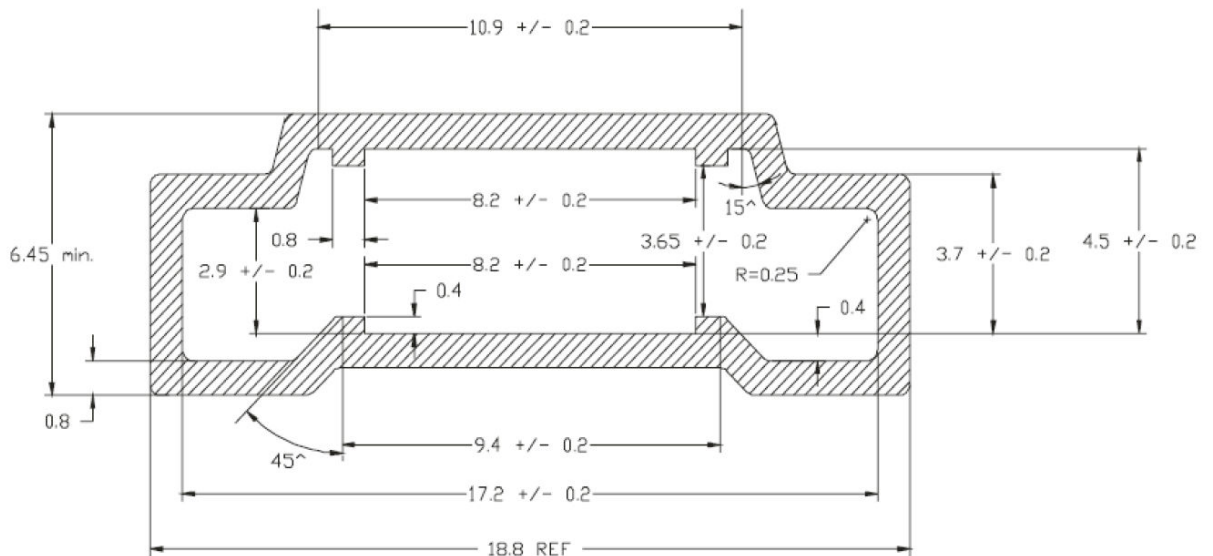
Figure 36. PowerSO-36 carrier tape



NOTE:

- 1) Cumulative tolerance of 10 sprocket holes:  $0.2$  mm
- 2) Camber:  $1$  mm/100 mm max

Figure 37. PowerSO-36 shipping tube



15.2 TFQFPN32 packing information

Figure 38. Tape and reel packing method concept

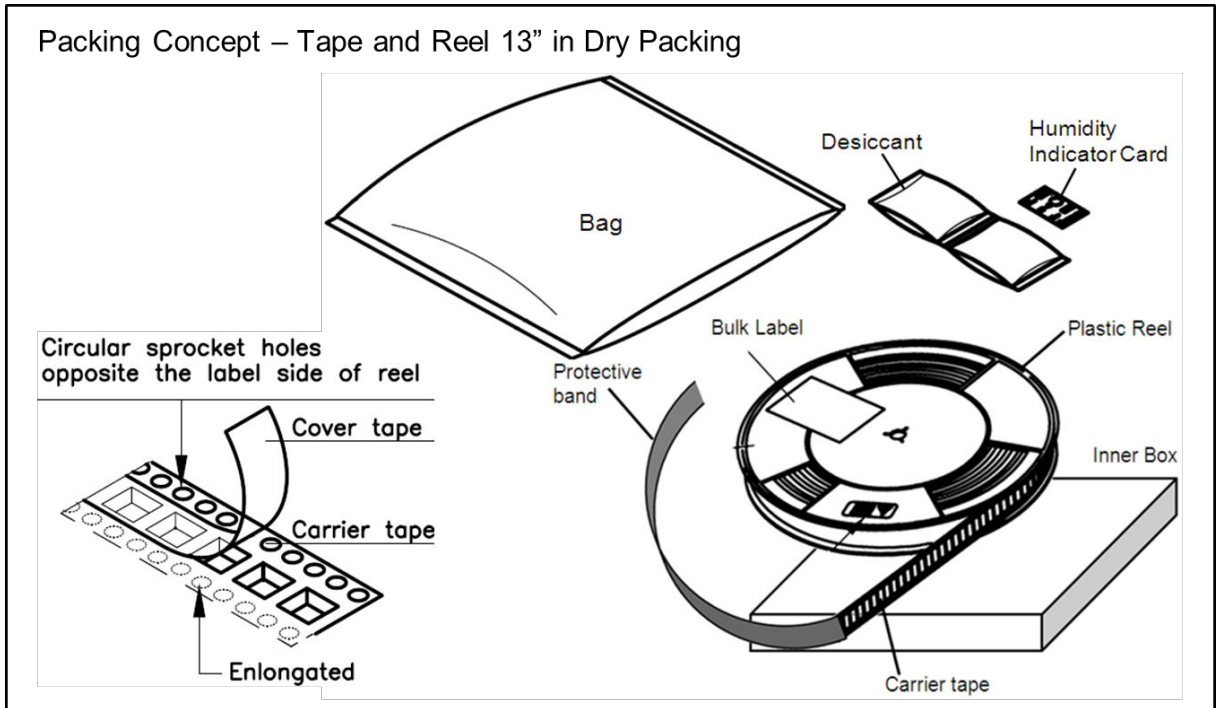


Figure 39. Winding direction

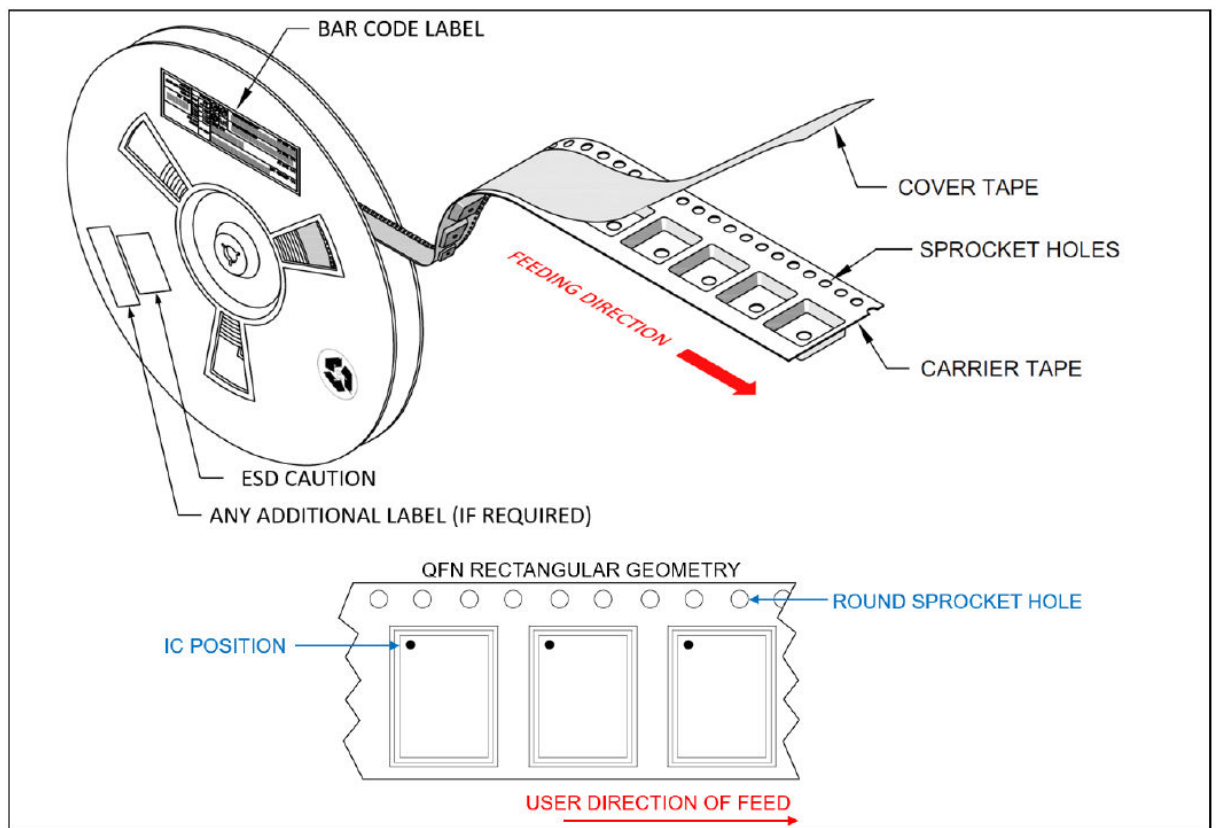


Figure 40. Reel dimensions (as per EIA-481 specification)

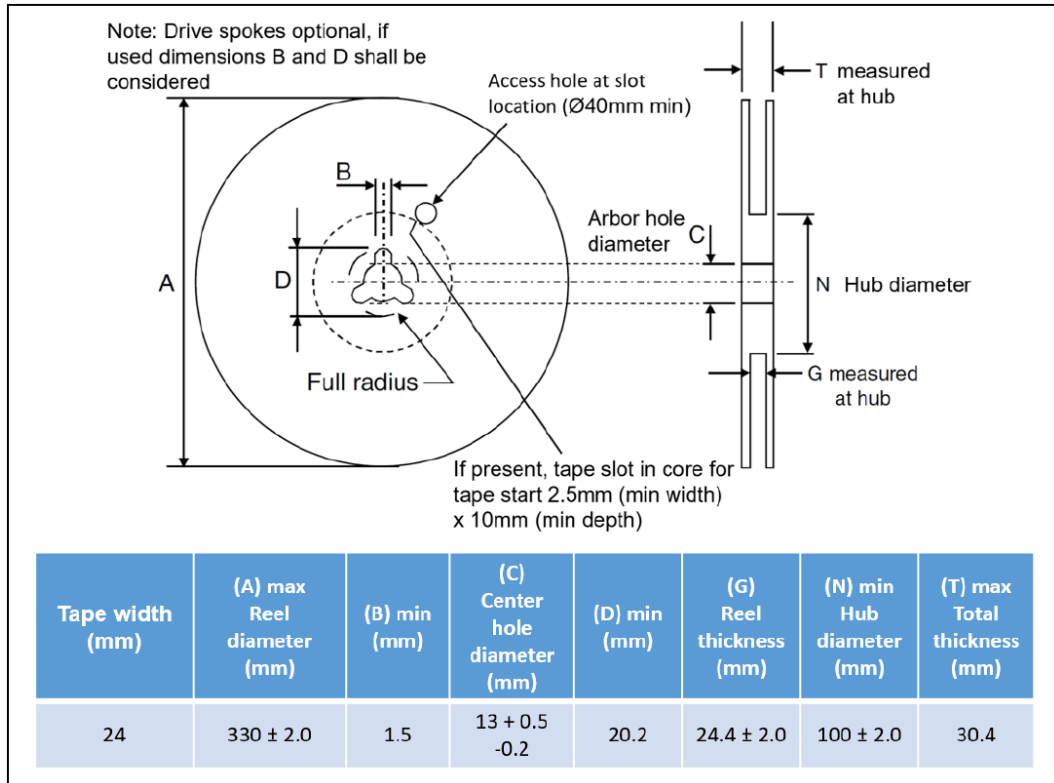


Figure 41. Leader and Trailer dimensions (as per EIA-481 specification)

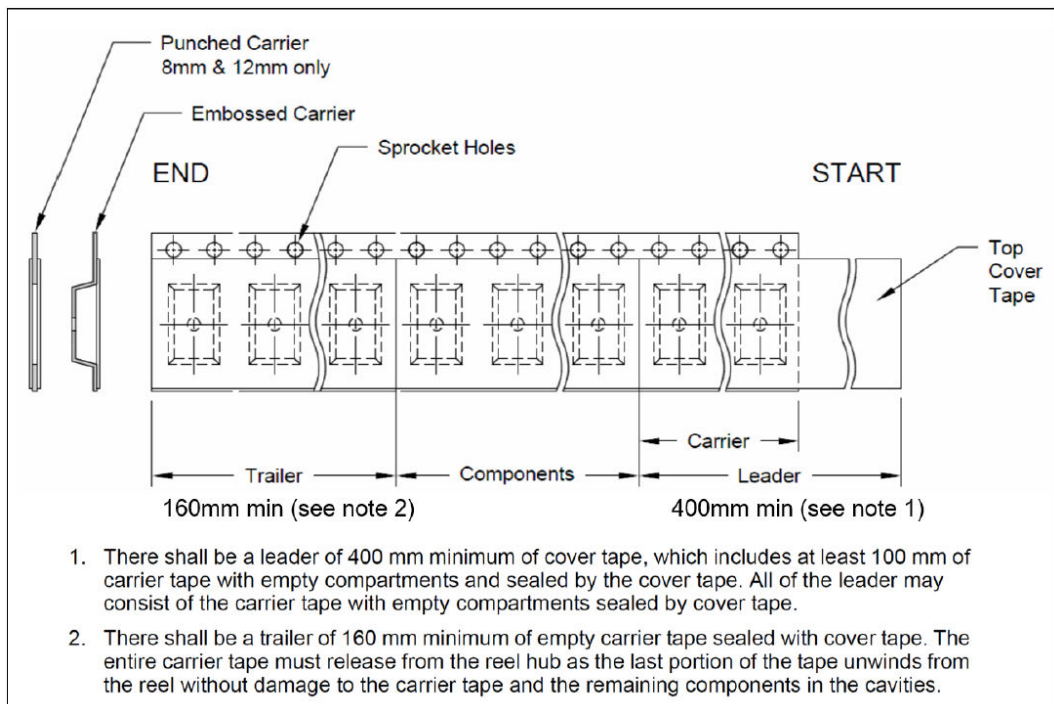
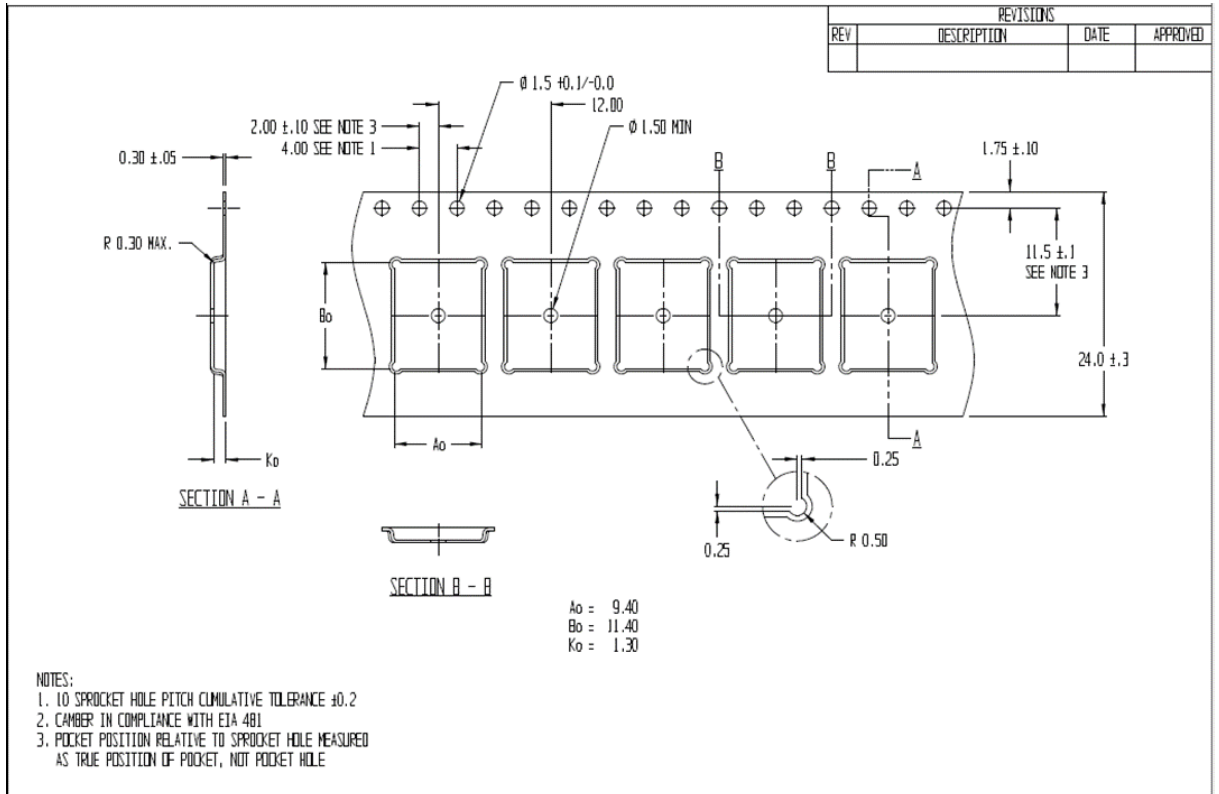


Figure 42. TFQFPN32 carrier tape



## 16 Ordering information

Table 21. Ordering information

Part number	Package	Packaging
ISO808A	PowerSO-36	Tube
ISO808A-1	PowerSO-36	Tube
ISO808ATR	PowerSO-36	Tape and reel
ISO808ATR-1	PowerSO-36	Tape and reel
ISO808AQTR	TFQFPN32	Tape and reel
ISO808AQTR-1	TFQFPN32	Tape and reel



## Revision history

Table 22. Document revision history

Date	Revision	Changes
21-Dec-2022	1	Initial release.
12-Sep-2023	2	Throughout the document added reference to TFQFPN32 package; changed <a href="#">Section ISO808A cover image</a> ; updated table in <a href="#">Section Product status link / summary</a> ; updated <a href="#">Section Features</a> with ISO808AQ/ISO808AQ-1; updated first row in <a href="#">Section Description</a> ; added <a href="#">Figure 3</a> ; updated <a href="#">Table 1</a> ; updated <a href="#">Table 2</a> ; updated <a href="#">Table 3</a> ; updated <a href="#">Table 6</a> , <a href="#">Table 11</a> and <a href="#">Table 12</a> ; updated <a href="#">Figure 15</a> , <a href="#">Figure 16</a> , <a href="#">Figure 17</a> , <a href="#">Figure 18</a> , <a href="#">Figure 19</a> , <a href="#">Figure 20</a> , <a href="#">Figure 22</a> , <a href="#">Figure 23</a> and <a href="#">Figure 26</a> ; added <a href="#">Figure 27</a> ; added <a href="#">Section 14.2</a> and <a href="#">Section 15.2</a> ; updated <a href="#">Table 21</a>
22-Dec-2023	3	Added reference to safety limits certification according IEC 60747-17 in front page and <a href="#">Table 13</a> . Replaced <a href="#">Figure 3</a> and added a new row in <a href="#">Table 1</a> . In <a href="#">Table 3</a> added a footnote regarding the maximum power dissipation based on the package version.
18-Mar-2024	4	Fixed typo on VDE number in the front page
04-Sep-2024	5	Replaced <a href="#">Figure 3</a> ; fixed value of $T_{JR}$ parameter in <a href="#">Table 6</a>

## Contents

<b>1</b>	<b>Block diagram</b> .....	<b>3</b>
<b>2</b>	<b>Pin connection</b> .....	<b>4</b>
<b>3</b>	<b>Absolute maximum ratings</b> .....	<b>6</b>
<b>4</b>	<b>Thermal data</b> .....	<b>7</b>
<b>5</b>	<b>Electrical characteristics</b> .....	<b>8</b>
<b>6</b>	<b>Functional description</b> .....	<b>14</b>
<b>6.1</b>	Serial interface .....	14
<b>6.2</b>	Serial data in (SDI) .....	14
<b>6.3</b>	Serial data out (SDO) .....	14
<b>6.4</b>	Serial data clock (CLK) .....	14
<b>6.5</b>	Slave select ( $\overline{SS}$ ) .....	14
<b>6.5.1</b>	Watchdog .....	16
<b>6.5.2</b>	Output enable (OUT_EN) .....	17
<b>6.6</b>	FAULT and PGOOD indications .....	17
<b>6.7</b>	Truth table .....	18
<b>6.7.1</b>	Junction over-temperature .....	19
<b>7</b>	<b>Power section</b> .....	<b>20</b>
<b>7.1</b>	Current limitation .....	20
<b>7.2</b>	Thermal protection .....	21
<b>8</b>	<b>Reverse polarity protection</b> .....	<b>23</b>
<b>9</b>	<b>Reverse polarity on VDD</b> .....	<b>24</b>
<b>10</b>	<b>Demagnetization energy</b> .....	<b>25</b>
<b>11</b>	<b>Conventions</b> .....	<b>26</b>
<b>11.1</b>	Supply voltage and power output conventions .....	26
<b>12</b>	<b>Thermal information</b> .....	<b>27</b>
<b>12.1</b>	Thermal impedance .....	27
<b>13</b>	<b>Daisy chaining</b> .....	<b>28</b>
<b>14</b>	<b>Package information</b> .....	<b>29</b>
<b>14.1</b>	PowerSO-36 package information .....	29
<b>14.2</b>	TFQFPN32 package information .....	32
<b>15</b>	<b>Packing information</b> .....	<b>36</b>
<b>15.1</b>	PowerSO-36 packing information .....	36
<b>15.2</b>	TFQFPN32 packing information .....	37



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<b>16</b>	<b>Ordering information .....</b>	<b>40</b>
	<b>Revision history .....</b>	<b>41</b>

## List of figures

<b>Figure 1.</b>	Block diagram . . . . .	3
<b>Figure 2.</b>	Pin connection PowerSO-36 (top through view) . . . . .	4
<b>Figure 3.</b>	Pin connection TFQFPN32 (top through view) . . . . .	4
<b>Figure 4.</b>	$R_{DS(on)}$ measurement . . . . .	10
<b>Figure 5.</b>	dV/dT definition . . . . .	10
<b>Figure 6.</b>	td(ON)-td(OFF) definition . . . . .	11
<b>Figure 7.</b>	SPI mode diagram . . . . .	15
<b>Figure 8.</b>	SPI input timing diagram . . . . .	15
<b>Figure 9.</b>	SPI output timing diagram . . . . .	16
<b>Figure 10.</b>	Watchdog behavior . . . . .	16
<b>Figure 11.</b>	OUT_EN without effect on output . . . . .	17
<b>Figure 12.</b>	OUT_EN effective on output channel . . . . .	17
<b>Figure 13.</b>	Power GOOD pin behavior . . . . .	18
<b>Figure 14.</b>	Thermal status update . . . . .	19
<b>Figure 15.</b>	Switching on resistive load . . . . .	20
<b>Figure 16.</b>	Switching on bulb lamp . . . . .	20
<b>Figure 17.</b>	Switching on light inductive load . . . . .	20
<b>Figure 18.</b>	Switching on heavy inductive load . . . . .	20
<b>Figure 19.</b>	Short-circuit (with OVT) during ON state . . . . .	21
<b>Figure 20.</b>	Switching on short-circuit (with OVT) . . . . .	21
<b>Figure 21.</b>	Thermal protection flowchart . . . . .	21
<b>Figure 22.</b>	Thermal protection and fault behavior ( $T_{JSD}$ triggered before $T_{CSD}$ ) . . . . .	22
<b>Figure 23.</b>	Thermal protection and fault behavior ( $T_{CSD}$ triggered before $T_{JSD}$ ) . . . . .	22
<b>Figure 24.</b>	Reverse polarity protection . . . . .	23
<b>Figure 25.</b>	$V_{DD}$ reverse polarity protection . . . . .	24
<b>Figure 26.</b>	Single pulse demagnetization energy vs. load current (Typical values at $T_{AMB} = 125\text{ °C}$ ) . . . . .	25
<b>Figure 27.</b>	Single pulse inductive load capability vs. load current ( $T_{AMB} = 125\text{ °C}$ ) . . . . .	25
<b>Figure 28.</b>	Supply voltage and power output conventions . . . . .	26
<b>Figure 29.</b>	Simplified thermal model of the process stage . . . . .	27
<b>Figure 30.</b>	Example of daisy-chaining connection . . . . .	28
<b>Figure 31.</b>	PowerSO-36 package outline . . . . .	29
<b>Figure 32.</b>	PowerSO-36 suggested footprint . . . . .	31
<b>Figure 33.</b>	TFQFPN32 package outline . . . . .	32
<b>Figure 34.</b>	TFQFPN32 package detail outline . . . . .	33
<b>Figure 35.</b>	TFQFPN32 suggested footprint (measured in mm) . . . . .	33
<b>Figure 36.</b>	PowerSO-36 carrier tape . . . . .	36
<b>Figure 37.</b>	PowerSO-36 shipping tube . . . . .	36
<b>Figure 38.</b>	Tape and reel packing method concept . . . . .	37
<b>Figure 39.</b>	Winding direction . . . . .	37
<b>Figure 40.</b>	Reel dimensions (as per EIA-481 specification) . . . . .	38
<b>Figure 41.</b>	Leader and Trailer dimensions (as per EIA-481 specification) . . . . .	38
<b>Figure 42.</b>	TFQFPN32 carrier tape . . . . .	39

## List of tables

<b>Table 1.</b>	Pin description . . . . .	5
<b>Table 2.</b>	Absolute maximum ratings . . . . .	6
<b>Table 3.</b>	Thermal data . . . . .	7
<b>Table 4.</b>	Power section . . . . .	8
<b>Table 5.</b>	Digital supply voltage . . . . .	8
<b>Table 6.</b>	Diagnostic pin and output protection function . . . . .	9
<b>Table 7.</b>	Power switching characteristics ( $V_{CC} = 24\text{ V}$ ; $R_{LOAD} = 48\ \Omega$ ; $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$ ) . . . . .	9
<b>Table 8.</b>	Logic inputs and output . . . . .	11
<b>Table 9.</b>	Serial interface timings ( $V_{DD} = 5\text{ V}$ ; $V_{CC} = 24\text{ V}$ ; $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$ ) . . . . .	12
<b>Table 10.</b>	Internal communication timings ( $V_{DD} = 5\text{ V}$ ; $V_{CC} = 24\text{ V}$ ; $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$ ) . . . . .	12
<b>Table 11.</b>	Insulation and safety-related specifications . . . . .	12
<b>Table 12.</b>	Insulation characteristics . . . . .	13
<b>Table 13.</b>	Safety limits . . . . .	13
<b>Table 14.</b>	SDI frame . . . . .	14
<b>Table 15.</b>	SDO frame . . . . .	14
<b>Table 16.</b>	Truth table . . . . .	18
<b>Table 17.</b>	PowerSO-36 package mechanical data . . . . .	30
<b>Table 18.</b>	PowerSO-36 footprint data . . . . .	31
<b>Table 19.</b>	TFQFPN32 package mechanical data . . . . .	34
<b>Table 20.</b>	Tolerance of form and position . . . . .	35
<b>Table 21.</b>	Ordering information . . . . .	40
<b>Table 22.</b>	Document revision history . . . . .	41

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