

## Power MOSFET

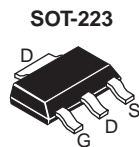
PRODUCT SUMMARY		
$V_{DS}$ (V)	650	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	8.4
$Q_g$ (Max.) (nC)	18	
$Q_{gs}$ (nC)	3.0	
$Q_{gd}$ (nC)	8.9	
Configuration	Single	

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC



Available  
**RoHS\***  
COMPLIANT  
HALOGEN  
**FREE**  
Available



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$		650	V
Gate-Source Voltage	$V_{GS}$		$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	1.2	A
		$T_C = 100\text{ }^\circ\text{C}$	0.8	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$		4.8	W/ $^\circ\text{C}$
Linear Derating Factor			0.33	
Linear Derating Factor (PCB Mount) <sup>e</sup>			0.020	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$		74	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$		2.0	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$		4.2	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$		3	W
	$T_A = 25\text{ }^\circ\text{C}$		0.02	
Peak Diode Recovery $dV/dt^c$	$dV/dt$		3.0	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		260 <sup>d</sup>	

#### Notes

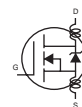

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 37\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 2.0\text{ A}$  (see fig. 12).
- $I_{SD} \leq 2.0\text{ A}$ ,  $dI/dt \leq 40\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	$R_{thJA}$	-	-	110	°C/W	
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	-	50		
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	3.0		

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		650	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.88	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	100	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1.2\text{ A}^b$	-	8.4	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 1.2\text{ A}$		1.4	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	350	-	pF
Output Capacitance	$C_{oss}$			-	48	-	
Reverse Transfer Capacitance	$C_{rss}$			-	8.6	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 2.0\text{ A}, V_{DS} = 360\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	18	nC
Gate-Source Charge	$Q_{gs}$			-	-	3.0	
Gate-Drain Charge	$Q_{gd}$			-	-	8.9	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 2.0\text{ A}, R_g = 18\text{ }\Omega, R_D = 135\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	10	-	ns
Rise Time	$t_r$			-	23	-	
Turn-Off Delay Time	$t_{d(off)}$			-	30	-	
Fall Time	$t_f$			-	25	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode 		-	-	2.0	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	8.0	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 2.0\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.6	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 2.0\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	290	580	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.67	1.3	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\text{ }\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

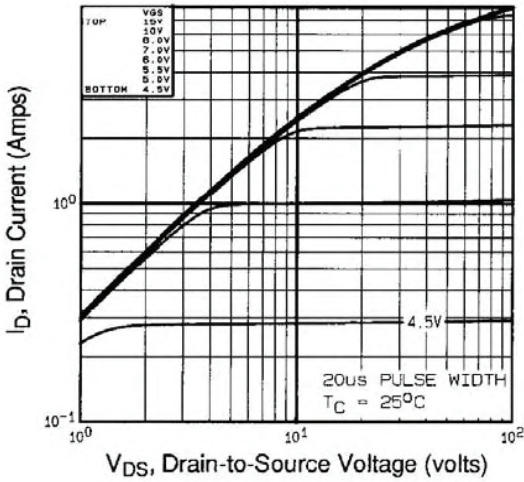


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$

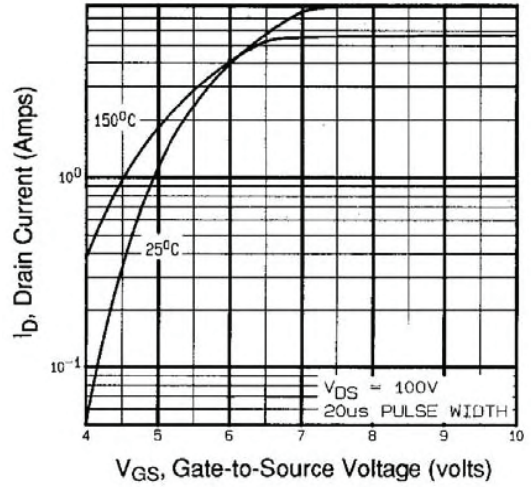


Fig. 3 - Typical Transfer Characteristics

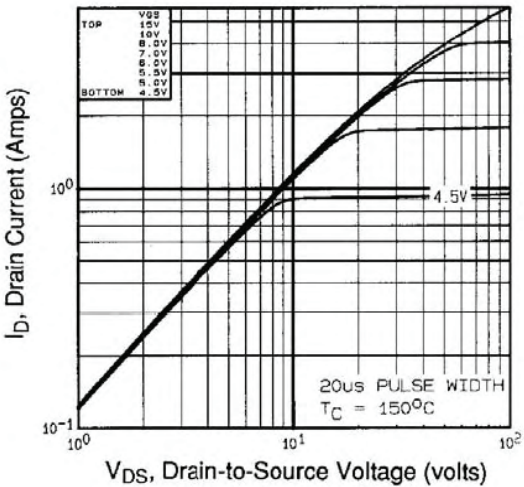


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

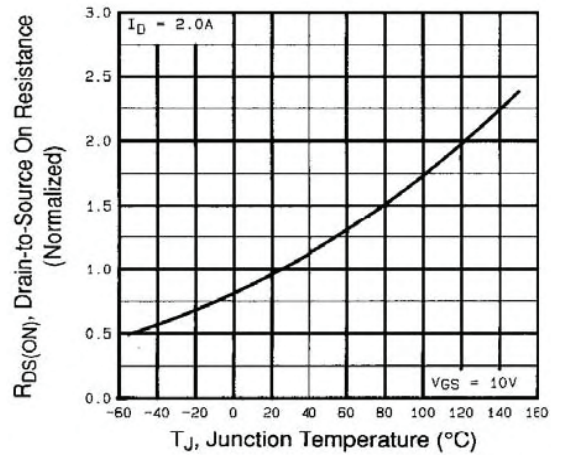


Fig. 4 - Normalized On-Resistance vs. Temperature

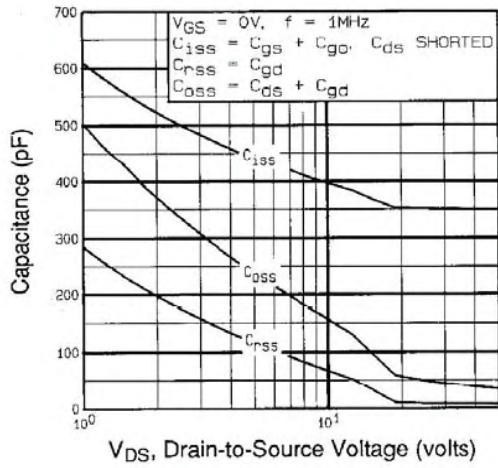


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

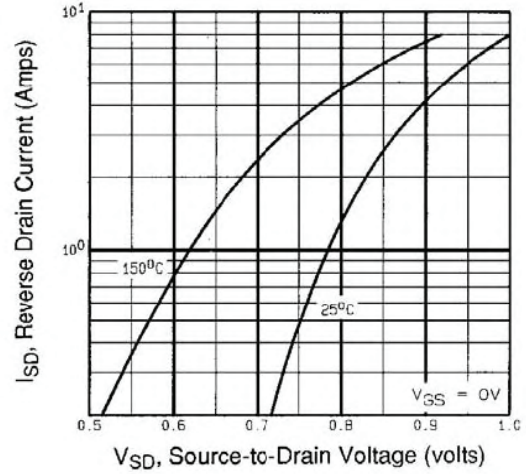


Fig. 7 - Typical Source-Drain Diode Forward Voltage

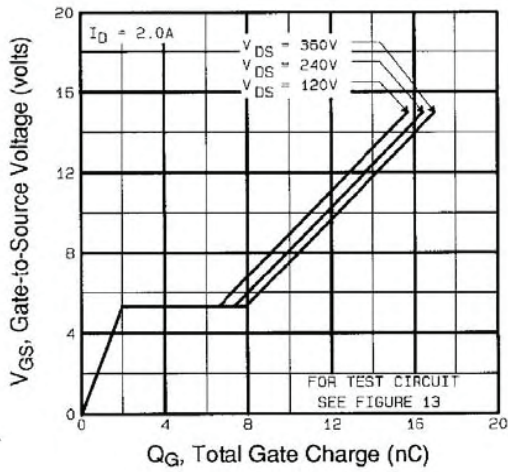


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

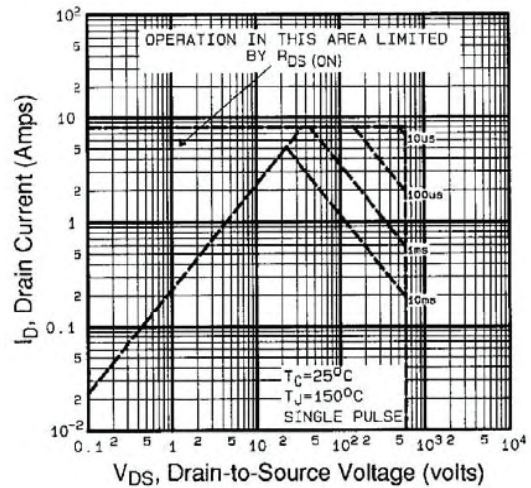


Fig. 8 - Maximum Safe Operating Area

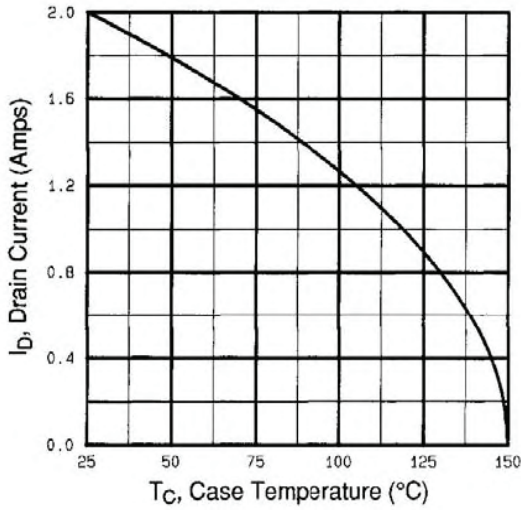


Fig. 9 - Maximum Drain Current vs. Case Temperature

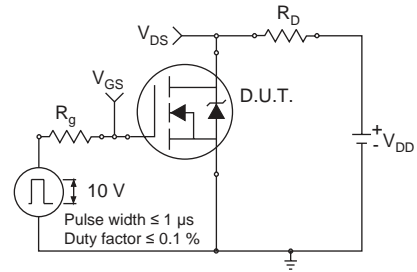


Fig. 10a - Switching Time Test Circuit

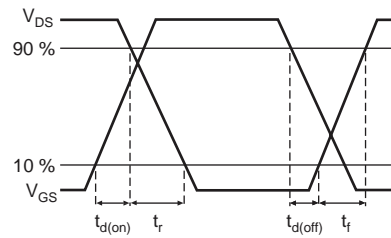


Fig. 10b - Switching Time Waveforms

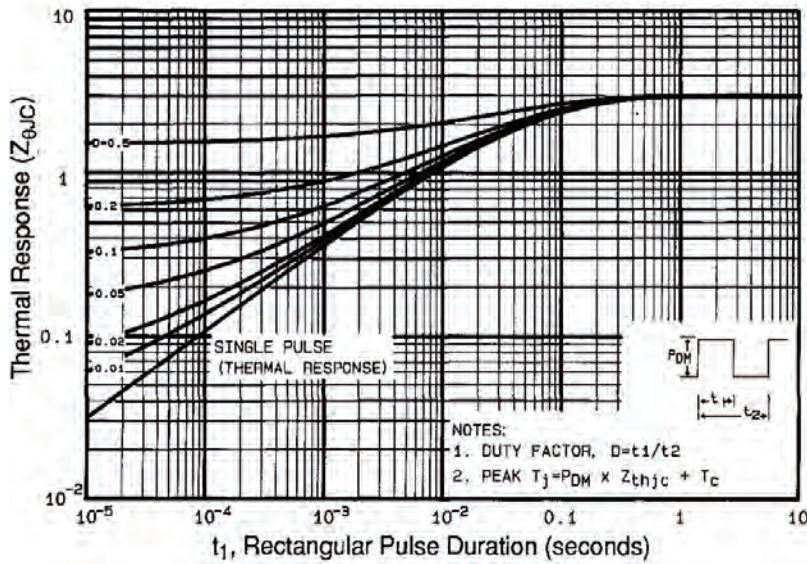


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

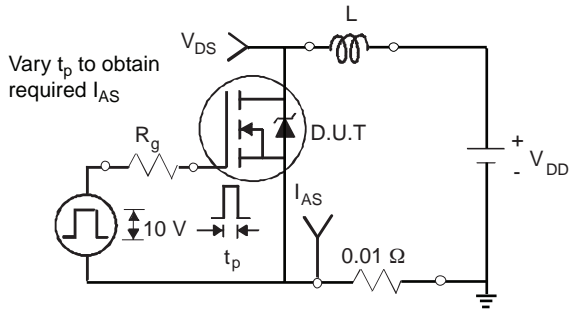


Fig. 12a - Unclamped Inductive Test Circuit

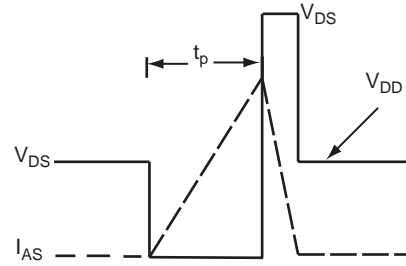


Fig. 12b - Unclamped Inductive Waveforms

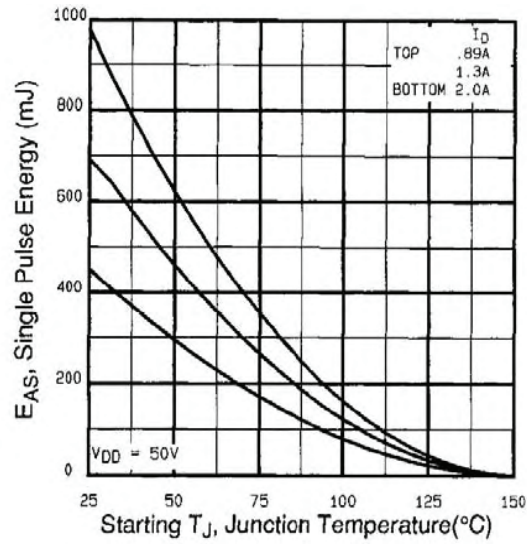


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

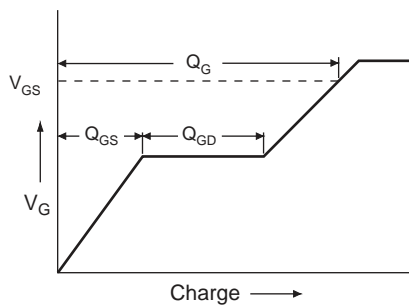


Fig. 13a - Basic Gate Charge Waveform

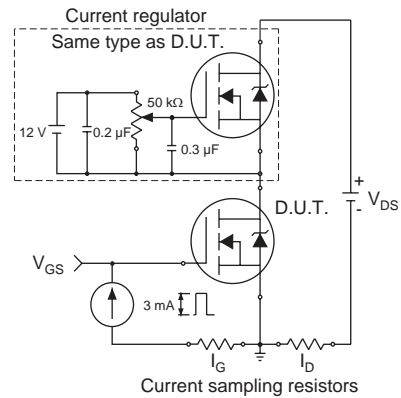
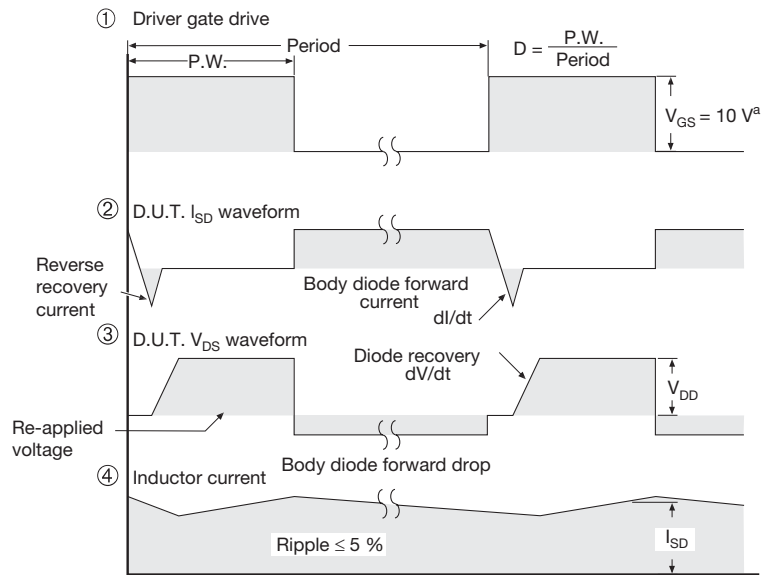
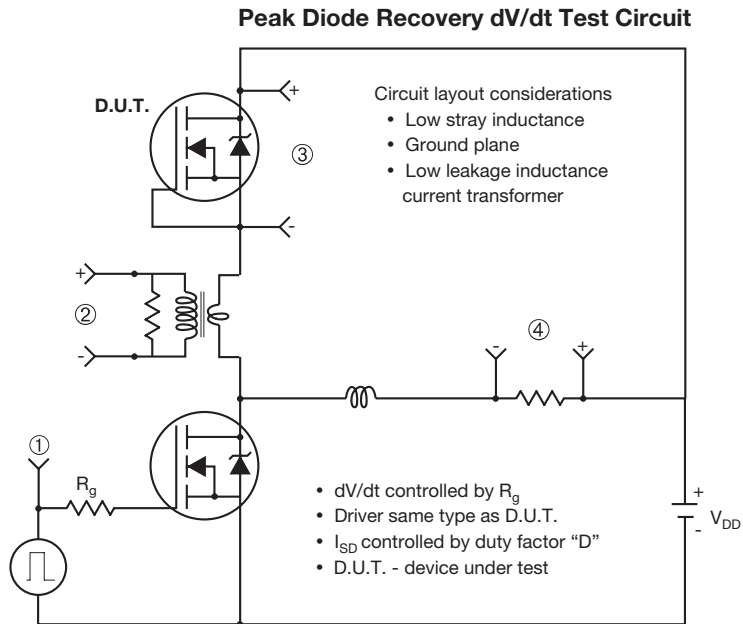


Fig. 13b - Gate Charge Test Circuit

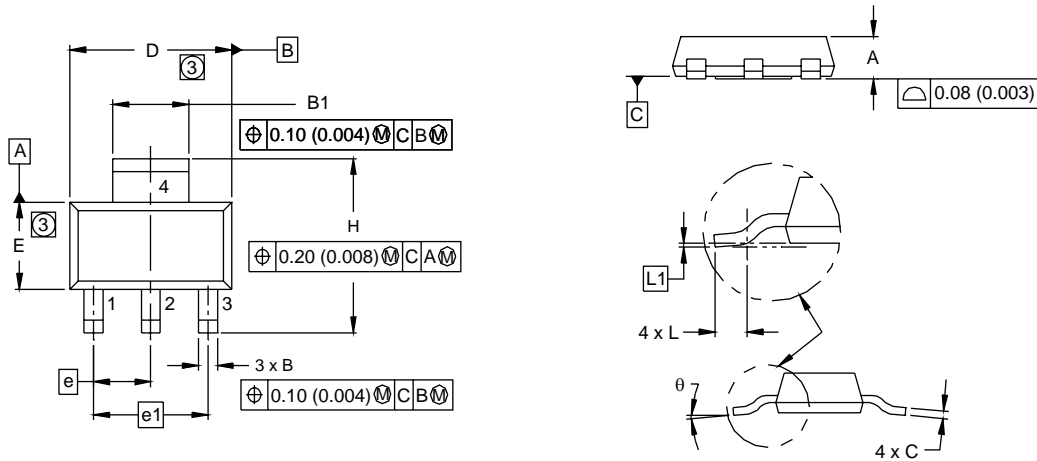


**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

**SOT-223 (HIGH VOLTAGE)**



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.55	1.80	0.061	0.071
B	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
C	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
E	3.30	3.70	0.130	0.146
e	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181 BSC	
H	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024 BSC	
$\theta$	-	10'	-	10'

ECN: S-82109-Rev. A, 15-Sep-08  
DWG: 5969

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension do not include mold flash.
4. Outline conforms to JEDEC outline TO-261AA.



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