

# Product Specification

## XBLW SN74LS161

Presettable Synchronous 4-bit  
Binary Counter; Asynchronous Reset

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## Description

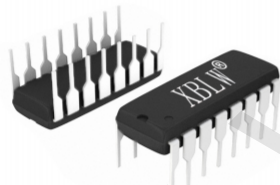
The SN74LS161 is a synchronous presettable binary counter with an internal look-ahead carry. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q0 to Q3) of the counters may be preset HIGH or LOW. A LOW at the parallel enable input ( $\overline{PE}$ ) disables the counting action and causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock. Preset takes place regardless of the levels at count enable inputs (CEP and CET). A LOW at the master reset input ( $\overline{MR}$ ) sets Q0 to Q3 LOW regardless of the levels at input pins CP,  $\overline{PE}$ , CET and CEP (thus providing an asynchronous clear function). The look-ahead carry simplifies serial cascading of the counters. Both CEP and CET must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH output of Q0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = 1 / (t_{P(max)}(CP \text{ to } TC) + t_{su}(CEP \text{ to } CP))$$

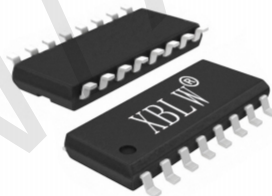
Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## Features

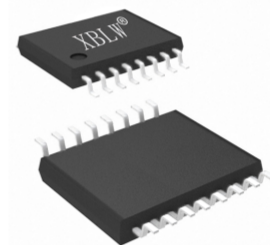
- Synchronous counting and loading
- 2 count enable inputs for n-bit cascading
- Asynchronous reset
- Positive-edge triggered clock
- Specified from -20°C to +85°C
- Packaging information: DIP-16/SOP-16/TSSOP-16



DIP-16



SOP-16



TSSOP-16

## Order Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74LS161N	DIP-16	74LS161N	Tube	1000Pcs/Box
XBLW SN74LS161DTR	SOP-16	74LS161	Tape	2500Pcs/Reel
XBLW SN74LS161DTR	TSSOP-16	74LS161	Tape	3000Pcs/Reel

### Block Diagram

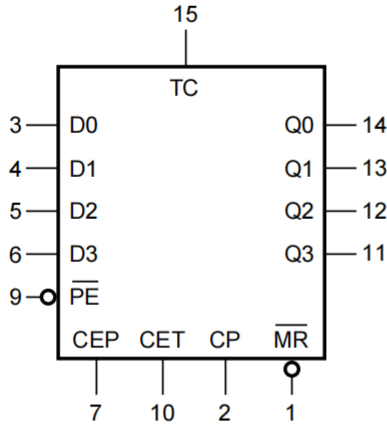


Figure 1. Logic symbol

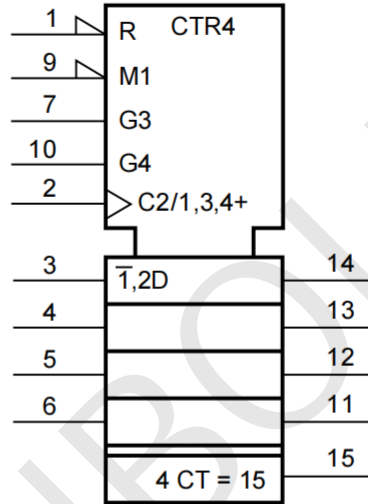


Figure 2. IEC Logic symbol

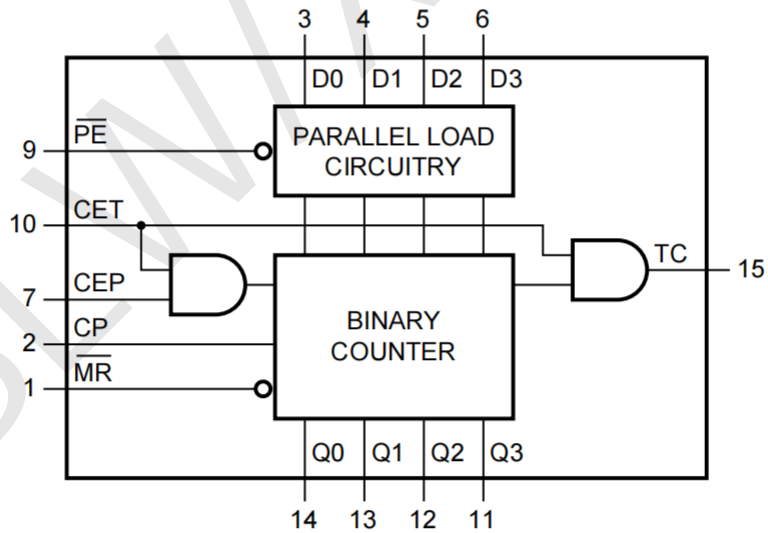


Figure 3. Functional diagram

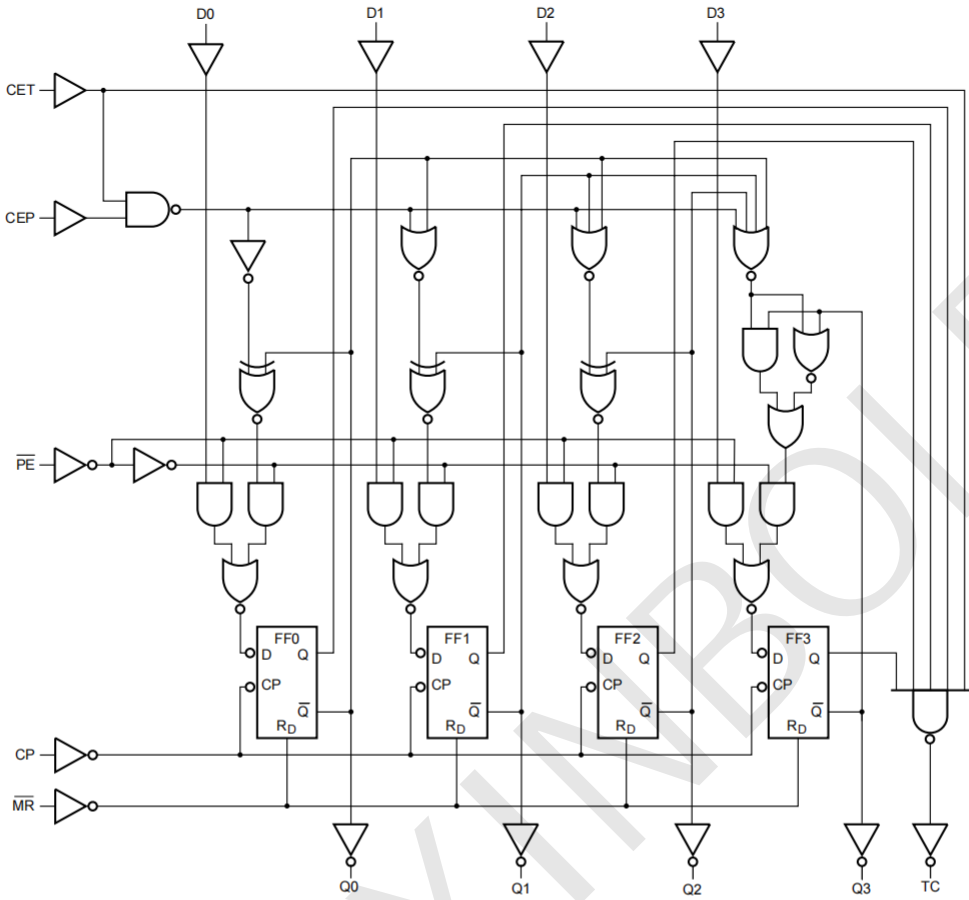


Figure 4. Logic diagram

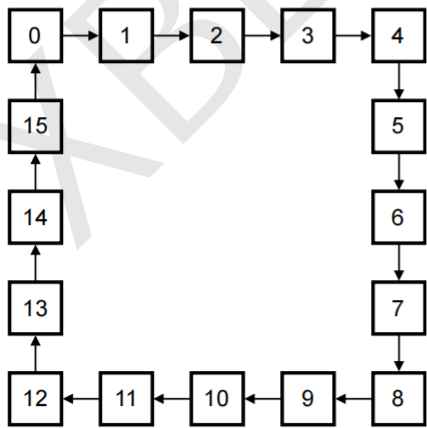


Figure 5. State diagram

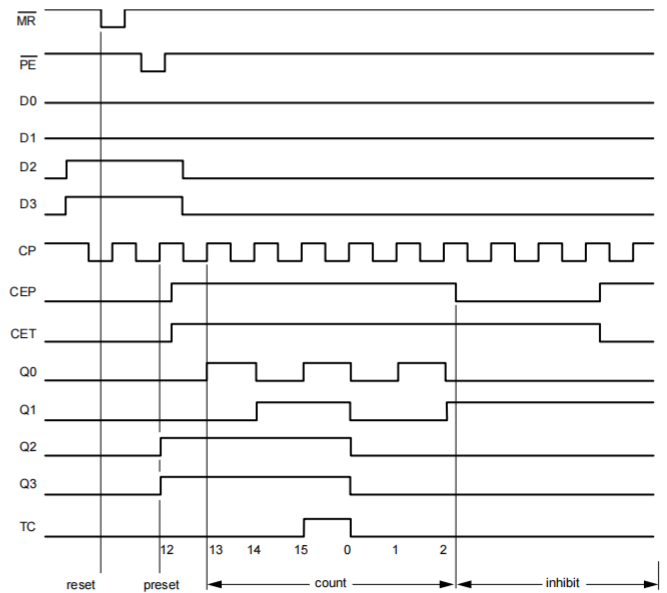
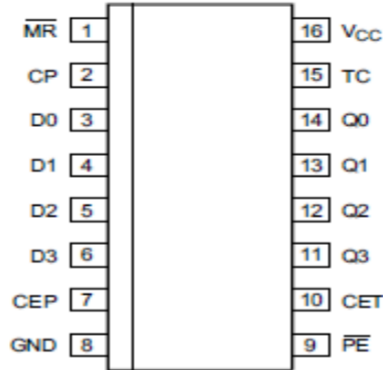


Figure 6. Typical timing sequence

## Pin Configurations



## Pin Description

Pin No.	Pin Name	Description
1	$\bar{M}R$	asynchronous master reset(active LOW)
2	CP	clock input(LOW-to-HIGH,edge triggered)
3	D0	data input
4	D1	data input
5	D2	data input
6	D3	data input
7	CEP	count enable input
8	GND	ground(0V)
9	$\bar{P}E$	parallel enable input(active LOW)
10	CET	count enable carry input
11	Q3	flip-flop output
12	Q2	flip-flop output
13	Q1	flip-flop output
14	Q0	flip-flop output
15	TC	terminal count output
16	V <sub>CC</sub>	supply voltage

## Function Table

Operating mode	Input						Output	
	$\bar{M}R$	CP	CEP	CET	$\bar{P}E$	Dn	Qn	TC
reset(clear)	L	X	X	X	X	X	L	L
parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	[2]
count	H	↑	h	h	h	X	count	[2]
hold(do nothing)	H	X	l	X	h	X	q <sub>n</sub>	[2]
	H	X	X	l	h	X	q <sub>n</sub>	L

Note:

[ 1 ] H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH clock transition;

l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

h=HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;

q=lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition.

[2] The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).

## Electrical Parameter

### Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V <sub>CC</sub>	-	-0.5	+7.0	V
input clamping current	I <sub>IK</sub>	V <sub>I</sub> < -0.5V or V <sub>I</sub> > V <sub>CC</sub> +0.5V	-	±20	mA
output clamping current	I <sub>OK</sub>	V <sub>O</sub> < -0.5V or V <sub>O</sub> > V <sub>CC</sub> +0.5V	-	±20	mA
output current	I <sub>O</sub>	-0.5V < V <sub>O</sub> < V <sub>CC</sub> +0.5V	-	±25	mA
supply current	I <sub>CC</sub>	-	-	+50	mA
ground current	I <sub>GND</sub>	-	-50	-	mA
storage temperature	T <sub>stg</sub>	-	-65	+150	°C
total power dissipation	P <sub>tot</sub>	-	-	500	mW
soldering temperature	T <sub>L</sub>	10s	DIP	245	°C
			SOP	250	

Note:

[ 1 ] For DIP16 packages: above 70°C the value of P<sub>tot</sub> derates linearly with 12mW/K.

[2] For SOP16 packages: above 70°C the value of P<sub>tot</sub> derates linearly with 8mW/K.

[3] For (T)SSOP16 packages: above 60°C the value of P<sub>tot</sub> derates linearly with 5.5mW/K.



## Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>SN74LS161</b>						
supply voltage	$V_{CC}$	-	2.0	5.0	6.0	V
input voltage	$V_I$	-	0	-	$V_{CC}$	V
output voltage	$V_O$	-	0	-	$V_{CC}$	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0V$	-	-	625	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	83	ns/V
ambient temperature	$T_{amb}$	-	-20	-	+85	°C

## Electrical Characteristics

### DC Characteristics 1

( $T_{amb}=25^{\circ}C$ , voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
HIGH-level input voltage	$V_{IH}$	$V_{CC}=2.0V$	1.5	1.2	-	V	
		$V_{CC}=4.5V$	3.15	2.4	-	V	
		$V_{CC}=6.0V$	4.2	3.2	-	V	
LOW-level input voltage	$V_{IL}$	$V_{CC}=2.0V$	-	0.8	0.5	V	
		$V_{CC}=4.5V$	-	2.1	1.35	V	
		$V_{CC}=6.0V$	-	2.8	1.8	V	
HIGH-level output voltage	$V_{OH}$	$V_I=V_{IH}$ or $V_{IL}$	$I_O=-20\mu A; V_{CC}=2.0V$	1.9	2.0	-	V
			$I_O=-20\mu A; V_{CC}=4.5V$	4.4	4.5	-	V
			$I_O=-20\mu A; V_{CC}=6.0V$	5.9	6.0	-	V
			$I_O=-4.0mA; V_{CC}=4.5V$	3.98	4.32	-	V
			$I_O=-5.2mA; V_{CC}=6.0V$	5.48	5.81	-	V
LOW-level output voltage	$V_{OL}$	$V_I=V_{IH}$ or $V_{IL}$	$I_O=20\mu A; V_{CC}=2.0V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=4.5V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=6.0V$	-	0	0.1	V
			$I_O=4.0mA; V_{CC}=4.5V$	-	0.15	0.26	V
			$I_O=5.2mA; V_{CC}=6.0V$	-	0.16	0.26	V
input leakage current	$I_I$	$V_I=V_{CC}$ or GND; $V_{CC}=6.0V$	-	-	$\pm 1$	$\mu A$	
supply current	$I_{CC}$	$V_I=V_{CC}$ or GND; $I_O=0A; V_{CC}=6.0V$	-	-	8.0	$\mu A$	
input apacitance	$C_I$	-	-	3.5	-	pF	

**DC Characteristics 2**

 ( $T_{amb} = -20^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
HIGH-level input voltage	$V_{IH}$	$V_{CC}=2.0\text{V}$	1.5	-	-	V	
		$V_{CC}=4.5\text{V}$	3.15	-	-	V	
		$V_{CC}=6.0\text{V}$	4.2	-	-	V	
LOW-level input voltage	$V_{IL}$	$V_{CC}=2.0\text{V}$	-	-	0.5	V	
		$V_{CC}=4.5\text{V}$	-	-	1.35	V	
		$V_{CC}=6.0\text{V}$	-	-	1.8	V	
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	$I_O = -20\mu\text{A}; V_{CC} = 2.0\text{V}$	1.9	-	-	V
			$I_O = -20\mu\text{A}; V_{CC} = 4.5\text{V}$	4.4	-	-	V
			$I_O = -20\mu\text{A}; V_{CC} = 6.0\text{V}$	5.9	-	-	V
			$I_O = -4.0\text{mA}; V_{CC} = 4.5\text{V}$	3.84	-	-	V
			$I_O = -5.2\text{mA}; V_{CC} = 6.0\text{V}$	5.34	-	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_O = 20\mu\text{A}; V_{CC} = 2.0\text{V}$	-	-	0.1	V
			$I_O = 20\mu\text{A}; V_{CC} = 4.5\text{V}$	-	-	0.1	V
			$I_O = 20\mu\text{A}; V_{CC} = 6.0\text{V}$	-	-	0.1	V
			$I_O = 4.0\text{mA}; V_{CC} = 4.5\text{V}$	-	-	0.33	V
			$I_O = 5.2\text{mA}; V_{CC} = 6.0\text{V}$	-	-	0.33	V
input leakage current	$I_I$	$V_i = V_{CC}$ or $\text{GND}; V_{CC} = 6.0\text{V}$	-	-	$\pm 1.0$	$\mu\text{A}$	
supply current	$I_{CC}$	$V_i = V_{CC}$ or $\text{GND}; I_O = 0\text{A}; V_{CC} = 6.0\text{V}$	-	-	80	$\mu\text{A}$	



### AC Characteristics 1

( $T_{amb}=25^{\circ}C$ ,  $GND = 0V$ ;  $t_r=t_f = 6ns$ ;  $C_L=50pF$ , unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit			
Propagation delay	$t_{pd}$	CP to Qn; see Figure8	$V_{CC}=2.0V$	-	61	190	ns		
			$V_{CC}=4.5V$	-	22	38	ns		
			$V_{CC}=5.0V; C_L= 15pF$	-	19	-	ns		
			$V_{CC}=6.0V$	-	18	32	ns		
		CP to TC; see Figure8	$V_{CC}=2.0V$	-	69	215	ns		
			$V_{CC}=4.5V$	-	25	43	ns		
			$V_{CC}=5.0V; C_L= 15pF$	-	21	-	ns		
			$V_{CC}=6.0V$	-	20	37	ns		
		CET to TC; see Figure9	$V_{CC}=2.0V$	-	33	150	ns		
			$V_{CC}=4.5V$	-	12	30	ns		
			$V_{CC}=5.0V; C_L= 15pF$	-	10	-	ns		
			$V_{CC}=6.0V$	-	10	26	ns		
High to LOW Propagation delay	$t_{PHL}$	$\overline{MR}$ to Qn; see Figure10	$V_{CC}=2.0V$	-	63	210	ns		
			$V_{CC}=4.5V$	-	23	42	ns		
			$V_{CC}=5.0V; C_L= 15pF$	-	20	-	ns		
			$V_{CC}=6.0V$	-	18	36	ns		
		$\overline{MR}$ to TC; see Figure10	$V_{CC}=2.0V$	-	63	220	ns		
			$V_{CC}=4.5V$	-	23	44	ns		
			$V_{CC}=5.0V; C_L= 15pF$	-	20	-	ns		
			$V_{CC}=6.0V$	-	18	37	ns		
		transition time	$t_t$	see Figure8 and see Figure9	$V_{CC}=2.0V$	-	19	75	ns
					$V_{CC}=4.5V$	-	7	15	ns
					$V_{CC}=6.0V$	-	6	13	ns
		pulse width	$t_w$	CP HIGH or LOW; see Figure8	$V_{CC}=2.0V$	80	22	-	ns
$V_{CC}=4.5V$	16				8	-	ns		
$V_{CC}=6.0V$	14				6	-	ns		
$\overline{MR}$ LOW; see Figure10	$V_{CC}=2.0V$			80	19	-	ns		
	$V_{CC}=4.5V$			16	7	-	ns		
	$V_{CC}=6.0V$			14	6	-	ns		
Recovery time	$t_{rec}$	$\overline{MR}$ to CP; see Figure10	$V_{CC}=2.0V$	100	19	-	ns		
			$V_{CC}=4.5V$	20	7	-	ns		
			$V_{CC}=6.0V$	17	6	-	ns		
Set-up time	$t_{su}$	Dn to CP; see Figure11	$V_{CC}=2.0V$	80	25	-	ns		
			$V_{CC}=4.5V$	16	9	-	ns		
			$V_{CC}=6.0V$	14	7	-	ns		
		$\overline{PE}$ to CP; see Figure11	$V_{CC}=2.0V$	100	30	-	ns		
			$V_{CC}=4.5V$	20	11	-	ns		
			$V_{CC}=6.0V$	17	9	-	ns		
		CEP,CET to CP; see Figure12	$V_{CC}=2.0V$	170	47	-	ns		
			$V_{CC}=4.5V$	34	17	-	ns		
			$V_{CC}=6.0V$	29	14	-	ns		
Hold time	$t_h$	$\overline{Dn}, \overline{PE}$ , CEP, CET to CP; see Figure11, 12	$V_{CC}=2.0V$	0	-14	-	ns		
			$V_{CC}=4.5V$	0	-5	-	ns		
			$V_{CC}=6.0V$	0	-4	-	ns		

Maximum frequency	$f_{MAX}$	CP; see Figure 8	$V_{CC}=2.0V$	4.6	13	-	MHz
			$V_{CC}=4.5V$	23	40	-	MHz
			$V_{CC}=5.0V; C_L=15pF$	-	44	-	MHz
			$V_{CC}=6.0V$	27	48	-	MHz
power dissipation capacitance	$C_{PD}$	$f_i=1MHz; V_i=GND \text{ to } V_{CC}$	-	33	-	pF	

Note:

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in uW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;  $V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;  $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

**AC Characteristics 2**

( $T_{amb} = -20^{\circ}C$  to  $+85^{\circ}C$ ,  $GND = 0V$ ;  $t_r = t_f = 6ns$ ;  $C_L = 50pF$ , unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Propagation delay	$t_{pd}$	CP to Qn; see Figure8	$V_{CC} = 2.0V$	-	-	240	ns
			$V_{CC} = 4.5V$	-	-	48	ns
			$V_{CC} = 6.0V$	-	-	41	ns
		CP to TC; see Figure8	$V_{CC} = 2.0V$	-	-	270	ns
			$V_{CC} = 4.5V$	-	-	54	ns
			$V_{CC} = 6.0V$	-	-	46	ns
		CET to TC; see Figure9	$V_{CC} = 2.0V$	-	-	190	ns
			$V_{CC} = 4.5V$	-	-	38	ns
			$V_{CC} = 6.0V$	-	-	33	ns
High to LOW Propagation delay	$t_{PHL}$	$\bar{MR}$ to Qn; see Figure10	$V_{CC} = 2.0V$	-	-	265	ns
			$V_{CC} = 4.5V$	-	-	53	ns
			$V_{CC} = 6.0V$	-	-	45	ns
		$\bar{MR}$ to TC; see Figure10	$V_{CC} = 2.0V$	-	-	275	ns
			$V_{CC} = 4.5V$	-	-	55	ns
			$V_{CC} = 6.0V$	-	-	47	ns
transition time	$t_t$	see Figure8 and see Figure9	$V_{CC} = 2.0V$	-	-	95	ns
			$V_{CC} = 4.5V$	-	-	19	ns
			$V_{CC} = 6.0V$	-	-	16	ns
pulse width	$t_w$	CP HIGH or LOW; see Figure8	$V_{CC} = 2.0V$	100	-	-	ns
			$V_{CC} = 4.5V$	20	-	-	ns
			$V_{CC} = 6.0V$	17	-	-	ns
		$\bar{MR}$ LOW; see Figure10	$V_{CC} = 2.0V$	100	-	-	ns
			$V_{CC} = 4.5V$	20	-	-	ns
			$V_{CC} = 6.0V$	17	-	-	ns
Recovery time	$t_{rec}$	$\bar{MR}$ to CP; see Figure10	$V_{CC} = 2.0V$	125	-	-	ns
			$V_{CC} = 4.5V$	25	-	-	ns
			$V_{CC} = 6.0V$	21	-	-	ns
Set-up time	$t_{su}$	Dn to CP; see Figure11	$V_{CC} = 2.0V$	100	-	-	ns
			$V_{CC} = 4.5V$	20	-	-	ns
			$V_{CC} = 6.0V$	17	-	-	ns
		$\bar{PE}$ to CP; see Figure11	$V_{CC} = 2.0V$	125	-	-	ns
			$V_{CC} = 4.5V$	25	-	-	ns
			$V_{CC} = 6.0V$	21	-	-	ns

		CEP,CET to CP; see Figure12	V <sub>CC</sub> =2.0V	215	-	-	ns
			V <sub>CC</sub> =4.5V	43	-	-	ns
			V <sub>CC</sub> =6.0V	37	-	-	ns
Hold time	t <sub>h</sub>	Dn, PE CEP,CET, to CP; see Figure11, 12	V <sub>CC</sub> =2.0V	0	-	-	ns
			V <sub>CC</sub> =4.5V	0	-	-	ns
			V <sub>CC</sub> =6.0V	0	-	-	ns
Maximum frequency	f <sub>MAX</sub>	CP;see Figure8	V <sub>CC</sub> =2.0V	3.6	-	-	MHz
			V <sub>CC</sub> =4.5V	18	-	-	MHz
			V <sub>CC</sub> =6.0V	21	-	-	MHz

Note:

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[2] t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.

## Testing Circuit

### AC Testing Circuit

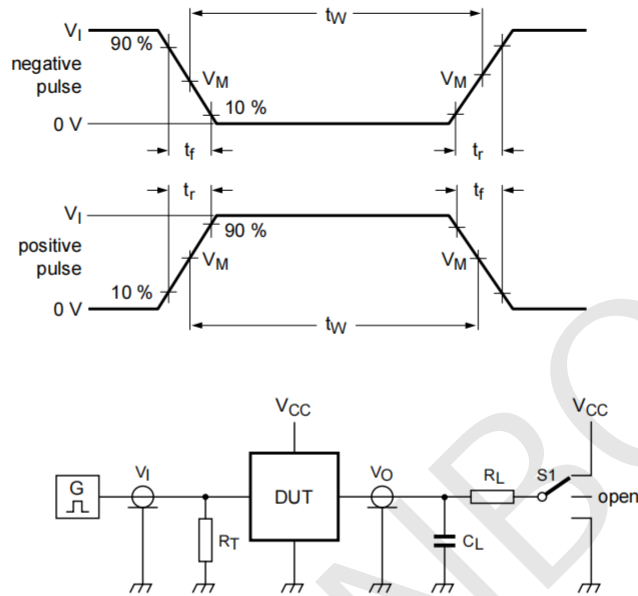


Figure 7. Test circuit for measuring switching times

Definitions for test circuit:

$C_L$ =Load capacitance including jig and probe capacitance.

$R_T$ =Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

$R_L$ =Load resistance

S1=Test selection switch

### AC Testing Waveforms

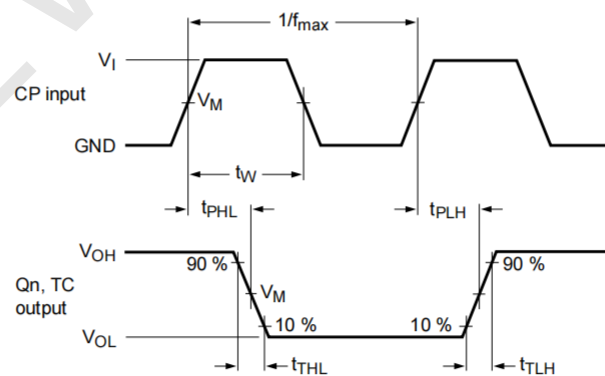


Figure 8. The clock (CP) to outputs (Qn, TC) propagation delays, pulse width, output transition times and maximum frequency

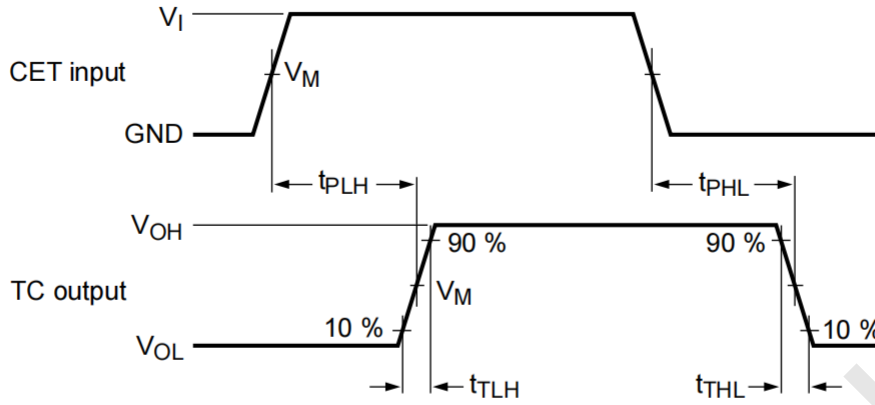


Figure 9. The count enable carry input (CET) to terminal count output (TC) propagation delays and output transition times

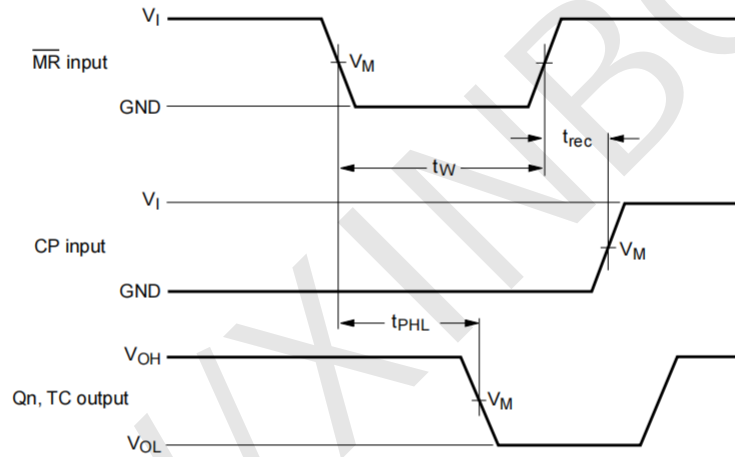


Figure 10. The master reset (MR) pulse width, master reset to output (Qn, TC) propagation delays, and the master reset to clock (CP) recovery times

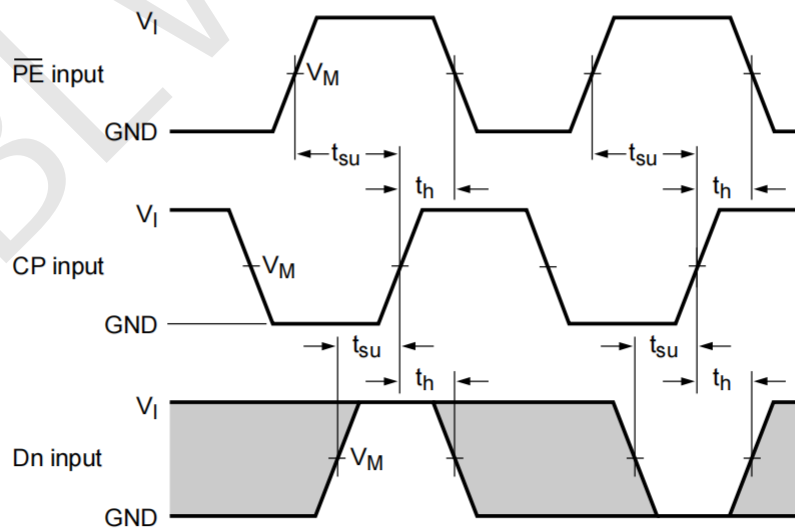


Figure 11. The data input (Dn) and parallel enable input (PE) set-up and hold times

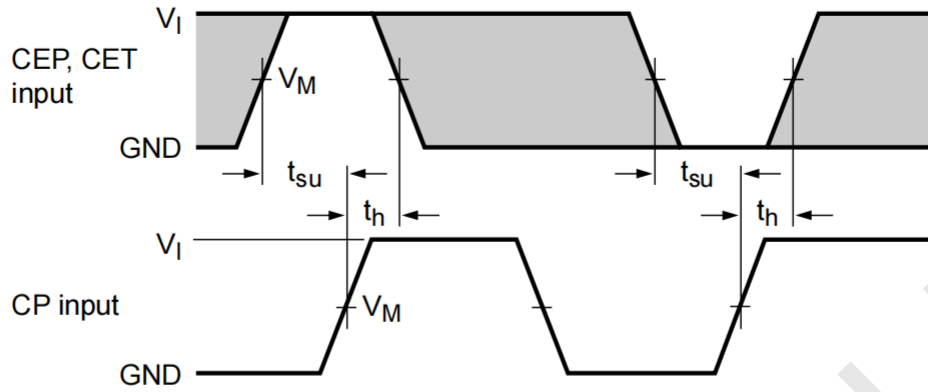


Figure 12. The count enable input (CEP) and count enable carry input (CET) set-up and hold times

### Measurement Points

Type	Input		Output
	$V_I$	$V_M$	$V_M$
SN74LS161	GND to $V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

### Test Data

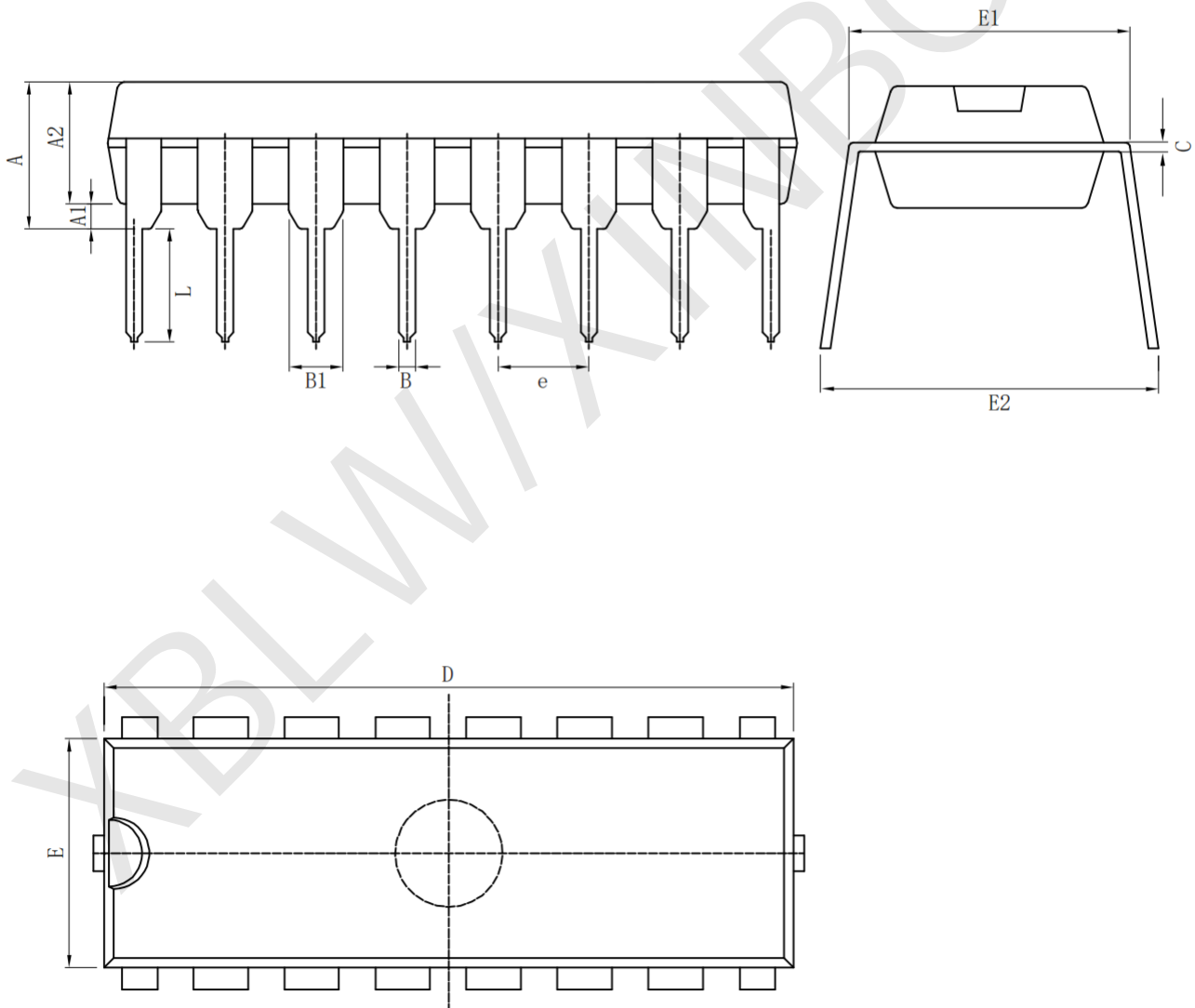
Type	Input		Load		S1 position
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$
SN74LS161	$V_{CC}$	6.0ns	15pF, 50pF	1K $\Omega$	open



## Package Information

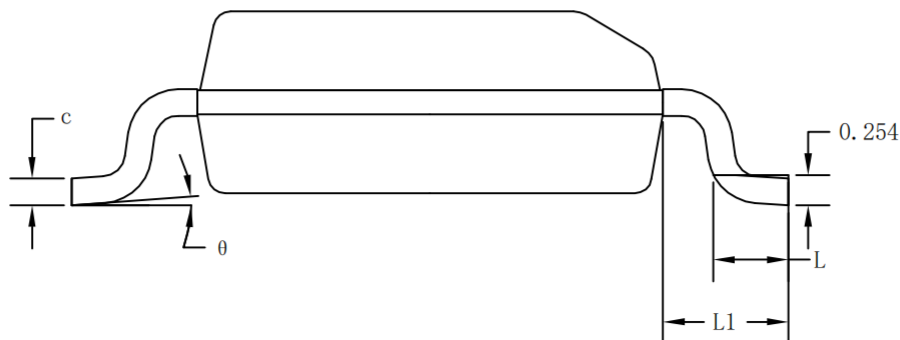
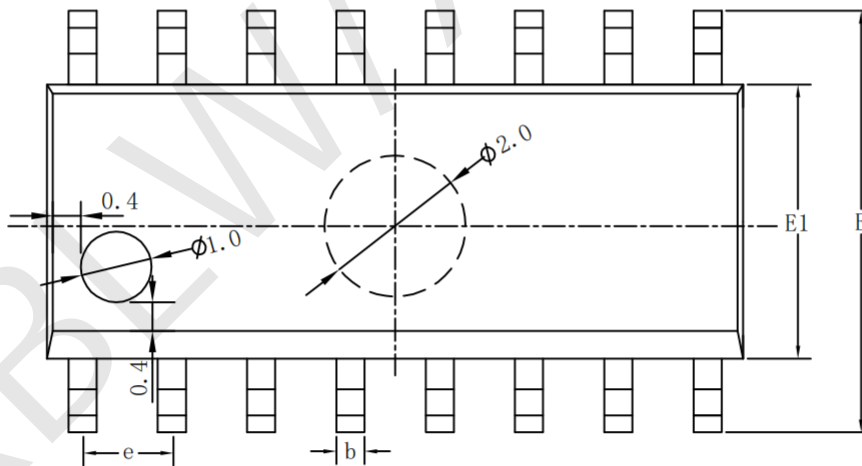
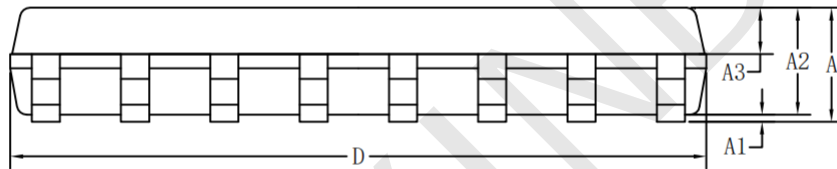
### · DIP-16

Symbol	Size	Dimensions In Millimeters		Symbol	Size	Dimensions In Inches	
		Min( mm)	Max( mm)			Min( in)	Max( in)
A		3.710	4.310	A		0.146	0.170
A1		0.510		A1		0.020	
A2		3.200	3.600	A2		0.126	0.142
B		0.380	0.570	B		0.015	0.022
B1		1.524 (BSC)		B1		0.060 (BSC)	
C		0.204	0.360	C		0.008	0.014
D		18.80	19.20	D		0.740	0.756
E		6.200	6.600	E		0.244	0.260
E1		7.320	7.920	E1		0.288	0.312
e		2.540 (BSC)		e		0.100 (BSC)	
L		3.000	3.600	L		0.118	0.142
E2		8.400	9.000	E2		0.331	0.354



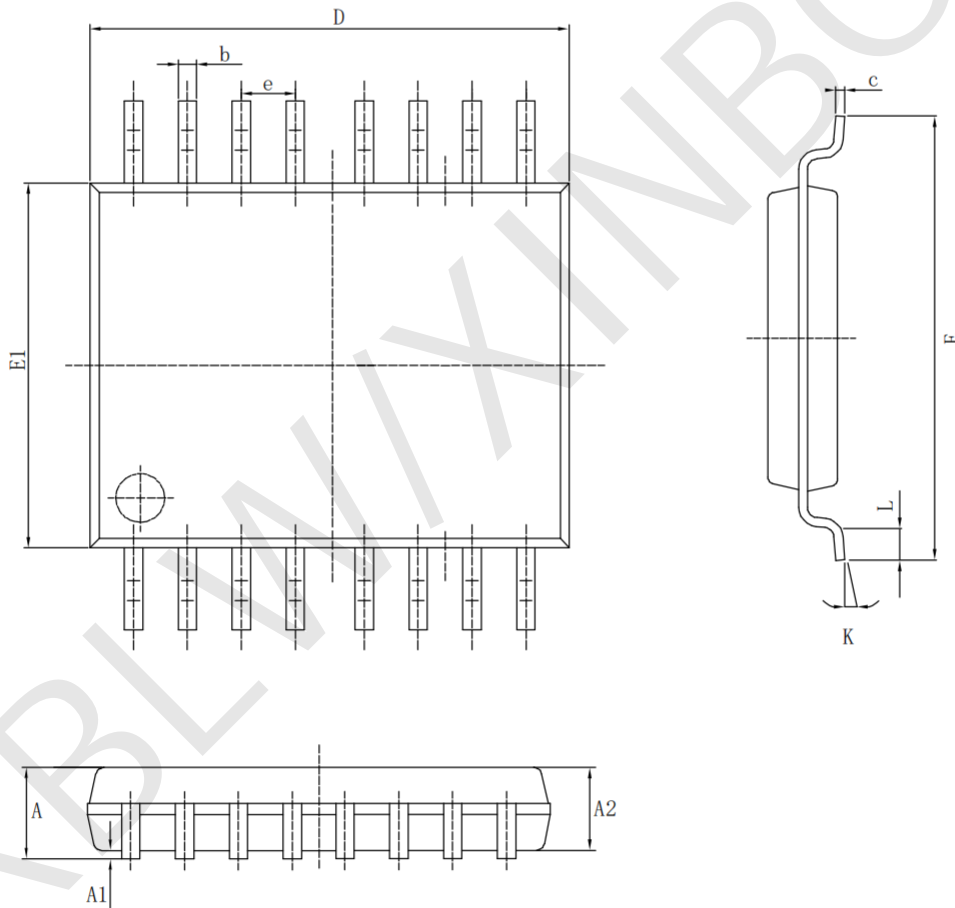
· SOP-16

Symbol	Dimensions In Millimeters			Symbol	Dimensions In Inches		
	Min (mm)	Nom (mm)	Max (mm)		Min (in)	Nom (in)	Max (in)
A	1.500	1.600	1.700	A	0.059	0.063	0.067
A1	0.100	0.150	0.250	A1	0.004	0.006	0.010
A2	1.400	1.450	1.500	A2	0.055	0.057	0.059
A3	0.600	0.650	0.700	A3	0.024	0.026	0.028
b	0.300	0.400	0.500	b	0.012	0.016	0.020
c	0.150	0.200	0.250	c	0.006	0.008	0.010
D	9.800	9.900	10.00	D	0.386	0.390	0.394
E	5.800	6.000	6.200	E	0.228	0.236	0.244
E1	3.850	3.900	3.950	E1	0.152	0.154	0.156
e	1.27 (BSC)			e	0.050 (BSC)		
L	0.500	0.600	0.700	L	0.020	0.024	0.028
L1	1.05 (BSC)			L1	0.041 (BSC)		
θ	0°	4°	8°	θ	0°	4°	8°



· TSSOP-16

Symbol	Dimensions In Millimeters		Symbol	Dimensions In Inches	
	Min (mm)	Max (mm)		Min (in)	Max (in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.480	E1	0.169	0.176
e	0.65 (BSC)		e	0.0256 (BSC)	
K	0°	8°	K	0°	8°
L	0.450	0.750	L	0.018	0.030



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