

General Description

The WST3401 is the highest performance trench P-Ch MOSFET with extreme high cell density , which provide excellent R_{DS(on)} and gate charge for most of the small power switching and load switch applications .

The WST3401 meet the RoHS and Green Product requirement , with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Green Device Available

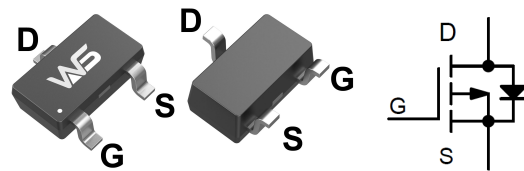
Product Summary

BVDSS	R _{DS(on)}	I _D
-30V	44mΩ	-5.5A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOT-23-3L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		10s	Steady State	
V _{DS}	Drain-Source Voltage	-30		V
V _{GS}	Gate-Source Voltage	± 12		V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ -10V ¹	-6.0	-5.5	A
I _D @T _C =70°C	Continuous Drain Current, V _{GS} @ -10V ¹	-4.9	-4.3	A
I _{DM}	Pulsed Drain Current ²	-17		A
P _D @T _A =25°C	Total Power Dissipation ³	1.32	1	W
P _D @T _A =70°C	Total Power Dissipation ³	0.84	0.64	W
T _{STG}	Storage Temperature Range	-55 to 150		°C
T _J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	125	°C/W
R _{θJA}	Thermal Resistance Junction-Ambient ¹ (t ≤ 10s)	---	95	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	80	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.023	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-3A	---	44	52	mΩ
		V _{GS} =-4.5V, I _D =-2A	---	50	58	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-0.6	---	-1.2	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	4	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-24V, V _{GS} =0V, T _J =25°C	---	---	-1	uA
		V _{DS} =-24V, V _{GS} =0V, T _J =55°C	---	---	-5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±12V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-3A	---	11	---	S
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-3A	---	6.4	9.0	nC
Q _{gs}	Gate-Source Charge		---	2.3	3.2	
Q _{gd}	Gate-Drain Charge		---	1.9	2.7	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, V _{GS} =-10V, R _G =3.3Ω, I _D =-3A	---	2.8	5.6	ns
T _r	Rise Time		---	8.4	15.1	
T _{d(off)}	Turn-Off Delay Time		---	39	78.0	
T _f	Fall Time		---	6	12.0	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	583	816	pF
C _{oss}	Output Capacitance		---	100	140	
C _{rss}	Reverse Transfer Capacitance		---	80	112	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	-4.3	A
I _{SM}	Pulsed Source Current ^{2,4}		---	---	-17	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1	V
t _{rr}	Reverse Recovery Time	I _F =-3A, dI/dt=100A/μs, T _J =25°C	---	7.8	---	nS
Q _{rr}	Reverse Recovery Charge		---	2.5	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper,t<10sec,t<10sec.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

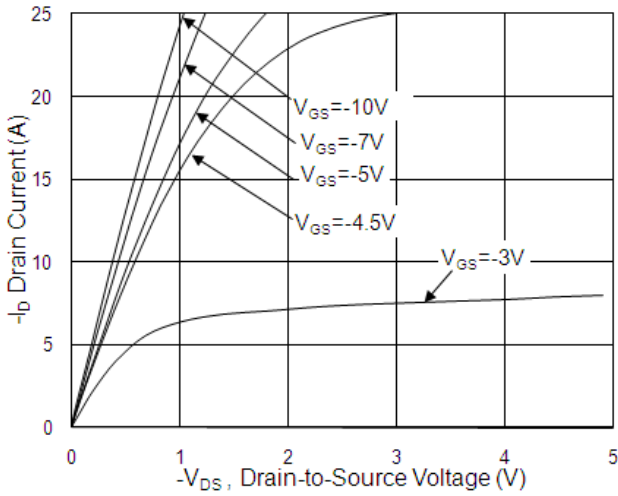


Fig.1 Typical Output Characteristics

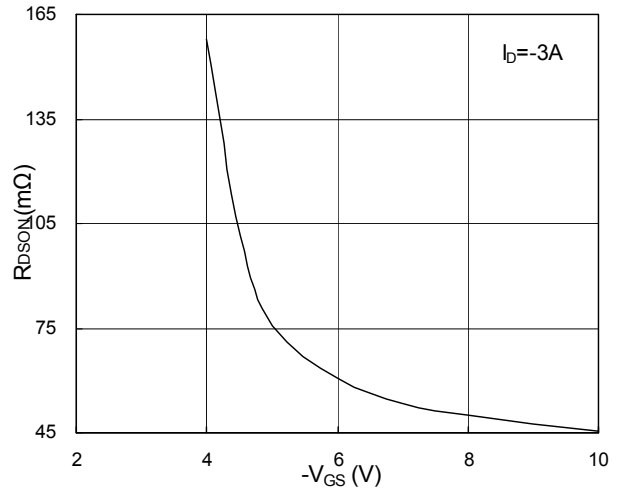


Fig.2 On-Resistance v.s Gate-Source

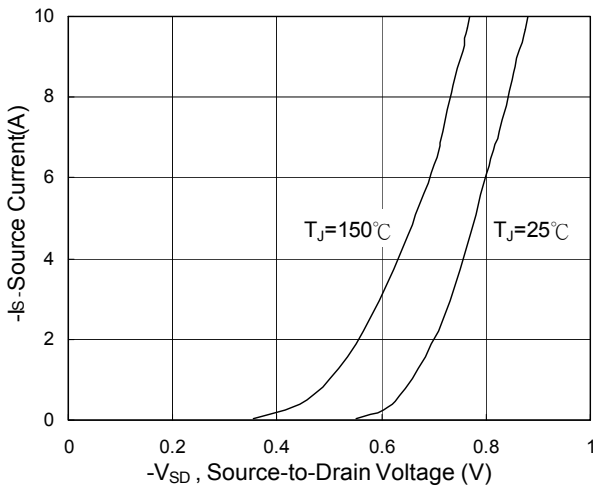


Fig.3 Forward Characteristics of Reverse

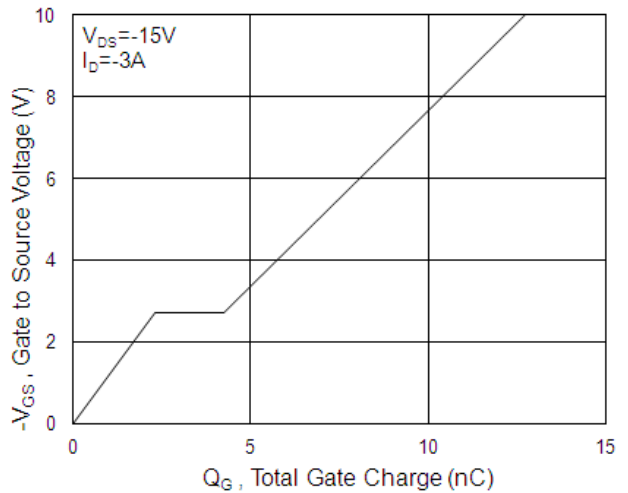


Fig.4 Gate-Charge Characteristics

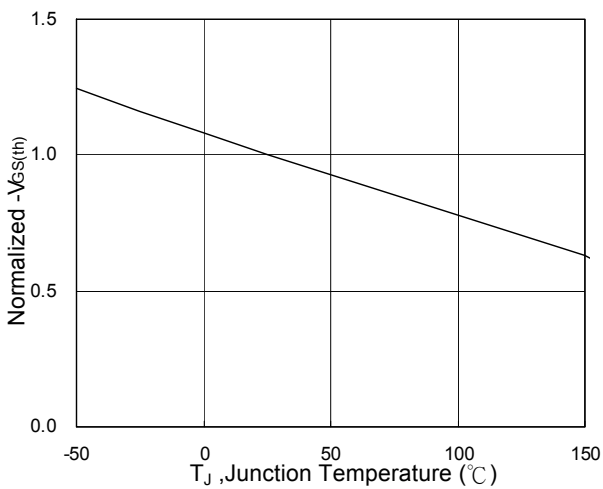


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

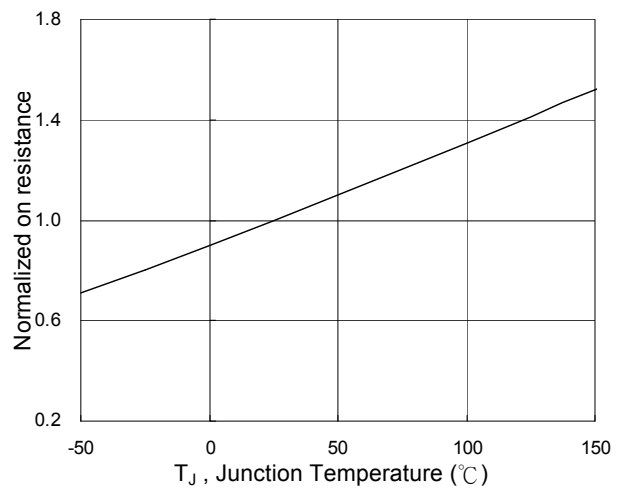


Fig.6 Normalized $R_{DS(on)}$ vs T_J

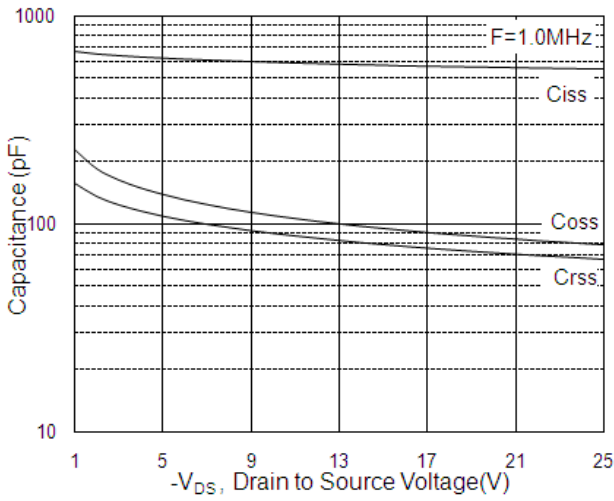


Fig.7 Capacitance

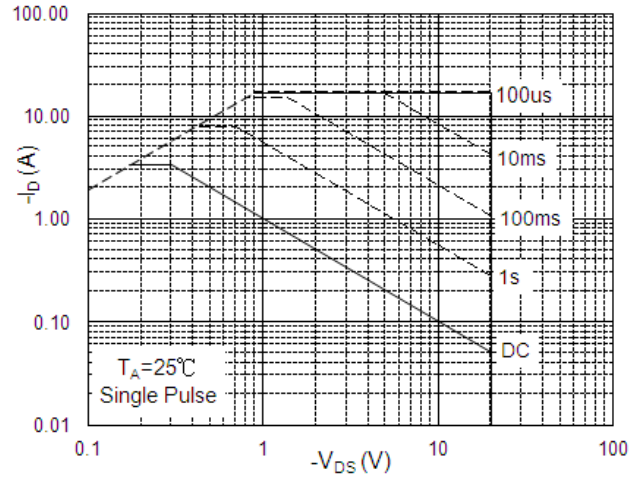


Fig.8 Safe Operating Area

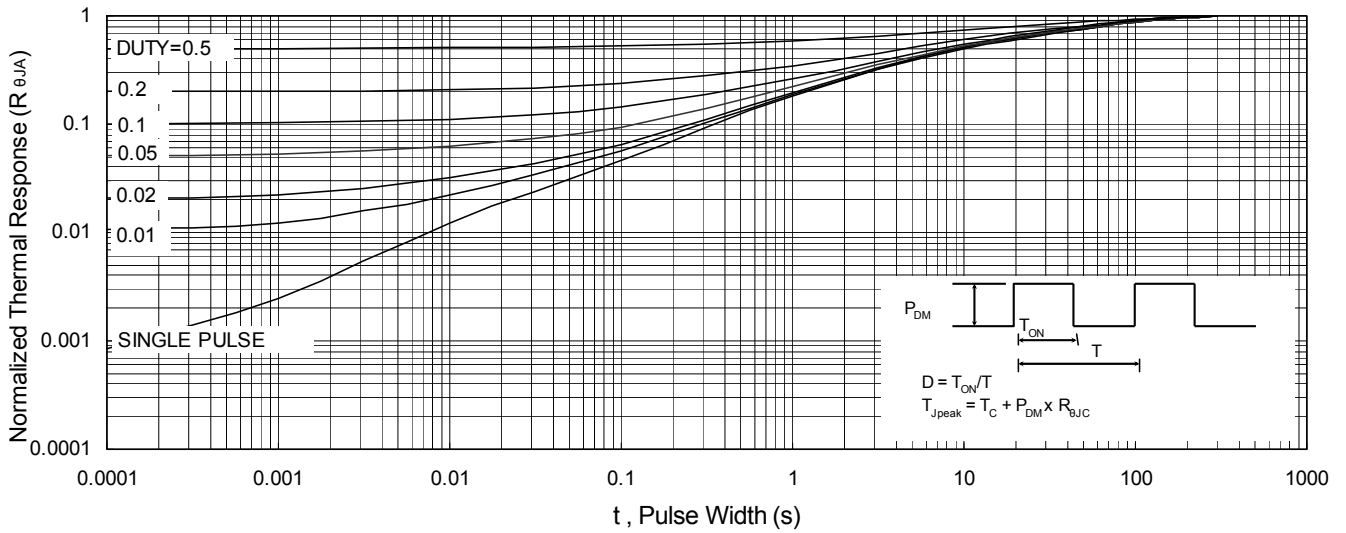


Fig.9 Normalized Maximum Transient Thermal Impedance

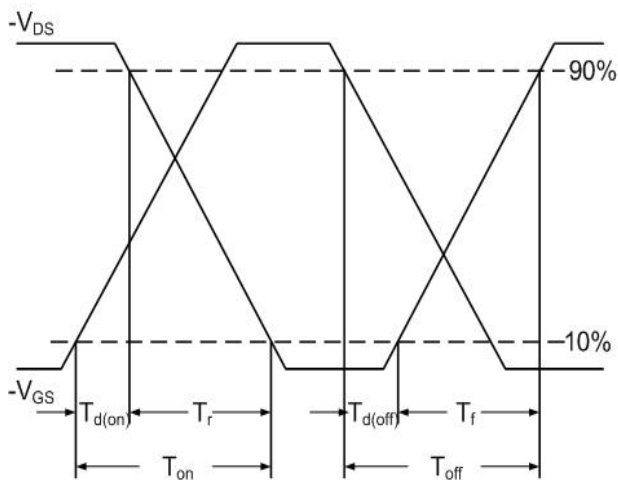


Fig.10 Switching Time Waveform

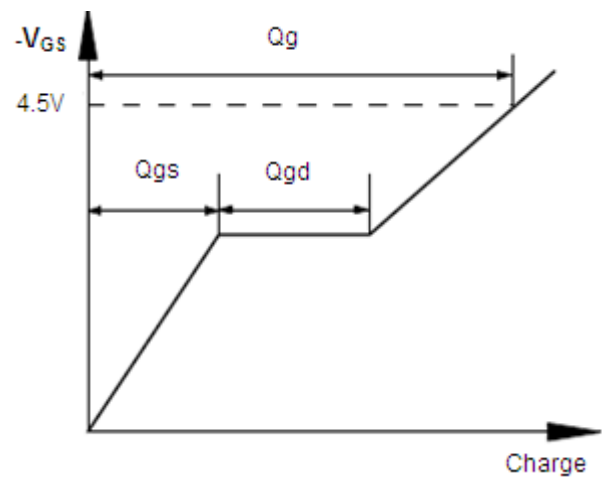


Fig.11 Gate Charge Waveform



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