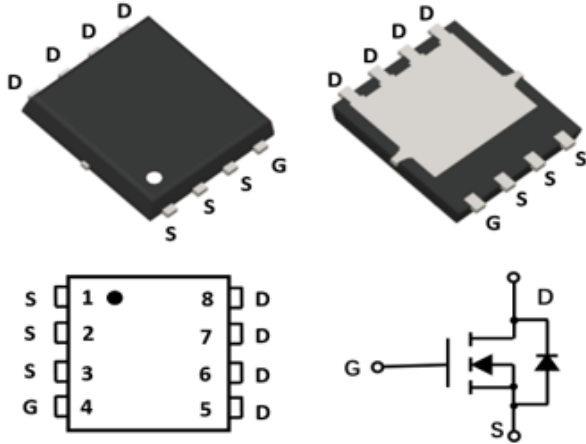


## N-Channel Enhancement Mode Field Effect Transistor

### PDFN5060



### Product Summary

- $V_{DS}$  100V
- $I_D$  60A
- $R_{DS(ON)}$ ( at  $V_{GS}=10V$ ) < 8.6 mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ ) < 13 mohm
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

- High Frequency Switching
- Synchronous Rectification

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	100	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_C=25^\circ\text{C}$	$I_D$	60	A
	$T_C=100^\circ\text{C}$		38	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	240	A
Avalanche energy <sup>B</sup>		EAS	200	mJ
Total Power Dissipation <sup>C</sup>	$T_C=25^\circ\text{C}$	$P_D$	88	W
	$T_C=100^\circ\text{C}$		35.2	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$t \leq 10S$	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.15	1.42	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG60G10B	F1	YJG60G10B	5000	10000	100000	13" reel



# YJG60G10B

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	100			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.3	1.8	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		7.5	8.6	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		9.5	13	mΩ
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V			1.3	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				60	A
Gate resistance	R <sub>G</sub>	f=1MHz, Open drain		0.68		Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, f=1MHZ		2270		pF
Output Capacitance	C <sub>oss</sub>			797		
Reverse Transfer Capacitance	C <sub>rss</sub>			36		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =25A		32		nC
Gate-Source Charge	Q <sub>gs</sub>			11.1		
Gate-Drain Charge	Q <sub>gd</sub>			4.78		
Reverse Recovery Chrage	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=100A/us		64		
Reverse Recovery Time	t <sub>rr</sub>			51.5		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =50V, I <sub>DS</sub> =25A R <sub>GEN</sub> =2.2Ω		9.3		ns
Turn-on Rise Time	t <sub>r</sub>			34.8		
Turn-off Delay Time	t <sub>D(off)</sub>			24.6		
Turn-off fall Time	t <sub>f</sub>			71		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V<sub>DD</sub>=50V, R<sub>G</sub>=25Ω, L=1mH, I<sub>AS</sub>=20A

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The Power dissipation PDSM is based on RθJA ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.



# YJG60G10B

## ■ Typical Performance Characteristics

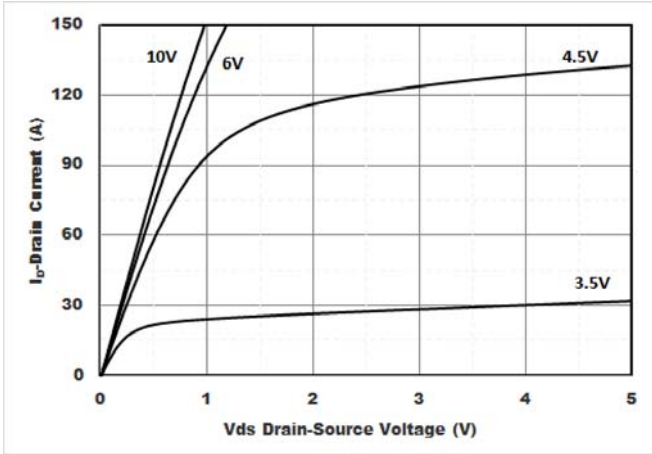


Figure1. Output Characteristics

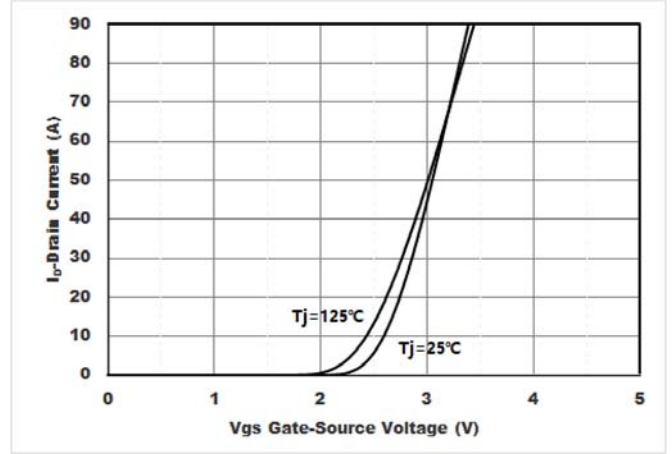


Figure2. Transfer Characteristics

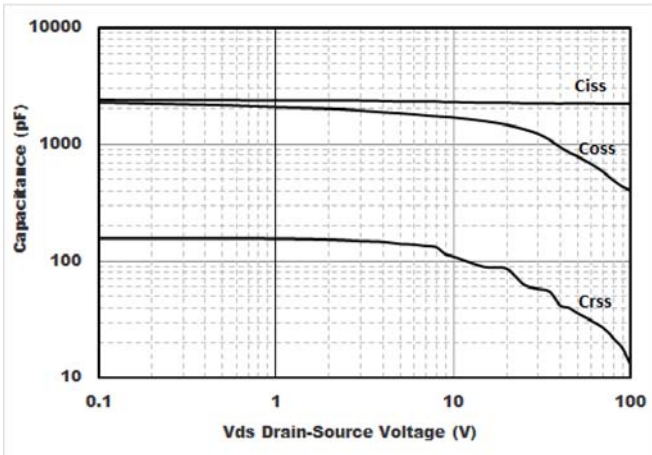


Figure3. Capacitance Characteristics

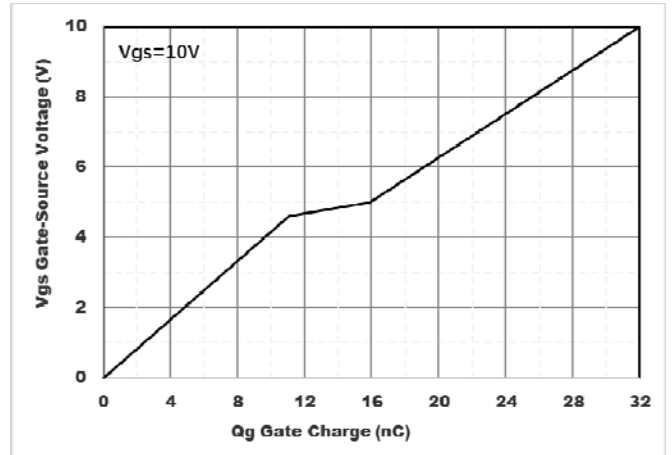


Figure4. Gate Charge

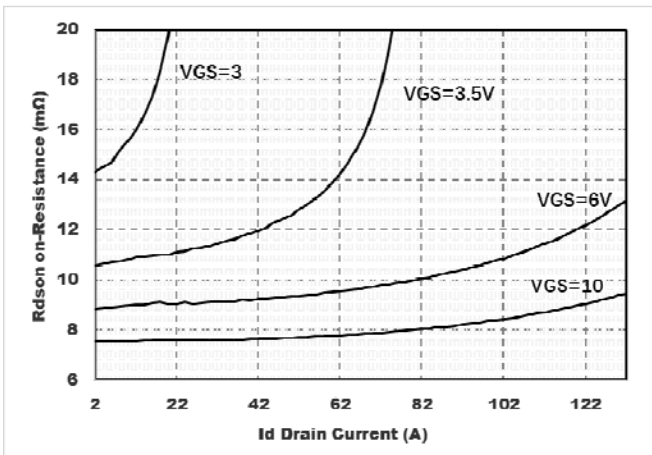


Figure5. : On-Resistance vs. Gate to Source Voltage

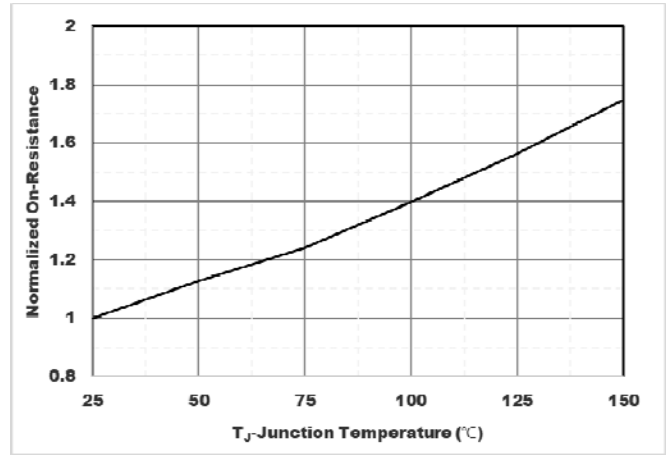


Figure6. Normalized On-Resistance



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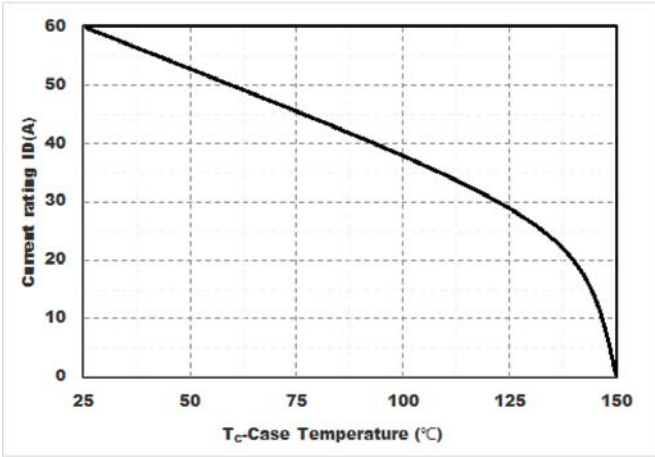


Figure7. Drain current

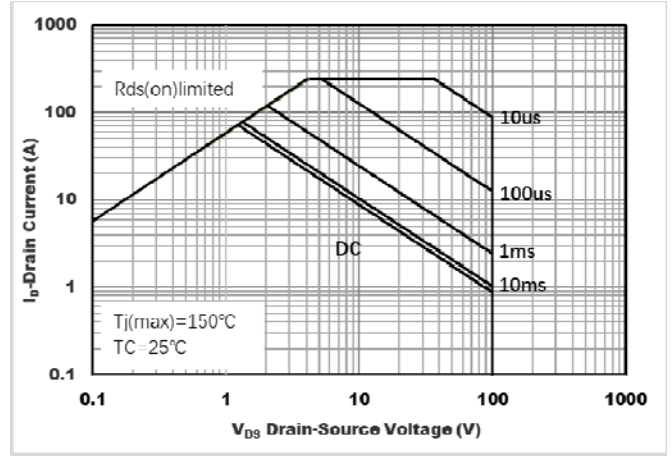


Figure8.Safe Operation Area

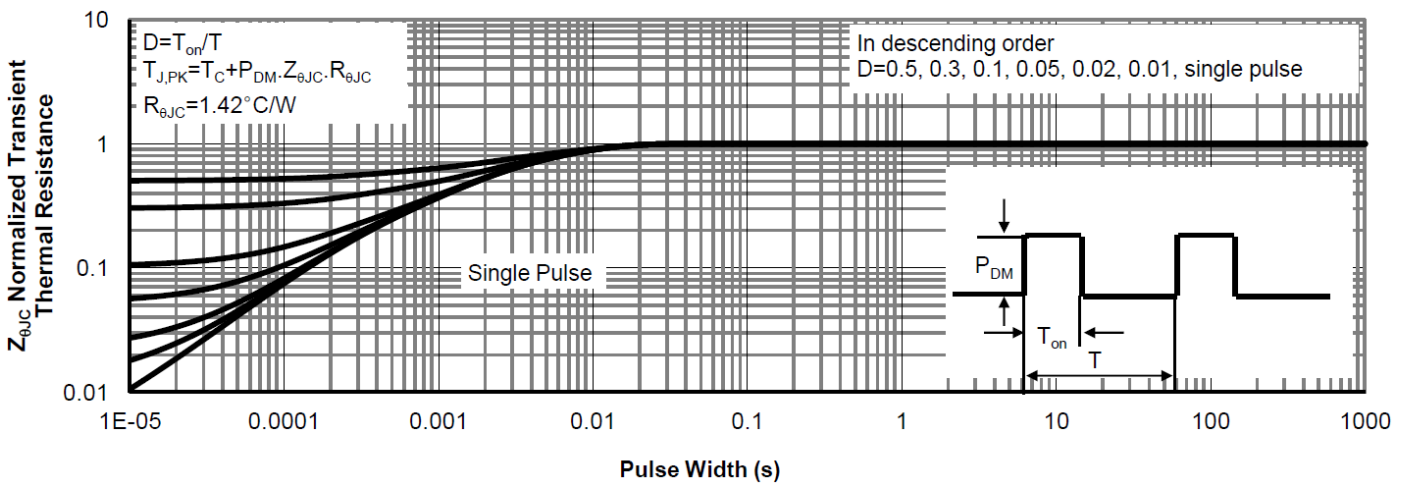
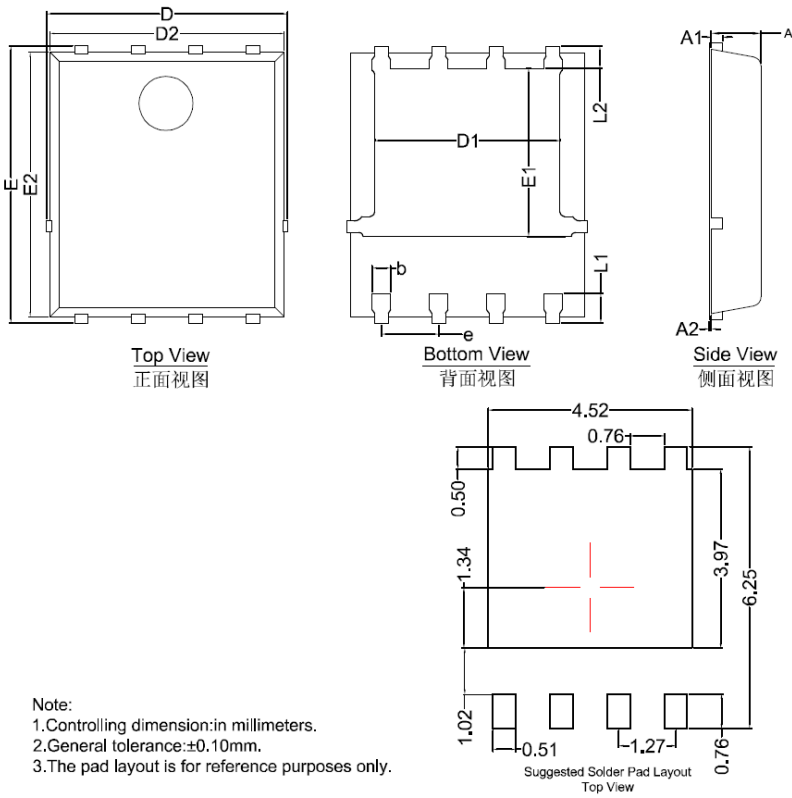


Figure9.Normalized Maximum Transient thermal impedance



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## ■ PDFN5060 Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.10$ mm.  
 3. The pad layout is for reference purposes only.



# YJG60G10B

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REV.	EFFECTIVE DATE	REVISION HISTORY	PREPARED
1.0	2021.4.21	New Release	Qun Zhao