SGM3804
Single Inductor, Positive/Negative Dual Output, Buck/Boost Converter

GENERAL DESCRIPTION

The SGM3804 generates both positive and negative precision regulated voltage power sources, with a patent pending control scheme for single inductor dual output converter. Outputs are programmable in 100mV steps in 2.4V to 6.4V range, which are commonly used in drivers for LCD displays and AMOLED displays, as well as in any other circuits requiring both rails, with different loading on each rail. The device is equipped with I^2C interface. With input in the range of 2.7V to 5.5V, the device is optimized for loading 100mA in boost-inverter mode and also works in buck-inverter mode.

The SGM3804 is available in a Green WLCSP-1.7×1.51-12B package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Single Inductor for Positive & Negative Outputs**
- **High Efficiency in Wide Output Loading Range**
- **Outputs Programmable with I^2C Interface**
- **2.4V to 6.4V Programmable for Both Outputs**
- **Factory Programmable Default Outputs:**
  SGM3804-0: V_{PO} = +5.4V/V_{NO} = -5.4V
  SGM3804-1: V_{PO} = +4.6V/V_{NO} = -3.5V
  SGM3804-2: V_{PO} = +5.0V/V_{NO} = -5.0V
  SGM3804-3: V_{PO} = +4.6V/V_{NO} = -2.4V
  SGM3804-4: V_{PO} = +6.4V/V_{NO} = -6.4V
- **1.6MHz Switching plus Pulse-Skip Operation**
- **Configurable Stop Active Discharge**
- **Slim Package Fits into *65132 Footprint**

APPLICATIONS

AMOLED/LCD Smart-Phones/Pads/Media-Players
Wearable Device Display/Audio
AFE with Positive & Negative Rails

TYPICAL APPLICATION

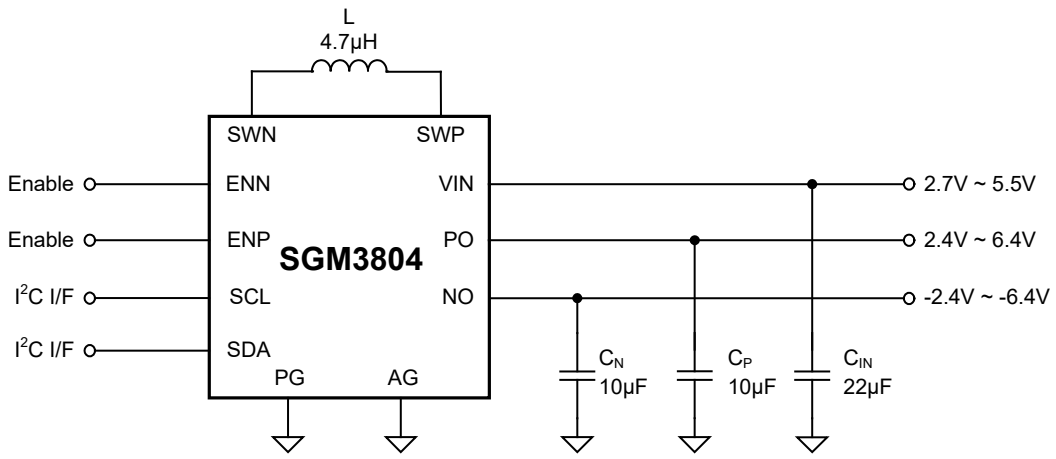


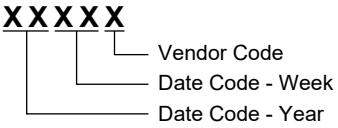
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM3804-0	WLCSP-1.7×1.51-12B	-40℃ to +85℃	SGM3804-0YG/TR	XXXXX G0AYG	Tape and Reel, 3000
SGM3804-1	WLCSP-1.7×1.51-12B	-40℃ to +85℃	SGM3804-1YG/TR	XXXXX G16YG	Tape and Reel, 3000
SGM3804-2	WLCSP-1.7×1.51-12B	-40℃ to +85℃	SGM3804-2YG/TR	XXXXX G54YG	Tape and Reel, 3000
SGM3804-3	WLCSP-1.7×1.51-12B	-40℃ to +85℃	SGM3804-3YG/TR	XXXXX G55YG	Tape and Reel, 3000
SGM3804-4	WLCSP-1.7×1.51-12B	-40℃ to +85℃	SGM3804-4YG/TR	XXXXX G56YG	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... -0.3V to 6V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
MM 400V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.7V to 5.5V
Environmental Temperature Range ..... -40℃ to +85℃
Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

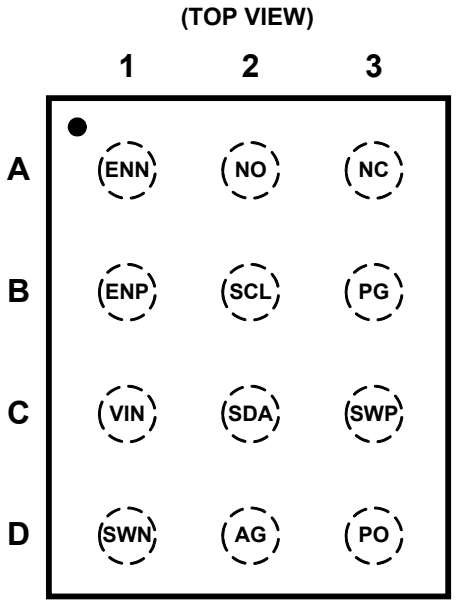
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



WLCSP-1.7×1.51-12B

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
A1	ENN	I	Enable for Negative-Rail Output.
A2	NO	O	Negative-Rail Output.
A3	NC	I	No Connection.
B1	ENP	I	Enable for Positive-Rail Output.
B2	SCL	I	I²C Interface Clock Signal Pin.
B3	PG	–	Power Ground.
C1	VIN	–	Supply Input.
C2	SDA	I/O	I²C Interface Data Signal Pin.
C3	SWP	O	Switch Node for Powering the Positive-Rail. Connect this pin to one end of power inductor.
D1	SWN	O	Switch Node for Powering the Negative-Rail. Connect this pin to the other end of power inductor.
D2	AG	–	Analog Ground.
D3	PO	O	Positive-Rail Output.

FUNCTIONAL BLOCK DIAGRAM

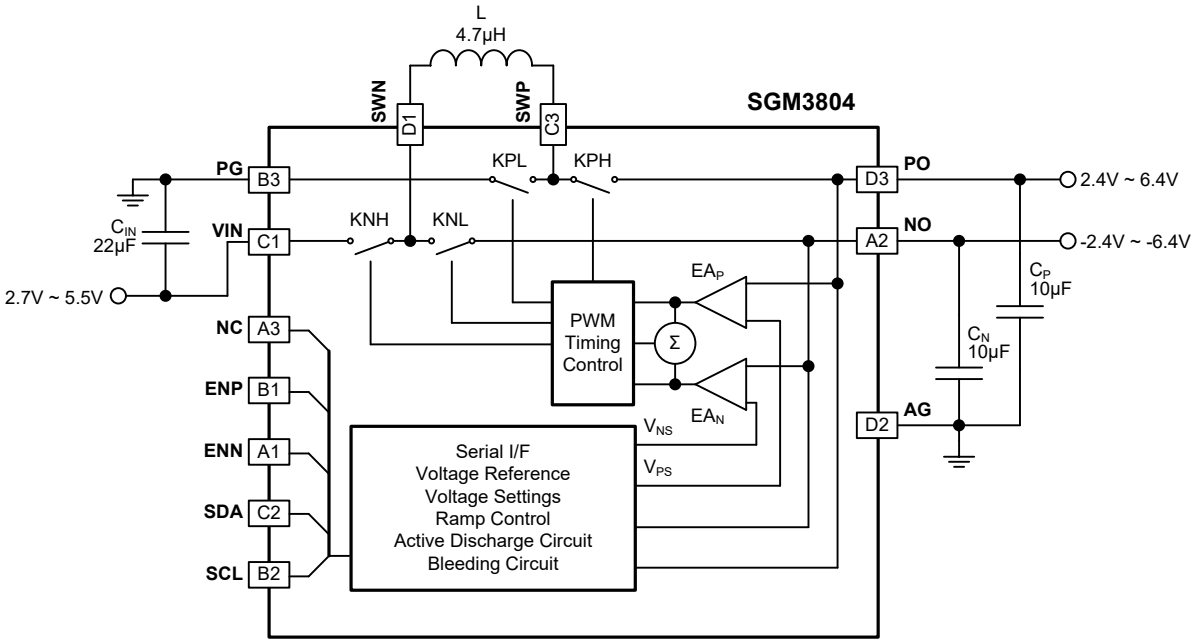


Figure 2. SGM3804 Functional Block Diagram

RECOMMENDED APPLICATION CIRCUIT

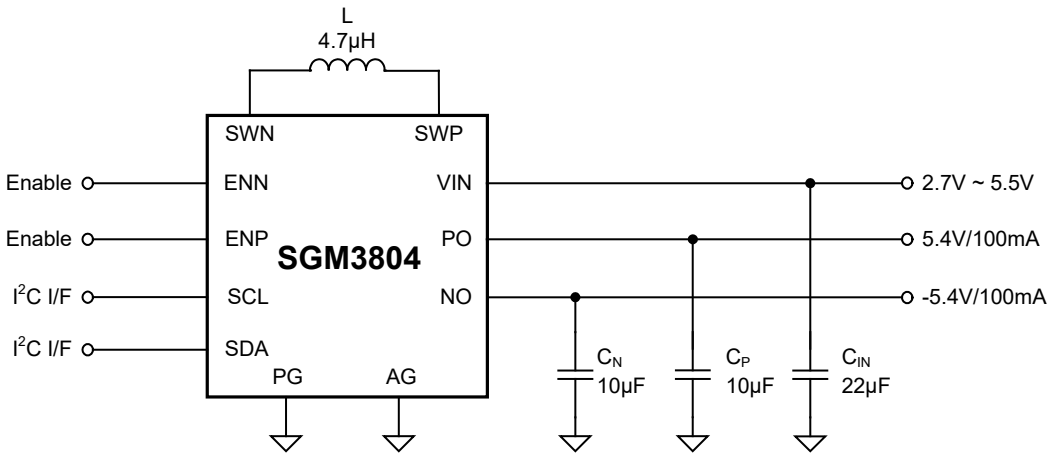


Figure 3. Recommended Application Circuit

ELECTRICAL CHARACTERISTICS

(Test at Full = -40℃ to +85℃, T_A = +25℃, V_{IN} = 3.7V, ENP = ENN = V_{IN}, unless otherwise specified noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
General Features							
Input Voltage Range	V_{IN}		+25℃	2.7		5.5	V
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling	+25℃		2.2	2.65	V
Supply Current with No Load	I_S	V_{IN} = 3.7V, no switching	+25℃		0.4	0.55	mA
		V_{IN} = 3.7V, switching	+25℃		0.78		
Shutdown Current	I_{OFF}	V_{IN} = 3.7V, ENP = ENN = GND	+25℃		0.4	1	μA
Power-On Blanking Time	t_{BLANK}	V_{IN} = 3.7V	+25℃		40		ms
Switching Frequency	f_{SW}	V_{IN} = 3.7V	+25℃	1.48	1.6	1.72	MHz
Inductor Peak Current	I_{PEAK}	V_{IN} = 3.7V	+25℃	1.3	1.55	1.85	A
Positive Output Voltage Range	V_{PO}		+25℃	2.4		6.4	V
Positive Output Voltage Accuracy	$V_{PO\_ACC\_54}$	V_{IN} = 3.7V, V_{PO} = +5.4V	+25℃	-60		60	mV
	$V_{PO\_ACC\_35}$	V_{IN} = 3.7V, V_{PO} = +3.5V	+25℃	-60		60	mV
Discharge Resistor of Positive Output	R_{DP}		+25℃		50		Ω
Discharge Time of Positive Output	t_{DISP}		+25℃		10		ms
Negative Output Voltage Range	V_{NO}		+25℃	-6.4		-2.4	V
Negative Output Voltage Accuracy	$V_{NO\_ACC\_54}$	V_{IN} = 3.7V, V_{NO} = -5.4V	+25℃	-65		65	mV
	$V_{NO\_ACC\_35}$	V_{IN} = 3.7V, V_{NO} = -3.5V	+25℃	-60		60	mV
Discharge Resistor of Negative Output	R_{DN}		+25℃		50		Ω
Discharge Time of Negative Output	t_{DISN}		+25℃		10		ms
LOGIC ENN, ENP, SCL, SDA							
Low Level Input Voltage	V_{IL}	V_{IN} = 2.7V to 5.5V	Full			0.4	V
High Level Input Voltage	V_{IH}	V_{IN} = 2.7V to 5.5V	Full	1.05			V
ENN and ENP Pull-Down Resistors	R_{EN}		+25℃		200		kΩ

I²C INTERFACE TIMING CHARACTERISTICS (1)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard mode	+25℃			100	kHz
		Fast mode	+25℃			400	kHz
LOW Period of the SCL Clock	t_{LOW}	Standard mode	+25℃	4.7			μs
		Fast mode	+25℃	1.3			μs
HIGH Period of the SCL Clock	t_{HIGH}	Standard mode	+25℃	4.0			μs
		Fast mode	+25℃	600			ns
Bus Free Time between a STOP and a START Conditions	t_{BUF}	Standard mode	+25℃	4.7			μs
		Fast mode	+25℃	1.3			μs
Hold Time for a Repeated START Condition	$t_{hd;STA}$	Standard mode	+25℃	4.0			μs
		Fast mode	+25℃	600			ns
Setup Time for a Repeated START Condition	$t_{su;STA}$	Standard mode	+25℃	4.7			μs
		Fast mode	+25℃	600			ns
Data Setup Time	$t_{su;DAT}$	Standard mode	+25℃	250			ns
		Fast mode	+25℃	100			ns
Data Hold Time	$t_{hd;DAT}$	Standard mode	+25℃	0.05		3.45	μs
		Fast mode	+25℃	0.05		0.9	μs
Rise Time of SCL Signal after a Repeated START Condition and after an Acknowledge Bit	t_{RCL1}	Standard mode	+25℃	$20 + 0.1C_B$		1000	ns
		Fast mode	+25℃	$20 + 0.1C_B$		1000	ns
Rise Time of SCL Signal	t_{RCL}	Standard mode	+25℃	$20 + 0.1C_B$		1000	ns
		Fast mode	+25℃	$20 + 0.1C_B$		300	ns
Fall Time of SCL Signal	t_{FCL}	Standard mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode	+25℃	$20 + 0.1C_B$		300	ns
Rise Time of SDA Signal	t_{RDA}	Standard mode	+25℃	$20 + 0.1C_B$		1000	ns
		Fast mode	+25℃	$20 + 0.1C_B$		300	ns
Fall Time of SDA Signal	t_{FDA}	Standard mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode	+25℃	$20 + 0.1C_B$		300	ns
Setup Time for STOP Condition	$t_{su;STO}$	Standard mode	+25℃	4.0			μs
		Fast mode	+25℃	600			ns
Capacitive Load for SDA and SCL	C_B		+25℃			0.4	nF

NOTE:
1. Industry standard I²C timing characteristics according to I²C-Bus Specification. Not tested in production.

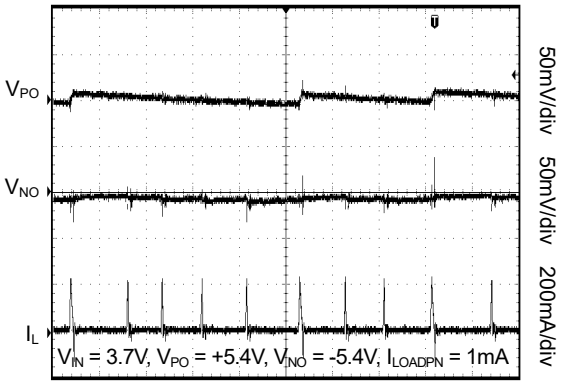
RECOMMENDED COMPONENTS OF TEST CIRCUITS

	COMPONENT		COMPONENT
INDUCTOR	SLF7055T-4R7N3R1-3PF	CAPACITOR	10μF/08055C106KAT2A
			22μF/C2012X7R1H226KT

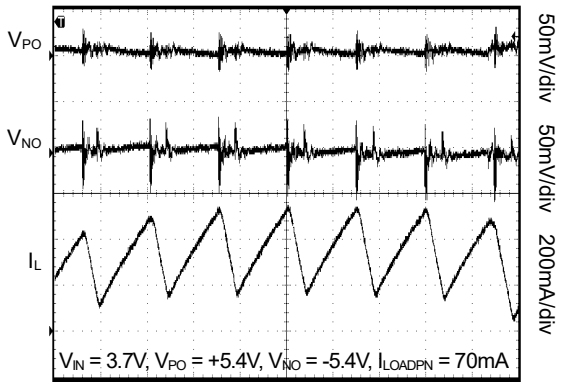
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 3.7V, V_{PO} = +5.4V, V_{NO} = -5.4V, unless otherwise noted.

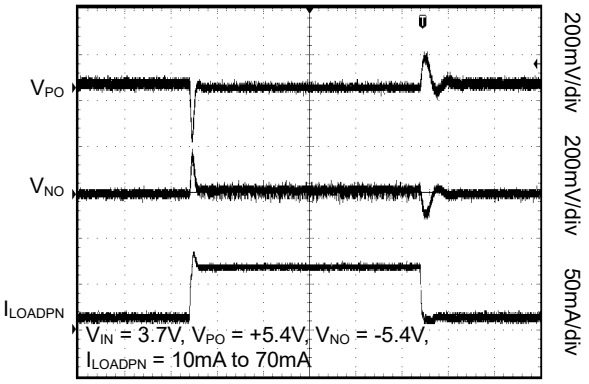
Light Load



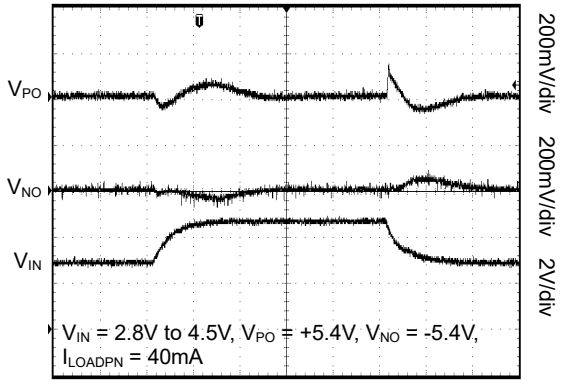
Heavy Load



Load Transient



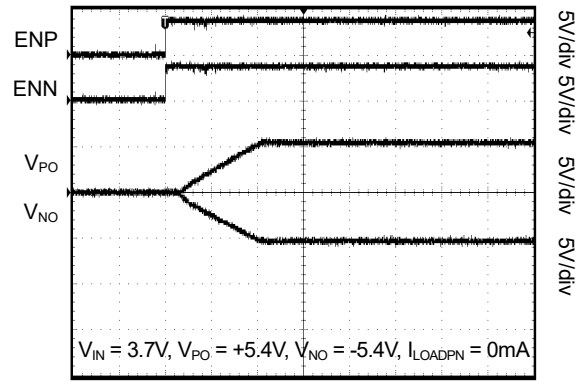
Line Transient



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

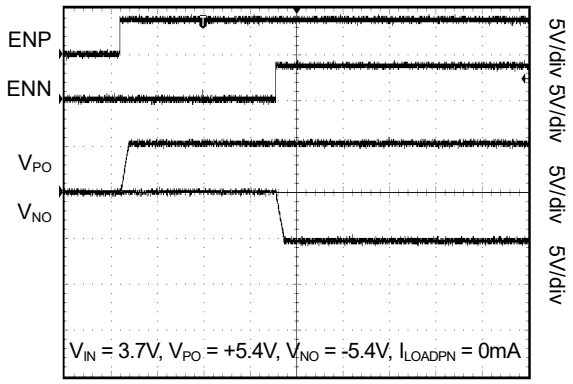
T_A = +25℃, V_{IN} = 3.7V, V_{PO} = +5.4V, V_{NO} = -5.4V, unless otherwise noted.

Power-Up Sequencing



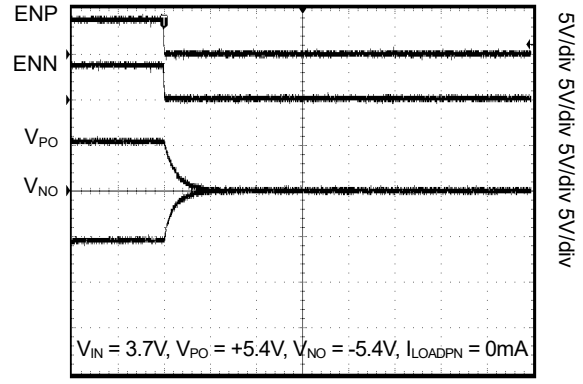
Time (1ms/div)

Power-Up Sequencing



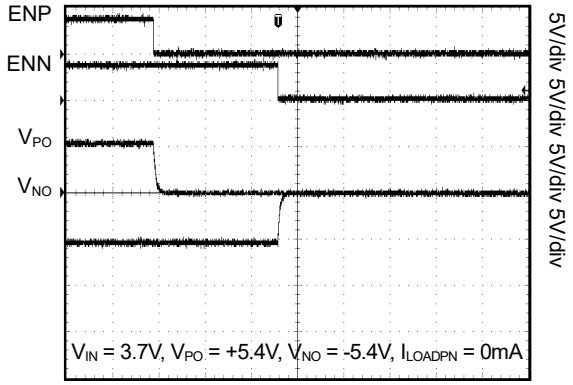
Time (10ms/div)

Power-Down Sequencing



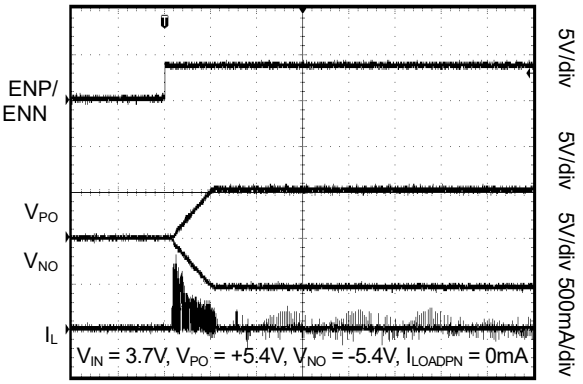
Time (2ms/div)

Power-Down Sequencing



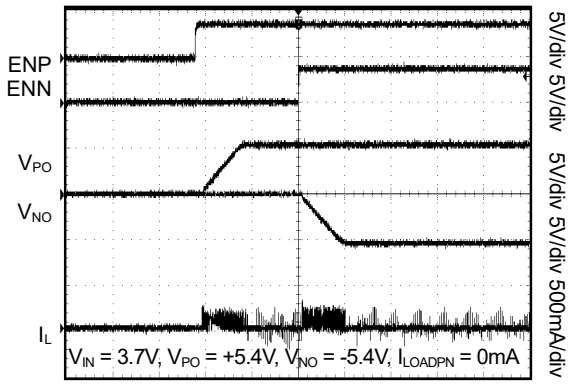
Time (10ms/div)

Inrush Current



Time (2ms/div)

Inrush Current

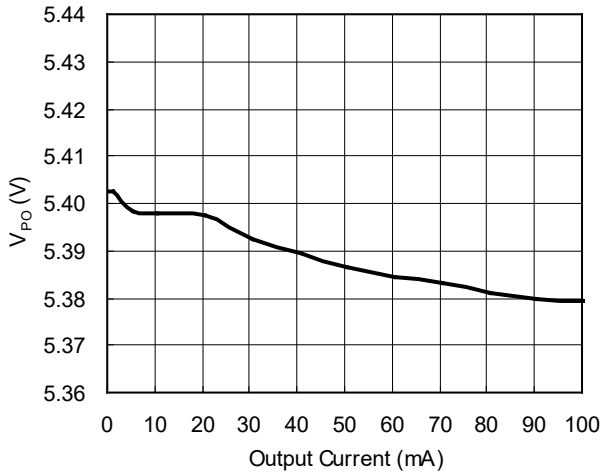


Time (2ms/div)

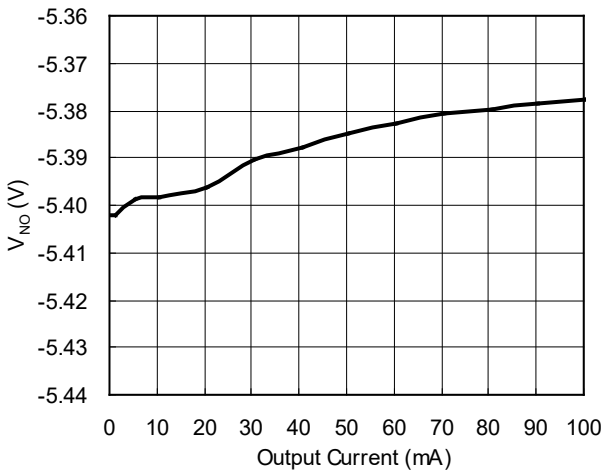
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 3.7V, V_{PO} = +5.4V, V_{NO} = -5.4V, unless otherwise noted.

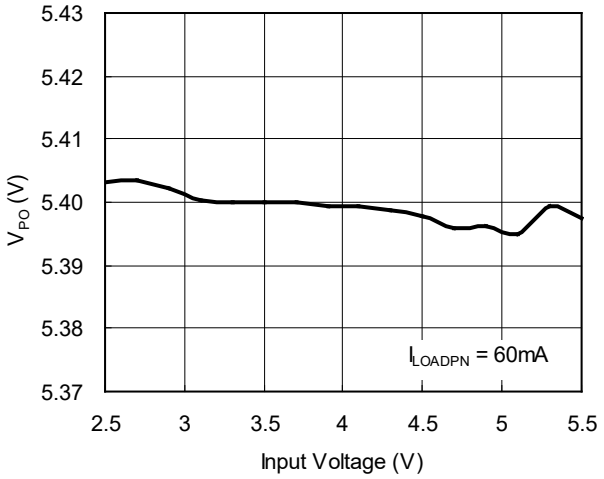
Positive Output Voltage vs. Output Current



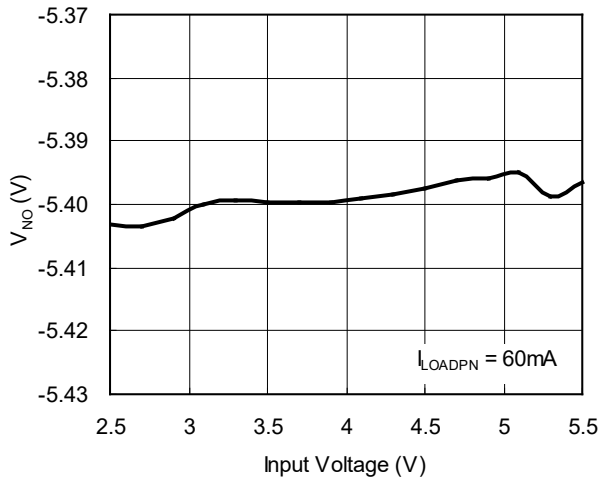
Negative Output Voltage vs. Output Current



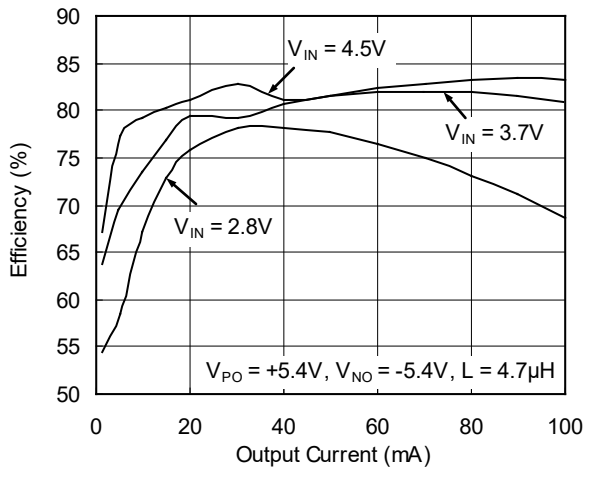
Positive Output Voltage vs. Input Voltage



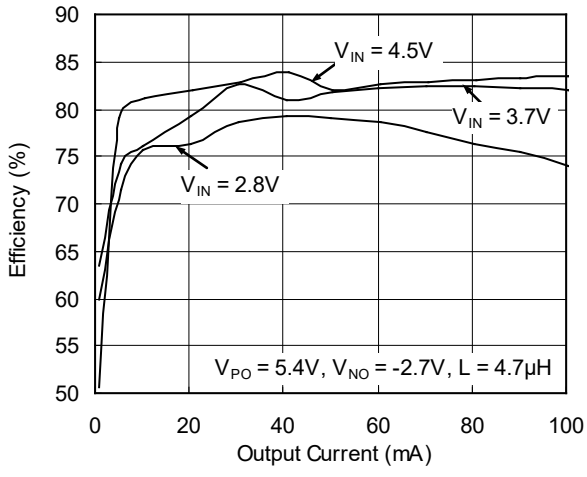
Negative Output Voltage vs. Input Voltage



Efficiency vs. Output Current



Efficiency vs. Output Current



CONTROLS AND LOGIC DIAGRAMS

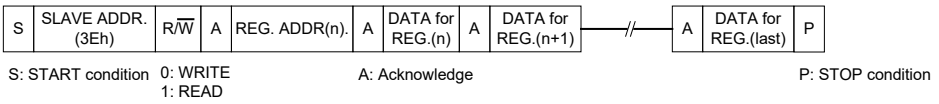


Figure 4. I²C Transfer Format Register Address Auto-Increment

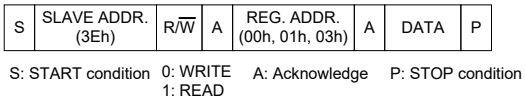


Figure 5. I²C Transfer Format Writing into a Single Register

Register Address Mapping

P: Programmable default value.

REG. ADDR.	BIT SYMBOLS AND DEFAULTS [7:0]							
	D7	D6	D5	D4	D3	D2	D1	D0
0x00			Bit5P	Bit4P	Bit3P	Bit2P	Bit1P	Bit0P
			P	P	P	P	P	P
0x01			Bit5N	Bit4N	Bit3N	Bit2N	Bit1N	Bit0N
			P	P	P	P	P	P
0x03						ADD50	DISP	DISN
						0	1	1

NOTE: Spaces left blank are not used, which could be filled with any value when programming.

Registers and Bits Descriptions

P: factory preset, W: write only bits, R/$\overline{W}$: free read or write bits. Blank for no predictable status or not care.

REG.	SYMBOL	BIT	DEFAULT	TYPE	DESCRIPTION
0x00	Bit5P	D5	P	W	Voltage code bit5 for positive rail.
0x00	Bit4P	D4	P	W	Voltage code bit4 for positive rail.
0x00	Bit3P	D3	P	W	Voltage code bit3 for positive rail.
0x00	Bit2P	D2	P	W	Voltage code bit2 for positive rail.
0x00	Bit1P	D1	P	W	Voltage code bit1 for positive rail.
0x00	Bit0P	D0	P	W	Voltage code bit0 for positive rail.
0x01	Bit5N	D5	P	W	Voltage code bit5 for negative rail.
0x01	Bit4N	D4	P	W	Voltage code bit4 for negative rail.
0x01	Bit3N	D3	P	W	Voltage code bit3 for negative rail.
0x01	Bit2N	D2	P	W	Voltage code bit2 for negative rail.
0x01	Bit1N	D1	P	W	Voltage code bit1 for negative rail.
0x01	Bit0N	D0	P	W	Voltage code bit0 for negative rail.
0x03	ADD50	D2	0	W	0: Keep the coded voltage specified with <Bit5N:Bit0N>; 1: Shift the negative rail voltage 50mV lower than the coded value.
0x03	DISP	D1	1	W	0: Disable positive rail discharge; 1: Enable positive rail discharge.
0x03	DISN	D0	1	W	0: Disable negative rail discharge; 1: Enable negative rail discharge.

CONTROLS AND LOGIC DIAGRAMS (continued)

Voltage Codes to Voltage Value Mapping

Codes (1)	Negative Voltage (V)	Positive Voltage (V)	Codes (1)	Negative Voltage (V)	Positive Voltage (V)	Codes (1)	Negative Voltage (V)	Positive Voltage (V)
18h	-6.4	6.4	**0Ah**	-5	5	**2Ch**	-3.6	3.6
17h	-6.3	6.3	**09h**	-4.9	4.9	**2Bh**	-3.5	3.5
16h	-6.2	6.2	**08h**	-4.8	4.8	**2Ah**	-3.4	3.4
15h	-6.1	6.1	**07h**	-4.7	4.7	**29h**	-3.3	3.3
14h	-6.0	6.0	**06h**	-4.6	4.6	**28h**	-3.2	3.2
13h	-5.9	5.9	**05h**	-4.5	4.5	**27h**	-3.1	3.1
12h	-5.8	5.8	**04h**	-4.4	4.4	**26h**	-3.0	3.0
11h	-5.7	5.7	**03h**	-4.3	4.3	**25h**	-2.9	2.9
10h	-5.6	5.6	**02h**	-4.2	4.2	**24h**	-2.8	2.8
0Fh	-5.5	5.5	**01h**	-4.1	4.1	**23h**	-2.7	2.7
0Eh	-5.4	5.4	**00h**	-4.0	4.0	**22h**	-2.6	2.6
0Dh	-5.3	5.3	**2Fh**	-3.9	3.9	**21h**	-2.5	2.5
0Ch	-5.2	5.2	**2Eh**	-3.8	3.8	**20h**	-2.4	2.4
0Bh	-5.1	5.1	**2Dh**	-3.7	3.7			

NOTE:
1. CODES = <Bit5P:Bit0P> = <Bit5N:Bit0N> with I^2C interface.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

OCTOBER 2016 – REV.A to REV.A.1 **Page**

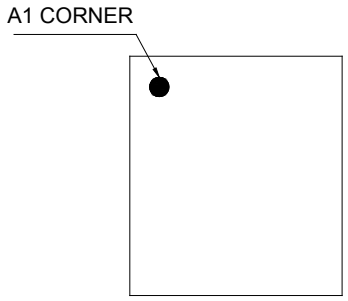
Changed Electrical Characteristics section 5
Changed Recommended Components of Test Circuits section 7

Changes from Original (JANUARY 2016) to REV.A **Page**

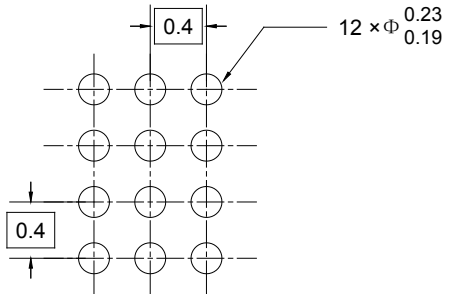
Changed from product preview to production data ..... All

PACKAGE OUTLINE DIMENSIONS

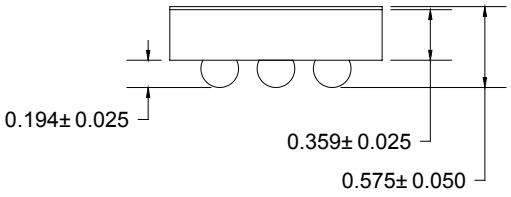
WLCSP-1.7×1.51-12B



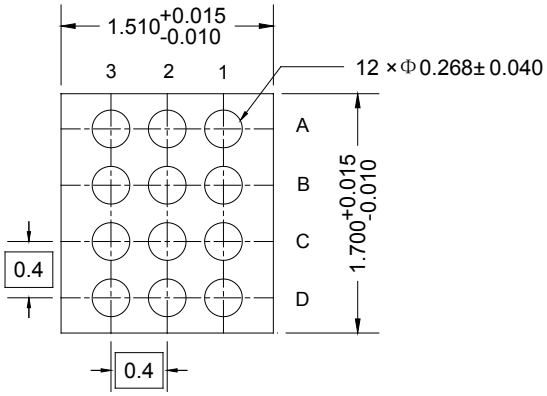
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

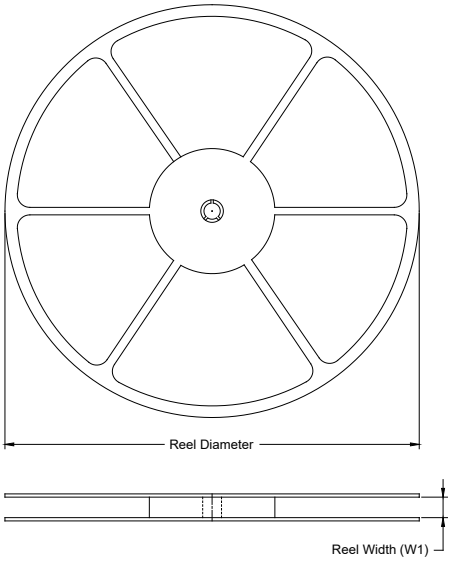


BOTTOM VIEW

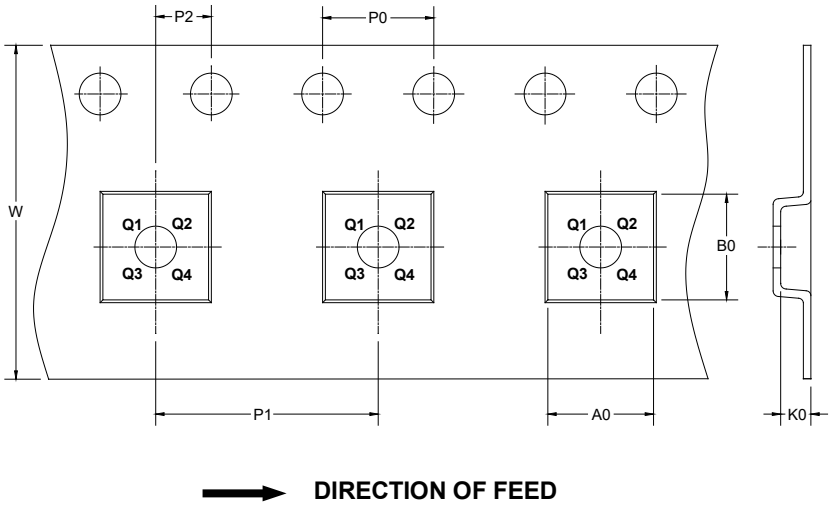
NOTE: All linear dimensions are in millimeters.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



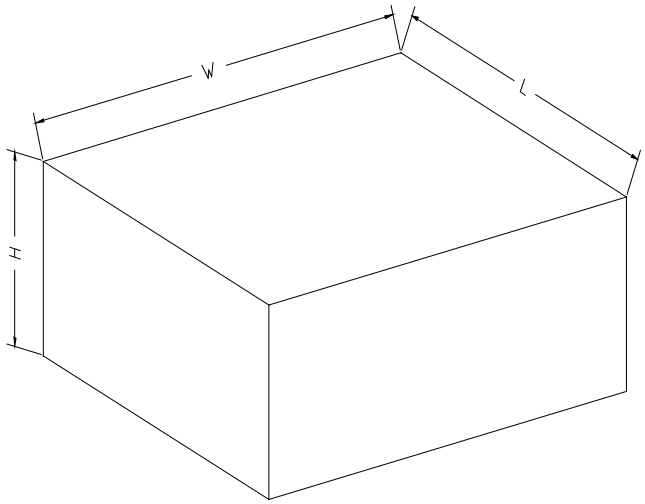
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.7×1.51-12B	7″	9.5	1.70	2.00	0.80	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002