High Efficiency 1.2MHz 28V Output, 2A Step Up Regulator

CJ9340 Series

■ INTRODUCTION

The CJ9340 is a constant frequency, currentmode step-up converter intended for small, low power applications. The CJ9340 switches at 1.2MHz and allows the use of tiny, low cost capacitors and inductors 2mm or less in height. Internal soft-start results in small inrush current and extends battery life.

The CJ9340 includes under-voltage lockout, current limiting, and thermal overload protection to prevent damage in the event of an output overload. The CJ9340 is available in a small 6-pin SOT-23 package.

■ FEATURES

- 2V to 24V Input Voltage
- Up to 28V Output Voltage
- Integrated 80mΩ Power MOSFET
- 1.2MHz Fixed Switching Frequency
- Internal 4A Switch Current Limit
- Internal Compensation
- Thermal Shutdown
- Output Adjustable from 0.6V
- Available in a 6-pin SOT-23 package

■ APPLICATIONS

- Digital Set-top Box (STB)
- Tablet Personal Computer (Pad)
- LCD Bias Supply
- Battery-Powered Equipment
- Portable Media Player (PMP)
- General Purposes

■ DEVICE INFORMATION:

PART NUMBER	PACKAGE
CJ9340T6	SOT-23-6L

■ Typical Application

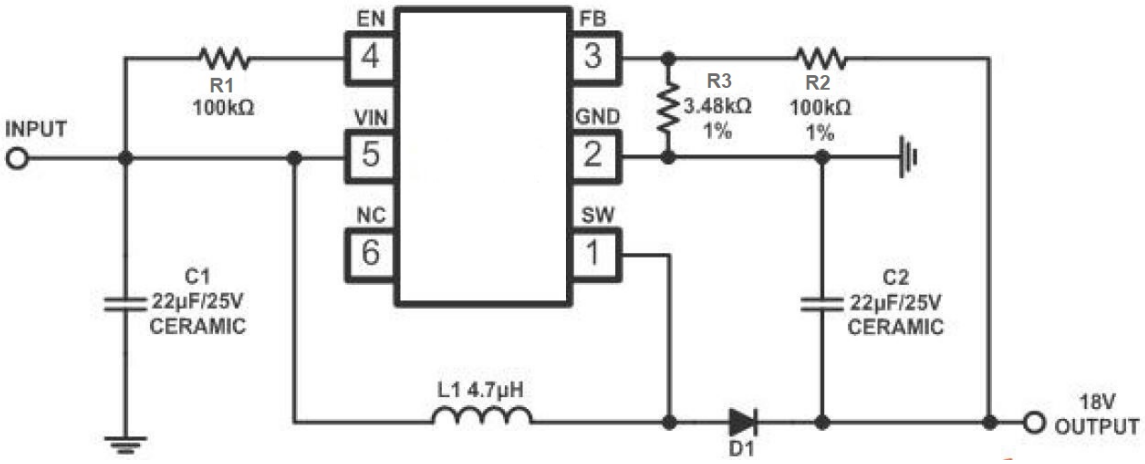


Figure1. Basic Application Circuit

■ Functional Block Diagram

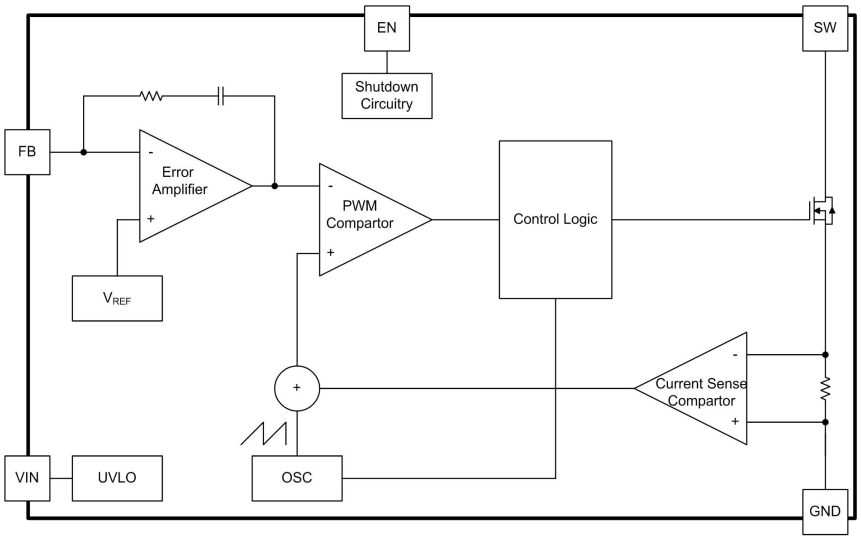
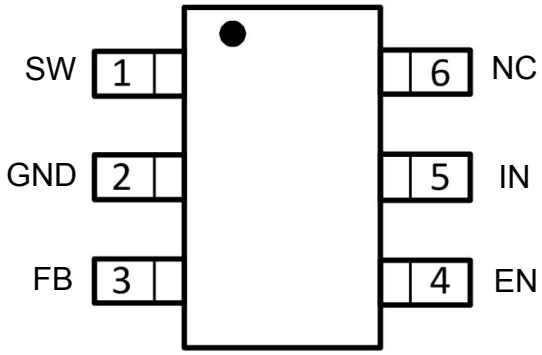


Figure 2. CJ9340 Block Diagram

■ Pin Description

PIN	NAME	FUNCTION
1	SW	Power Switch Output. SW is the drain of the internal MOSFET switch. Connect the power inductor and output rectifier to SW. SW can swing between GND and 28V.
2	GND	Ground Pin
3	FB	Feedback Input. The FB voltage is 0.6V. Connect a resistor divider to FB.
4	EN	Regulator On/Off Control Input. A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input supply for automatic startup.
5	IN	Input Supply Pin. Must be locally bypassed.
6	NC	Not Connection

■ Package/order Information



(SOT-23-6L)

■ Absolute Maximum Ratings (Note 1)

PARAMETER	ABSOLUTE MAXIMUM RATINGS	UNIT
V_{IN}, V_{EN}	-0.3 to 26	V
V_{SW}	-0.3 to 26	V
All Other Pins	-0.3 to 6	V
Continuous Power Dissipation(T_A=+25℃)	0.6	W
Junction Temperature	150	°C
Operating Temperature Range	-40 to 85	
Lead Temperature	260	°C
Storage Temperature	-65 to 150	°C
Thermal Resistance θ_{JA}	250	°C /W
Thermal Resistance θ_{JC}	130	°C /W

■ Recommended Operating Conditions

PARAMETER	RECOMMENDED	UNIT
Supply Voltage V_{IN}	2 to 24	V
Output Voltage V_{OUT}	V_{IN} to 28	V
Operating Junction Temp.(T_J)	-40 to 125	°C

■ Electrical Charcteristics (Note 3)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current(Shutdown)	I_{IN}	V_{EN}=0V		0.1	1	μA
Quiescent Current (PFM)		V_{FB}=0.7V,No switch		50	100	μA
Quiescent Current (PWM)		V_{FB}=0.5V,switch		0.2	0.4	mA
SW Leakage		V_{SW} = 20V			1	μA
SW On Resistance				80	150	mΩ
Operating Input Voltage			2		24	V
Current Limit	I_{LIMIT}	V_{IN}= 5V,Duty cycle=50%		4		A
Oscillator Frequency	f_{SW}	V_{FB}=0.75V		1.2		MHz
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.7V		90		%
Feedback Voltage	V_{FB}		588	600	612	mV
FB Input Bias Current		V_{FB}=0.6V	-50	-10		nA
EN Threshold	V_{EN}			1		V
Thermal Shutdown				160		°C

■ Operation

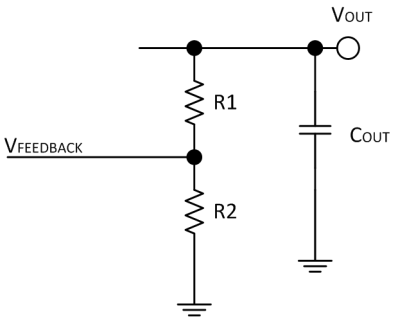
The CJ9340 uses a fixed frequency, peak current mode boost regulator architecture to regulate voltage at the feedback pin. The operation of the CJ9340 can be understood by referring to the block diagram of Figure 3. At the start of each oscillator cycle the MOSFET is turned on through the control circuitry. To prevent sub-harmonic oscillations at duty cycles greater than 50 percent, a stabilizing ramp is added to the output of the current sense amplifier and the result is fed into the negative input of the PWM comparator. When this voltage equals The output voltage of the error amplifier the power MOSFET is turned off. The voltage at the output of the error amplifier is an amplified version of the difference between the 0.6V band gap reference voltage and the feedback voltage. In this way the peak current level keeps the output in regulation. If the feedback voltage starts to drop, the output of the error amplifier increases. These results in more current to flow through the power MOSFET, thus increasing the power delivered to the output. The CJ9340 has internal soft start to limit the amount of input current at startup and to also limit the amount of overshoot on the output.

■ Applications Information

Setting the Output Voltage

CJ9340 are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FB} \times \frac{R_1 + R_2}{R_2}$$



Inductor Selection

The CJ9340 boost converter can utilize small surface mount and chip inductors due to the fast 1.2MHz switching frequency. Inductor values between 2.2μH and 10μH are suitable for most applications. Larger values of inductance will allow slightly greater output current capability by reducing the inductor ripple current. Increasing the inductance above 10μH will increase size while providing little improvement in output current capability. The minimum boost inductance value is given by:

$$L > \frac{V_{IN} \times (V_{OUT} + V_{DIODE} - V_{IN})}{F_S \times I_{RIPPLE} \times (V_{OUT} + V_{DIODE})}$$

Where

• IRIPPLE：Peak-to-Peak inductor current

• VIN：Input voltage

• VOUT：Output voltage

•VDIODE：Output diode Forward Voltage

• FS：Switching frequency, Hertz

The inductor current ripple is typically set for 20% to40% of the maximum inductor current. High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low DCR(series resistance of the winding) to reduce the I2R power losses, and must not saturate at peak inductor current levels. Molded chokes and some chip inductors usually.

Capacitor Selection

The internal loop compensation of the CJ9340 boost converter is designed to be stable with output capacitor values of 10μF or greater. Low ESR (equivalent series resistance) capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. A 10μF to 22μF output capacitor is sufficient for most fixed frequency applications. For applications where Burst Mode operation is enabled, a minimum value of 22μF is recommended. Larger values may be used to obtain very low output ripple and to improve transient response. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges. Y5V types should not be used. Case sizes smaller than 0805 are not recommended due to their increased DC bias effect.

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. It follows that ceramic capacitors are also a good choice for input decoupling and should be located as close as possible to the device. A 22μF input capacitor connected to inductor is sufficient for most applications. Larger values maybe used without limitations. For applications where the power source is more than a few inches away, a larger bulk decoupling capacitor is recommended on the input to the boost converter.

Diode Selection

A Schottky diode should be used for the output diode. The forward current rating of the diode should be higher than the load current, and the reverse voltage rating must be higher than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds

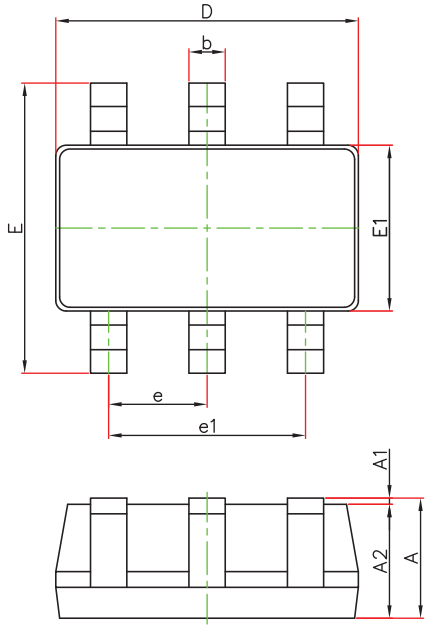
and long recovery times cause the efficiency and the load regulation to suffer.

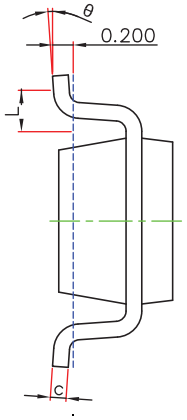
Layout Consideration

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the CIN input capacitor, to the regulator VIN terminal, to the regulator SW terminal, to the inductor then out to the output capacitor COUT and load. The second loop starts from the output capacitor ground, to the regulator GND terminals, to the inductor and then out to COUT and the load. To minimize both loop areas the input capacitor should be placed as close as possible to the VIN terminal. Grounding for both the input and output capacitors should consist of a small localized topside plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected together then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

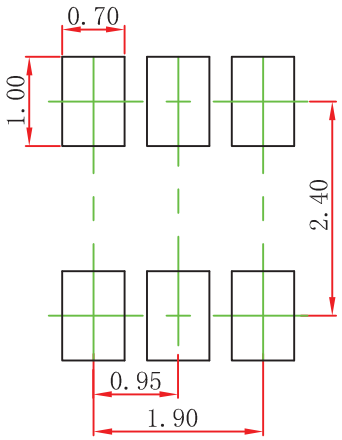
SOT-23-6L Package Outline Dimensions





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-23-6L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

DISCLAIMER

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