产品特性

- 48pin LQFP 封装
- 支持处理器接口：8 位、16 位对内部存储器访问
- 集成 10/100M 收发器，支持 HP Auto-MDIX 检测
- 用于半双工时，支持 back pressure 流控模式
- 用于全双工时，支持 IEEE802.3x 流控模式
- 支持唤醒帧、link 状态变化、magic packet 事件等远程唤醒
- 支持 100M 光纤接口
- 内建 16K 字节 SRAM
- 内建 3.3V 转 2.5V 稳压器
- 支持 IP/TCP/UDP checksum 产生和检查
- 支持从 EEPROM 自动装载 vendor ID, product ID.
- 可选的 EEPROM 配置
- 低功耗操作模式
- Power reduced mode
- Power down mode
- 可选的 tx drivers 1:1 或 1.25:1 变压器
- 兼容 3.3V 和 5V tolerant I/O

产品应用

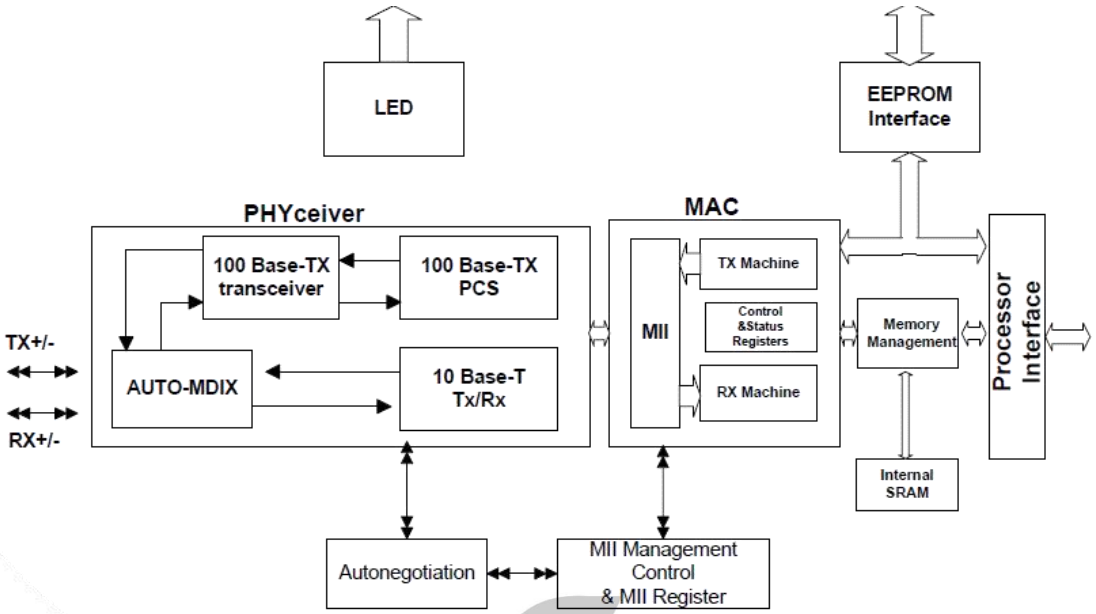
- 家庭网络设备：机顶盒、个人录像机、数码媒体适配器
- 串行转以太网：门禁控制、LED 显示屏、无线 AP 继电器等
- 并行转以太网：POS/微型打印机、复印机
- USB 转以太网：存储设备、网络打印机
- GPIO 转以太网：家庭网络传感器
- 安全系统：数字录像机、网络摄像机、信息亭
- 工厂和楼宇自动化控制系统
- 医疗监测设备
- 嵌入式服务器

产品描述

CBM1001A-Q 是一款集成了 10/100M PHY, MAC 层的高性价比的快速以太网控制器芯片，内建 16K 字节 SRAM，对外提供了一个通用的处理器访问接口。本芯片具备低功耗，高性能的优良特性，支持 3.3V IO 电平，并可以接受 5V 输入 IO 电压。

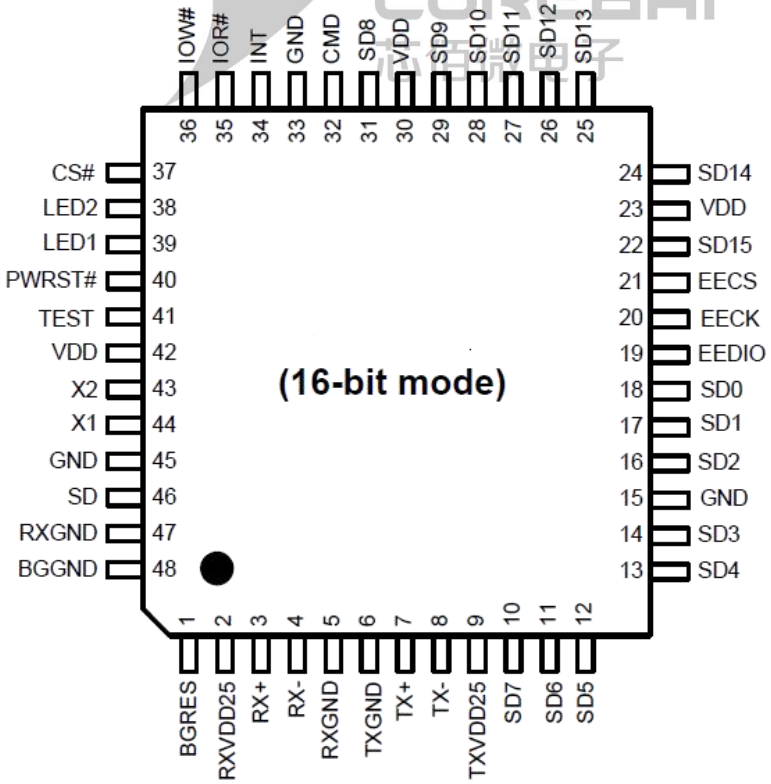
CBM1001 支持 8 位和 16 位数据接口，用于访问内部的 SRAM。内建的 PHY 可以支持 UTP3,4,5 10Base-T 及 UTP5 100Base-TX。完全符合 IEEE 802.3u 规格。支持自动协商功能。

功能框图

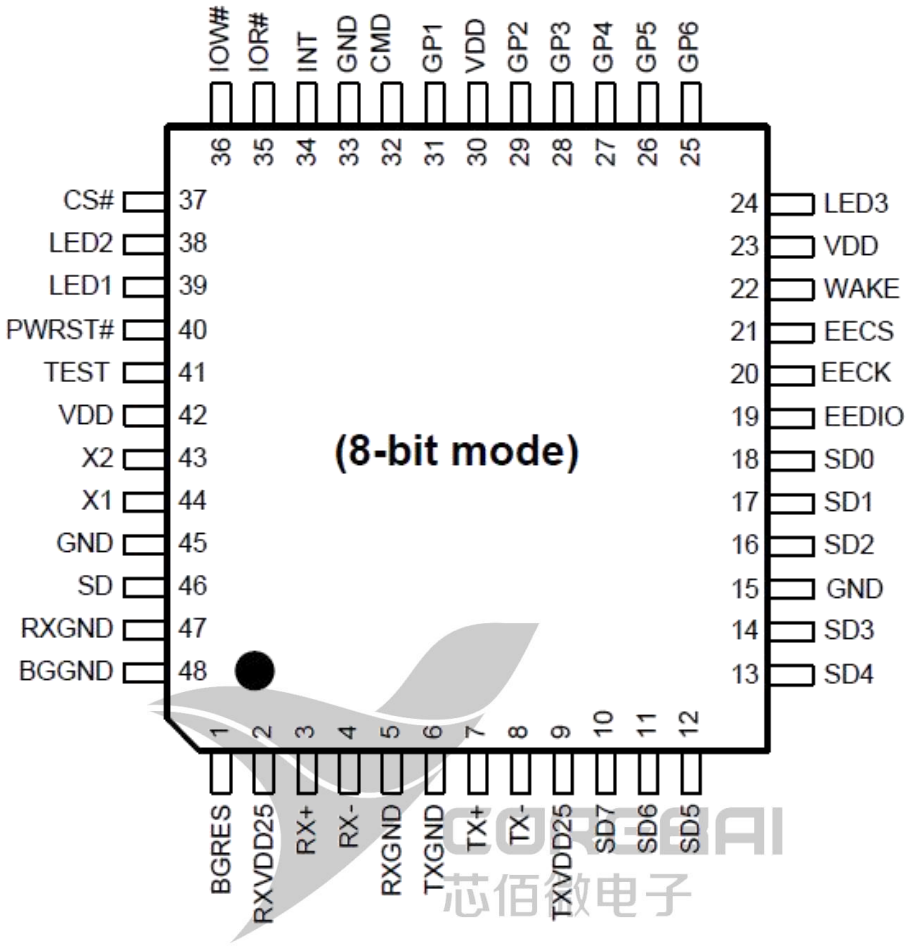


引脚配置

16 位模式



8 位模式



引脚简述

管脚编号	引脚名称	类型	说明
Processor Interface			
35	IOR#	I,PD	Processor read command
36	IOW#	I,PD	Processor write command
37	CS#	I,PD	Chip select
32	CMD	I,PD	Command type
34	INT	O,PD	Interrupt Request
18,17,16, 14,13,12,	SD0~7	I/O,PD	Processor Data Bus bit 0~7

11,10			
31,29,28, 27,26,25, 24,22	SD8~15	I/O,PD	Processor Data Bus bit 8~15
8-bit mode pins			
22	WAKE	O,PD	Issue a wake up signal when wake up event happens
24	LED3	O,PD	Full-duplex LED
25,26,27	GP6~4	O,PD	General Purpose output pins
28,29,31	GP3,GP2,GP1	I/O	General I/O ports
EEPROM interface			
19	EEDIO	I/O,PD	IO data to eeprom
20	EECK	O,PD	Clock to eeprom
21	EECS	O,PD	Chip select to eeprom
Clock interface			
43	X2	O	Crystal 25Mhz out
44	X1	I	Crystal 25Mhz in
LED interface			
39	LED1	O	Speed LED
38	LED2	O	Link/Active LED
46	SD	I	Fiber-optic signal detect
48	BGGND	P	Bandgap ground
1	BGRES	I/O	Bandgap pin
2	RXVDD25	P	2.5V power output for TP RX
9	TXVDD25	P	2.5V power output for TP TX
3	RX+	I/O	TP RX input
4	RX-	I/O	TP RX input
5,47	RXGND	P	RX Ground
6	TXGND	P	TX Ground
7	TX+	I/O	TP TX output
8	TX-	I/O	TP TX output
Others			
41	TEST	I	Test mode
40	PWRST#	I	Power on reset

23,30,42	VDD	P	Digital VDD, 3.3V power input
15,33,45	GND	P	Digital GND

寄存器说明

MAC 寄存器

Register	Description	Offset	Default value
NCR	Network control register	00H	00H
NSR	Network Status register	01H	00H
NCR	TX control register	02H	00H
TSR I	TX status register I	03H	00H
TSR II	TX status register II	04H	00H
RCR	RX control register	05H	00H
RSR	RX status register	06H	00H
ROCR	Receive overflow counter register	07H	00H
BPTR	Back pressure threshold register	08H	37H
FCTR	Flow control threshold register	09H	38H
FCR	RX flow control register	0AH	00H
EPCR	EEPROM & PHY control register	0BH	00H
EPAR	EEPROM & PHY address register	0CH	40H
EPDRL	EEPROM & PHY low byte data register	0DH	xxH
EPDRH	EEPROM & PHY high byte data register	0EH	xxH
WCR	Wake Up Control Register (in 8 bit mode)	0FH	00H
PAR	Physical address register	10H~15H	Determined by eeprom
MAR	Multicast address register	16H-1DH	xxH
GPCR	General purpose control register (in 8-bit mode)	1EH	01H
GPR	General purpose register	1FH	xxH
TRPAL	TX SRAM read pointer address low byte	22H	00H
TRPAH	TX SRAM read pointer address high byte	23H	00H
RWPAL	RX SRAM write pointer address low byte	24H	00H
RWPAH	RX SRAM write pointer address high byte	25H	0CH
VID	Vendor ID	28H~29H	0A46H

PID	Product ID	2AH~2BH	9000H
CHIPR	CHIP revision	2CH	19H
TCR2	TX control register 2	2DH	00H
OCR	Operation control register	2EH	00H
SMCR	Special mode control register	2FH	00H
ETXCSR	Early transmit control/status register	30H	00H
TCSCR	Transmit check sum control register	31H	00H
RCSCSR	Receive check sum control status register	32H	00H
MPAR	MII PHY address register	33H	00H
LEDCR	LED pin control register	34H	00H
BUSCR	Processor bus control register	38H	61H
INTCR	INT pin control register	39H	00H
SCCR	System clock tum on control register	50H	00H
RSCCR	Resume system clock control register	51H	XXH
MRCMDX	Memory data pre-fetch read command without address increment register	F0H	XXH
MRCMDX1	Memory data read command with address increment register	F1H	XXH
MRCMD	Memory data read command with address increment register	F2H	XXH
MRRL	Memory data read address register low byte	F4H	00H
MRRH	Memory data read address register high byte	F5H	00H
MWCMDX	Memory data write command without address increment register	F6H	XXH
MWCMD	Memory data write command with address increment register	F8H	XXH
MWRL	Memory data write address register low byte	FAH	00H
MWRH	Memory data wirte address register high byte	FBH	00H
TXPLL	TX packet length low byte register	FCH	XXH

TXPLH	TX packet length high byte register	FDH	XXH
ISR	Interrupt status register	FEH	00H
IMR	Interrupt mask register	FFH	00H

PHY 寄存器

ADD	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	CONTROL	Reset	Loop back	Speed select	Auto-N Enable	Power Down	Isolate	Restart Auto-N	Full Duplex	Coll. Test	Reserved						
		0	0	1	1	0	0	0	1	0	000_0000						
01	STATUS	T4 Cap.	TX FDX Cap.	TX HDX Cap.	10 FDX Cap.	10 HDX Cap.	Reserved				Pream. Supr.	Auto-N Compl.	Remote Fault	Auto-N Cap.	Link Status	Jabber Detect	Extd Cap.
		0	1	1	1	1	0000				1	0	0	1	0	0	1
02	PHYID1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
03	PHYID2	1	0	1	1	1	0	Model No.					Version No.				
								01010					0000				
04	Auto-Neg. Advertise	Next Page	FLP Rcv Ack	Remote Fault	Reserved		FC Adv	T4 Adv	TX FDX Adv	TX HDX Adv	10 FDX Adv	10 HDX Adv	Advertised Protocol Selector Field				
05	Link Part. Ability	LP Next Page	LP Ack	LP RF	Reserved		LP FC	LP T4	LP TX FDX	LP TX HDX	LP 10 FDX	LP 10 HDX	Link Partner Protocol Selector Field				
06	Auto-Neg. Expansion	Reserved											Pardet Fault	LP Next Pg Able	Next Pg Able	New Pg Rcv	LP AutoN Cap.
16	Specified Config.	BP 4B5B	BP SCR	BP ALIGN	BP_ADP OK	Reserved	TX	Reserved	Reserved	Force 100LNK	Reserved	Reserved	RPDCTR-EN	Reset St. Mch	Pream. Supr.	Sleep mode	Remote LoopOut
17	Specified Conf/Stat	100 FDX	100 HDX	10 FDX	10 HDX	Reserved	Reversed	Reversed	PHY ADDR [4:0]				Auto-N. Monitor Bit [3:0]				
18	10T Conf/Stat	Rsvd	LP Enable	HBE Enable	SQUE Enable	JAB Enable	Reserved	Reserved									Polarity Reverse
19	PWDOR	Reserved							PD10DRV	PD100I	PDchip	PDcrm	PDaeq	PDdrv	PDecli	PDecto	PD10
20	Specified config	TSTSE1	TSTSE2	FORCE_TXSD	FORCE_FEF	Reserved				MDIX_CNTL	AutoNeg_lpbk	Mdix_fix Value	Mdix_down	MonSel1	MonSel0	Reserved	PD_value

功能说明

主机接口

主机接口是一个通用的处理器局部总线接口，采用片选信号 CS#来选中 CBM1001, CS#默认是低有效，可以通过 EEPROM 设定改变极性。主机可通过两路端口，一是 INDEX，二是 DATA，复用 SD 信号，当 CMD=0 时，SD 表示 INDEX 信息；当 CMD=1 时，SD 表示 DATA 信息。INDEX 是要访问的寄存器的地址信息，在访问任何寄存器前，需要先设置 INDEX 信息。

DMA 控制

CBM1001 提供了 DMA 支持，用于简化对内部存储器的访问。在配置存储器的起始地址后，首先发送一个 dummy read/write 命令，装载当前数据到内部数据缓冲器，然后，可以通过 read/write 命令访问目标地址。地址将按照 8 位或 16 位模式自动递增。下一地址的数据被自动装载入数据缓冲器。

内部存储器大小是 16K 字节，前 3K 字节用于发送，后 13KB 字节用于接收。

帧发送

TX SRAM 可以存储两个包，分别命名为 Index I 和 Index II。Index register 02h 控制 CRC 和 pads 的插入。状态在 03h 和 04h 寄存器内记录。硬件或软件复位后，发送起始地址位于 00h, Index I 有效。

首先写入数据到 TX SRAM，然后写入数据大小到 byte_count register fch 和 fdh。设置 control register 的 bit1 后，CBM1001 开始发送 index I 包。在 index I 包发送完成前，index II 的包数据可以写入 TX SRAM，在 index I 发送完成后，可以马上设置 index II 的 byte_count 和 control register 的 bit1。这样 index I 和 index II 可循环交替发送。

帧接收

RX SRAM 是 ring 的结构。在硬件或软件复位后，RX SRAM 的起始地址位于 C00h 处。每个包拥有 4 字节的 header，跟随接收到的数据，包括 CRC 数据。Header 的结构是 01h, status, byte_count low, byte_count high。

收发器操作

100Base TX 操作

发送包括 4B5B encoder, scrambler, parallel to serial converter, NRZ to NRZI 转换，NRZI 到 MLT-3 转换，最后经 MLT-3 驱动器驱动信号到线缆。

接收包括 signal decteck，数字自适应均衡器，MLT-3 到 binary 译码器，时钟恢复模块，NRZI 到 NRZ 译码器，串行到并行转换器，descrambler 解扰，编码对齐，4B5B 译码器。

10Base-T 操作

10Base-T 收发器符合 IEEE 802.3u 标准，当 CBM1001 工作在 10base-t 模式，编码方案是曼彻斯特编码，

电气特性

操作条件

Symbol	Parameter	Min	Max	Unit	Conditions
D_{VDD}	Supply Voltage	3.135	3.465	V	
Tc	Case Reserve	-	85	℃	
P_D (Power DIssipation)	100BASE-TX	-	87	mA	3.3V
	10BASE-T TX(100% utilization)	-	92	mA	3.3V
	10BASE-T idle	-	38	mA	3.3V
	Auto-negotiation	-	56	mA	3.3V
	Power Reduced Mode(without cable)	-	31	mA	3.3V
	Power Down Mode	-	21	mA	3.3V
	Power Down Mode (system clock off)	-	7	mA	3.3V

直流电气特性

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
Input						
V_{IL}	Input Low Voltage	-	-	0.8	V	
V_{IL}	Input High Voltage	2.0	-	-	V	
I_{IL}	Input Low Leakage Current	-1	-	-	uA	VIN=0.0V
I_{IH}	Input High Leakage Current	-	-	1	uA	VIN=3.3V
Cin	Input capapcitance	4	5	6	pf	
Outputs						
V_{OL}	Output Low Voltage	-	-	0.4	V	IOL=4mA
V_{OH}	Output High Voltage	2.4	-	-	V	IOH=-4mA
Receiver						
V_{ICM}	RX+/RX-Common Mode Input Voltage	-	2.5	-	V	100Ω Termination Across
Transmitter						
V_{TD100}	100TX+/-Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
V_{TD10}	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
I_{TD100}	100TX+/- Differential Output Current	|19|	|20|	|21|	mA	Absolute Value

交流特性

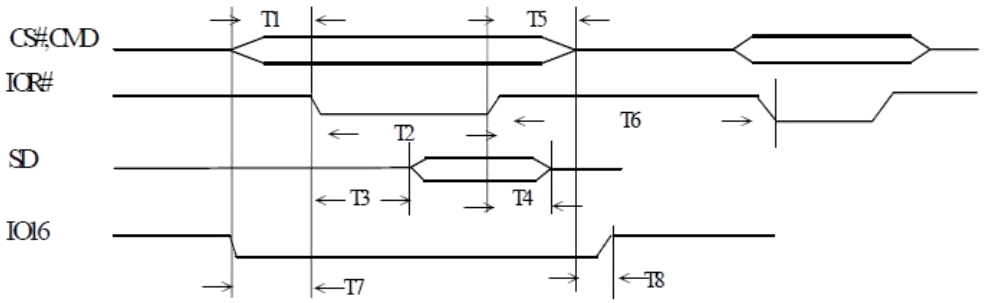
TP 接口

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$t_{TR/F}$	100TX+/- Differential Rise/Fall Time	3.0	-	5.0	ns	
t_{TM}	100TX+/- Differential Rise/Fall Time Mismatch	0	-	0.5	ns	
t_{TDC}	100TX+/- Differential Output Duty Cycle Distortion	0	-	0.5	ns	
$T_{t/T}$	100TX+/- Differential Output Peak-to-Peak Jitter	0	-	1.4	ns	
X_{OST}	100TX+/- Differential Voltage Overshoot	0	-	5	%	

晶振时序

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
T_{CKC}	OSC Clock Cycle	39.998	40	40.002	ns	50ppm
T_{PWH}	OSC Pulse Width High	16	20	24	ns	
T_{PWL}	OSC Pulse Width Low	16	20	24	ns	

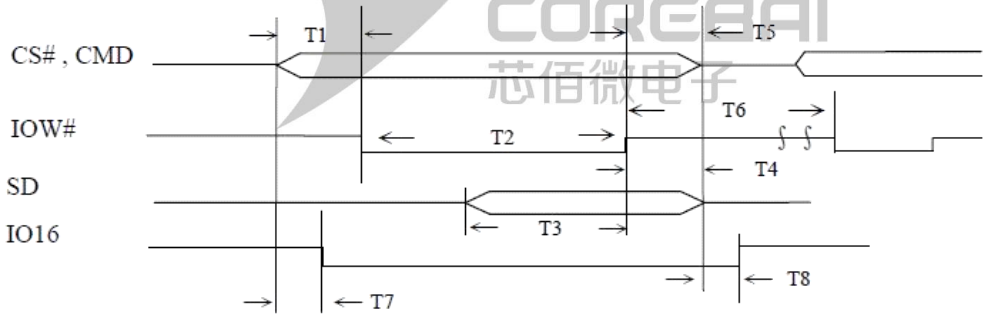
处理器读时序



Symbol	Parameter	Min	Typ	Max	Unit
T_1	CS#,CMD valid to IOR# valid	0			ns

T_2	IOR# width	10			ns
T_3	System Date(SD) Delay time			3	ns
T_4	IOR# invalid to System Date(SD) invalid			3	ns
T_5	IOR# invalid to CS#,CMD invalid	0			ns
T_6	IOR# invalid to next IOR#/IOW# valid When read CBM1001 register	2			clk*
T_6	IOR# invalid to next IOR#/IOW# valid When read CBM1001 memory withF2h register	4			clk*
T_2+T_6	IOR# invalid to next IOR#/IOW# valid When read CBM1001 memory with F2h register	1			clk*
T_7	CS#,CMD valid to IO 16 valid			3	ns
T_8	CS#,CMD invalid to IO16 invalid			3	ns

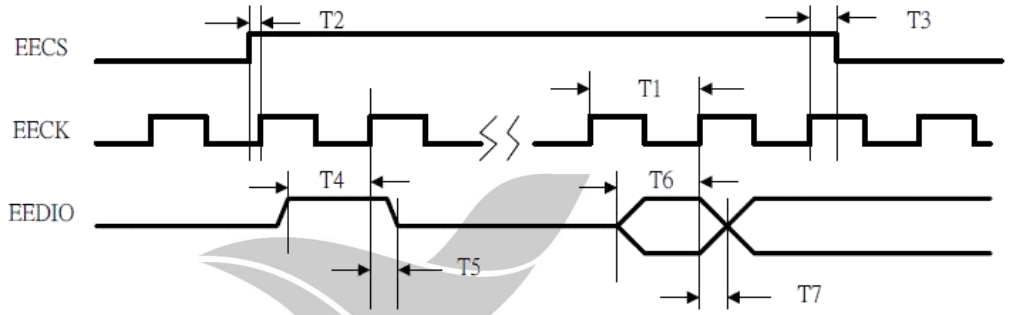
处理器写时序



Symbol	Parameter	Min	Typ	Max	Unit
T_1	CS#,CMD valid to IOW# valid	0			ns
T_2	IOW# width	10			ns
T_3	System Date(SD) Setup time	10			ns
T_4	System Date(SD) Hold time	3			ns
T_5	IOW # Invalid to CS#,CMD invalid	0			ns
T_6	IOW# invalid to next IOW#/IOR# valid When write CBM1001 INDEX port	1			clk*

T_6	IOW# Invalid to next IOW#/IOR# valid When write CBM1001 memory DATE port	2			clk*
T_2+T_6	IOW# invalid to next IOR#/IOW# valid When write CBM1001 memory	1			clk*
T_7	CS#,CMD valid to IO 16 valid			3	ns
T_8	CS#,CMD invalid to IO16 invalid			3	ns

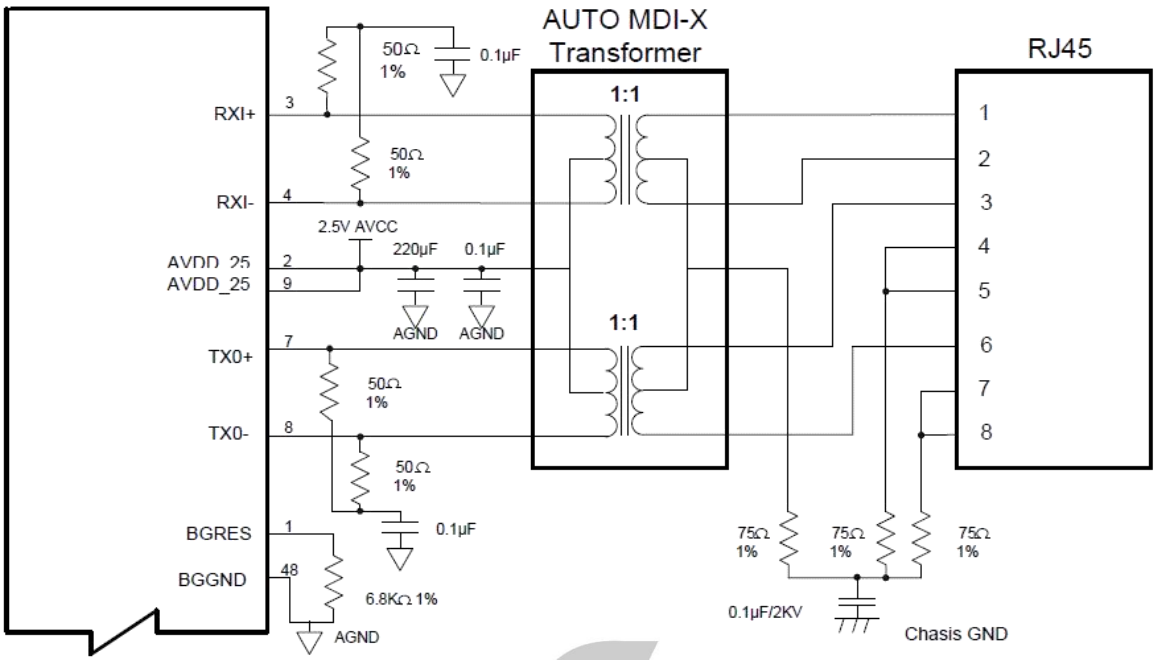
EEPROM 接口时序



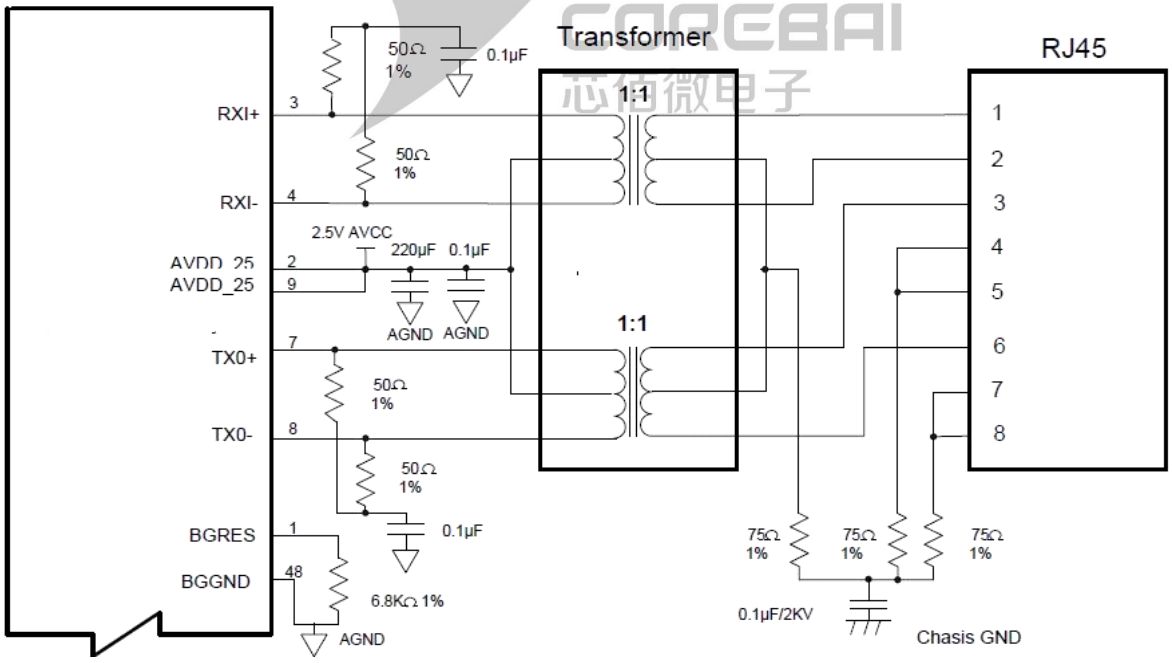
Symbol	Parameter	Min	Typ	Max	Unit
T_1	EECK Frequency		0.375		Mhz
T_2	EECS Setup Time		500		ns
T_3	EECS Hold Time		2166		ns
T_4	EEDIO Setup Time wheno output		480		ns
T_5	EEDIO Hold Time when output		2200		ns
T_6	EEDIO Setup Time when input	8			ns
T_7	EEDIO Hold Time when input	8			ns

应用指南

Auto MDIX 应用

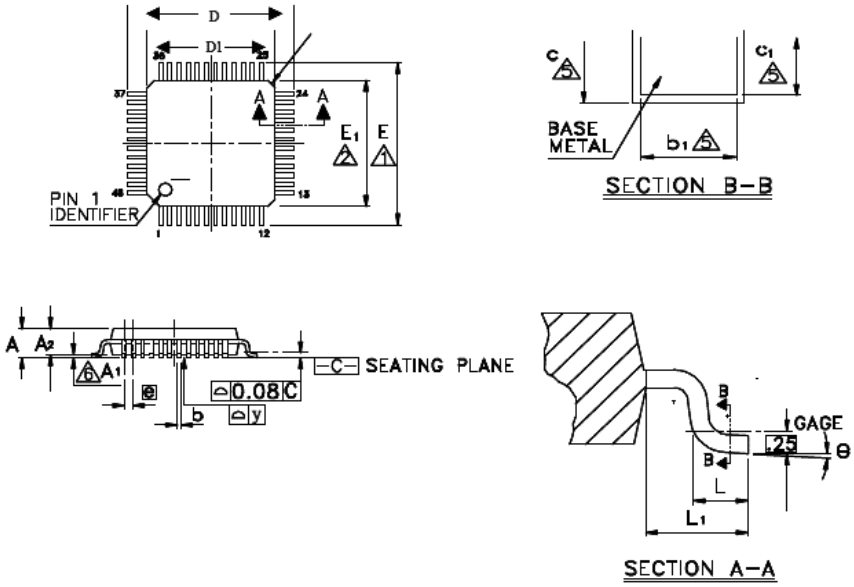


Non auto MDIX 应用



封装信息

LQFP 48L (F.P. 2mm) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.063	-	-	1.60
A1	0.002	-	0.006	0.05	-	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
b1	0.007	0.008	0.009	0.17	0.20	0.23
C	0.004	-	0.008	0.09	-	0.20
C1	0.004	-	0.006	0.09	-	0.16
D	0.354 BSC			9.00 BSC		
D1	0.276 BSC			7.00 BSC		
E	0.354 BSC			9.00 BSC		
E1	0.276 BSC			7.00BSC		
e	0.020 BSC			0.50 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	0.039 REF			1.00 REF		
y	0.003 MAX			0.08 MAX		

1. To be determined at seating plane.
2. Dimensions D1 and E1 do not include mold protrusion.

D1 and E1 are maximum plastic body size dimensions including mold mismatch.

3. Dimensions b does not include dambar protrusion. Total in excess of the b dimensions at maximum material condition. Dambar cannot be located on the lower radius of the foot.
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7. Controlling dimension: millimeter.
8. Reference documents: JEDEC MS-026, BBC.