NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE85H21C uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in automotive applications and a wide variety of other applications.

General Features

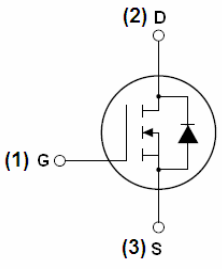
- V_{DSS} =85V,I_D =210A
  $R_{DS(ON)}$ < 4.95mΩ @ V_{GS}=10V
- Good stability and uniformity with high E_{AS}
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

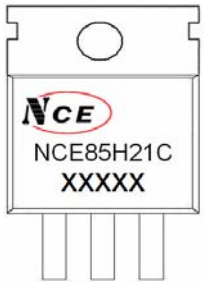
- Automotive applications
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

100% ΔVds TESTED!



Schematic diagram



Marking and pin assignment

TO-220-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE85H21C	NCE85H21C	TO-220	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	85	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	210 (Note5)	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	148	A
Pulsed Drain Current	I_{DM}	850	A
Maximum Power Dissipation	P_D	300	W
Derating factor		2.0	W/℃
Single pulse avalanche energy (Note 3)	E_{AS}	1800	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	5	V/ns
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 1)	$R_{\theta JC}$	0.5	℃/W
Thermal Resistance,Junction-to-Ambient (Note 1)	$R_{\theta JA}$	60	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

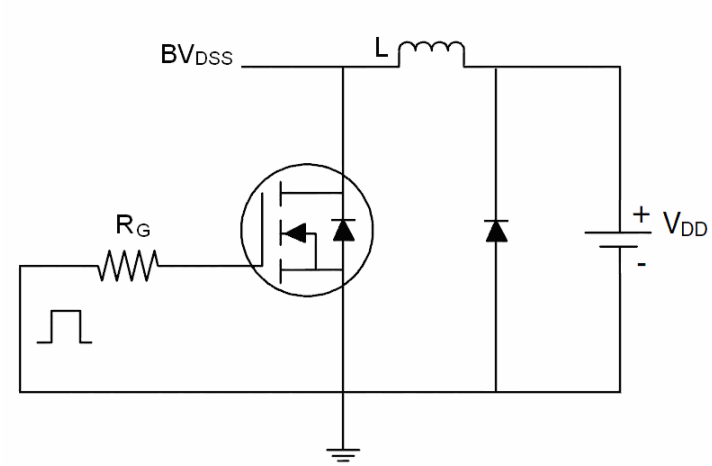
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	85	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=85V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±200	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3.2	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=40A	-	4.1	4.95	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=20A	35	-	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	7600	-	PF
Output Capacitance	C_{oss}		-	720	-	PF
Reverse Transfer Capacitance	C_{rss}		-	346	-	PF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=40V,I_D=40A V_{GS}=10V,R_{GEN}=1.2Ω (Note2)	-	23	-	nS
Turn-on Rise Time	t_r		-	124	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	84	-	nS
Turn-Off Fall Time	t_f		-	78	-	nS
Total Gate Charge	Q_g	V_{DS}=40V,I_D=40A, V_{GS}=10V(Note2)	-	140	-	nC
Gate-Source Charge	Q_{gs}		-	40	-	nC
Gate-Drain Charge	Q_{gd}		-	57	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=40A	-	-	1.2	V
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 40A di/dt = 100A/μs(Note2)	-	110	-	nS
Reverse Recovery Charge	Qrr		-	300	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

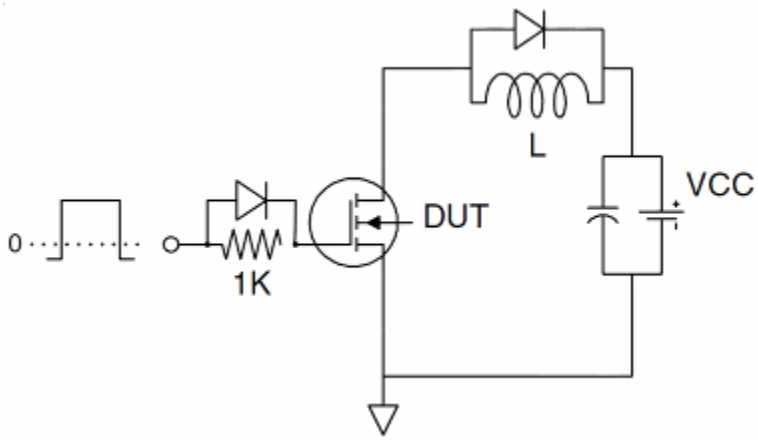
1. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation PDSM is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.
2. Pulse Test: Pulse Width ≤ 400μs, Duty Cycle ≤ 2%.
3. EAS condition：Tj=25℃,V_{DD}=42.5V,V_G=10V,L=0.5mH,Rg=25Ω
4. I_{SD}≤125A, di/dt≤260A/μs, VDD≤$V_{(BR)DSS}$，TJ ≤175°C

Test Circuit

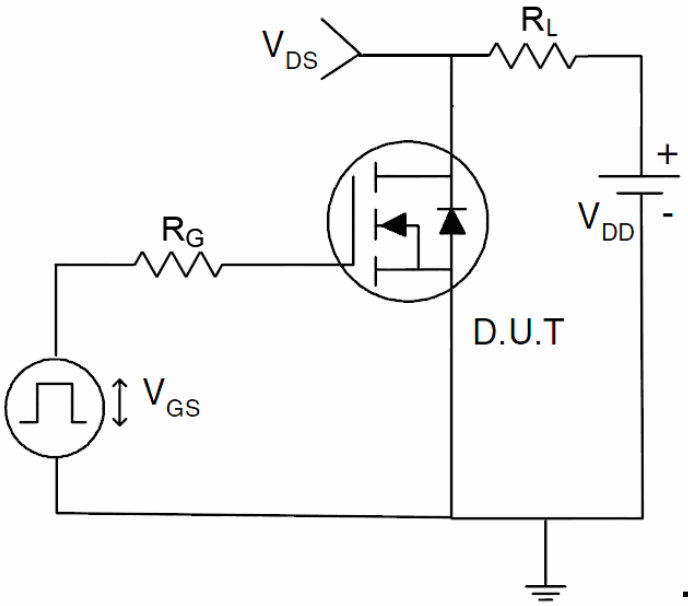
1) E_{AS} test circuit



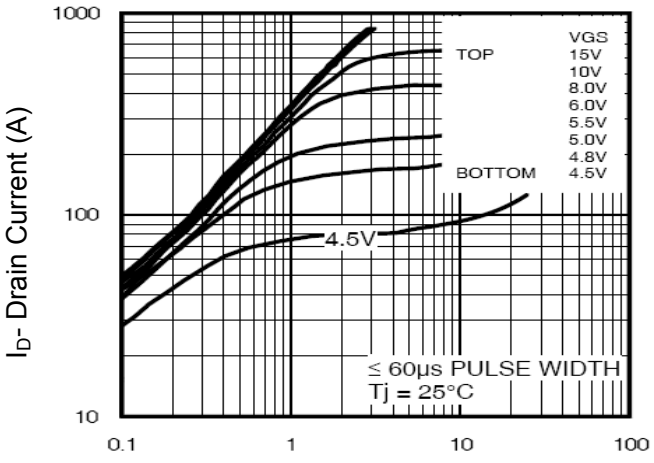
2) Gate charge test circuit



3) Switch time test circuit

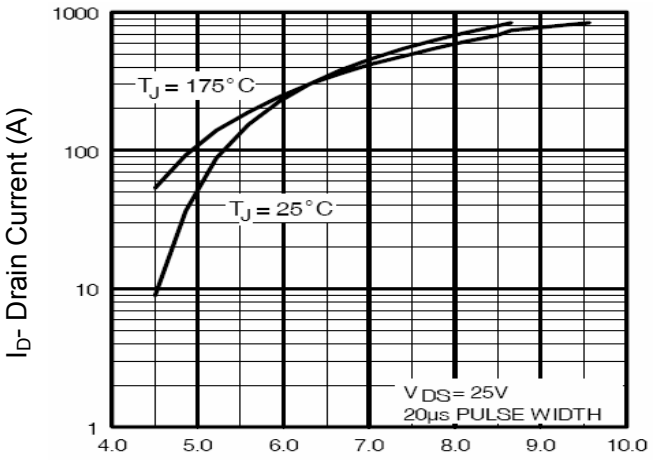


Typical Electrical and Thermal Characteristics



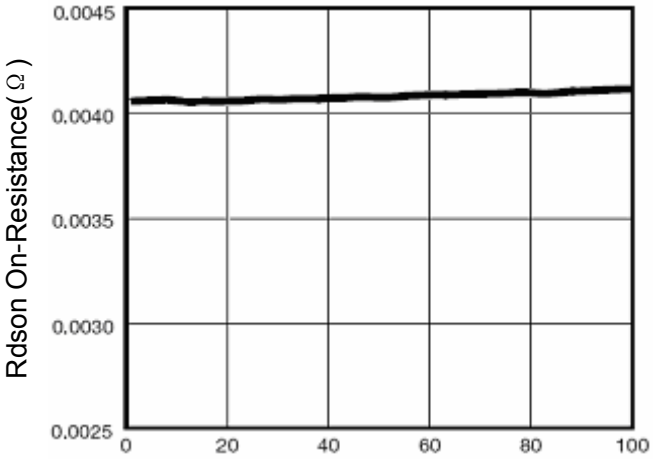
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



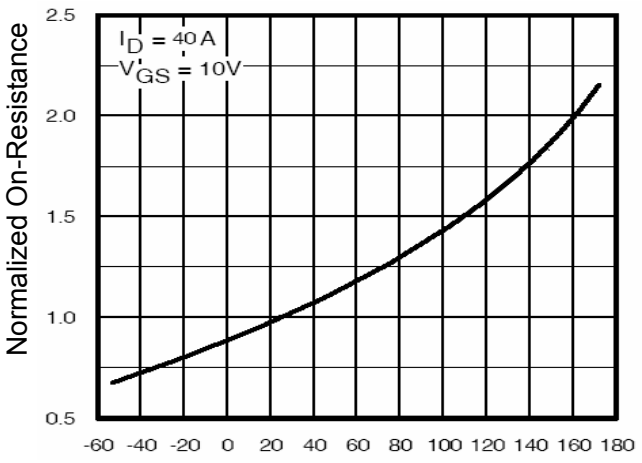
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



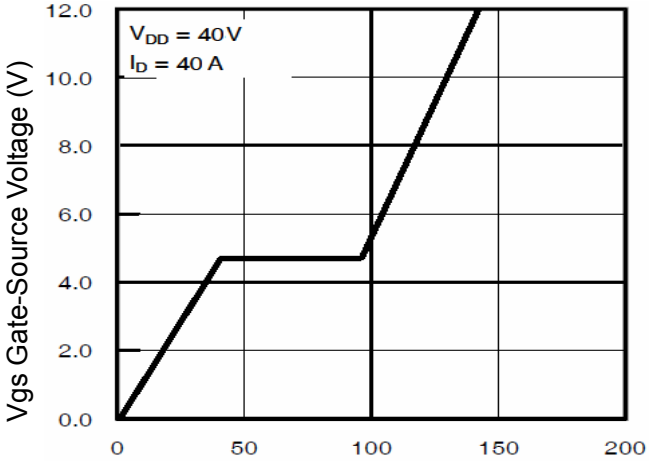
I_D- Drain Current (A)

Figure 3 Rdson- Drain Current



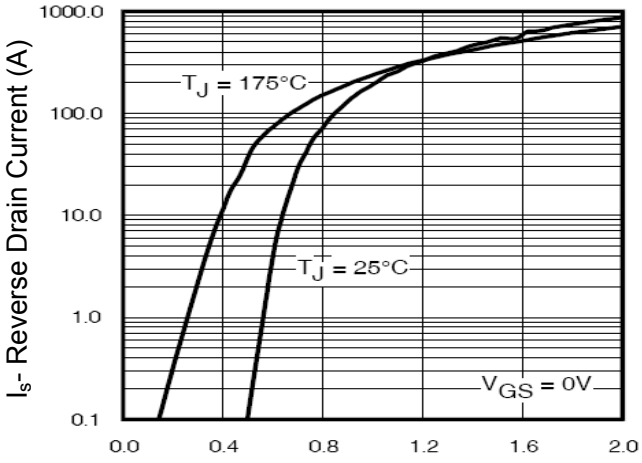
T_J-Junction Temperature(℃)

Figure 4 Rdson-JunctionTemperature



Qg Gate Charge (nC)

Figure 5 Gate Charge



Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward

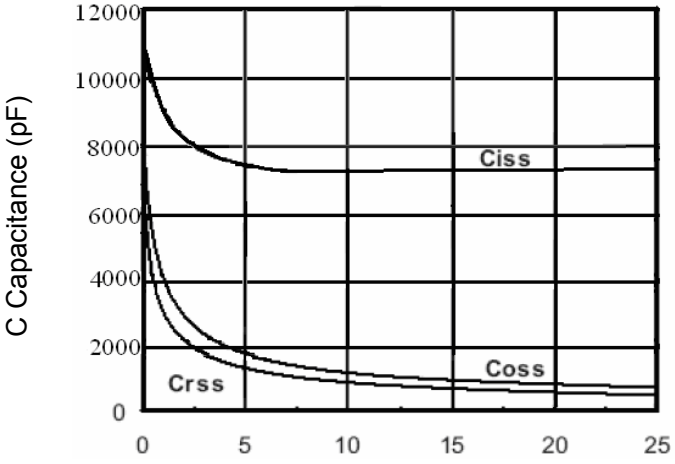


Figure 7 Capacitance vs Vds

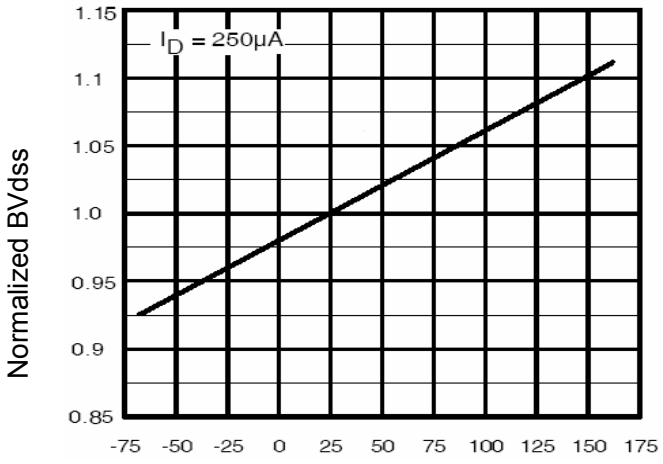


Figure 10 BV_{DSS} vs Junction Temperature

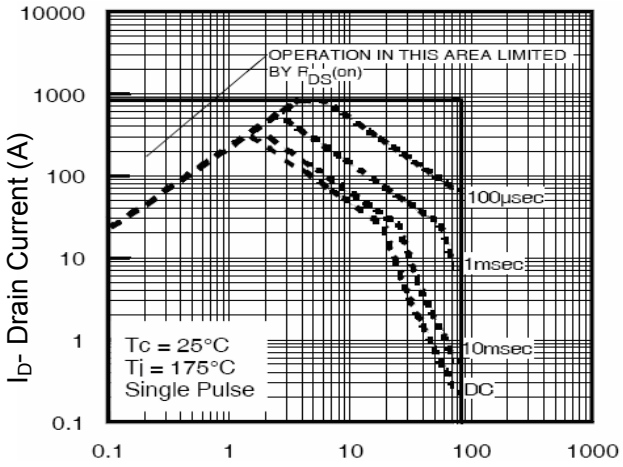


Figure 8 Safe Operation Area

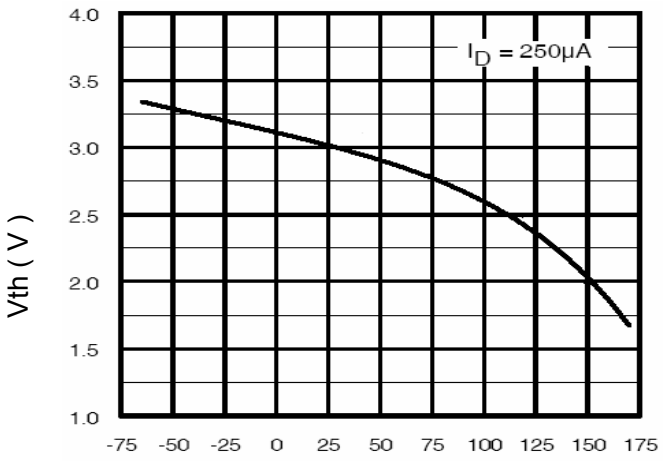


Figure 11 $V_{GS(th)}$ vs Junction Temperature

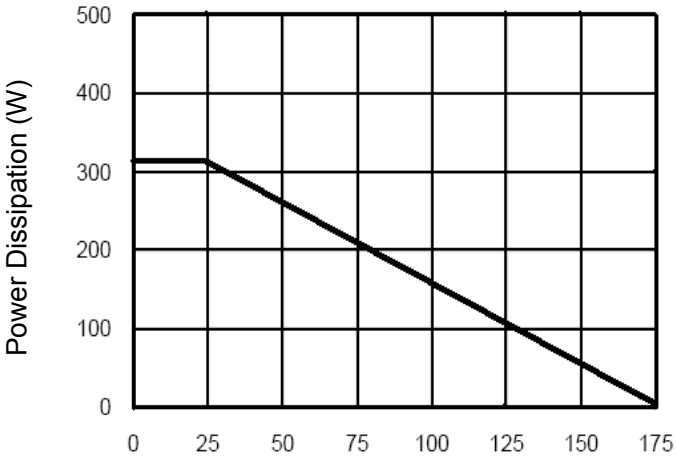


Figure 9 Power De-rating

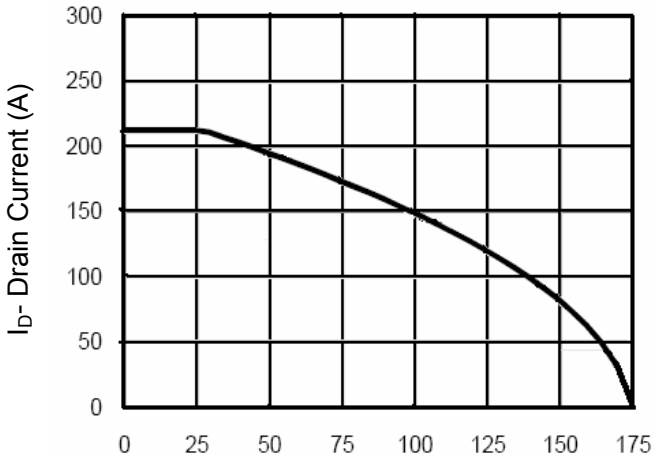


Figure 12 Current De-rating

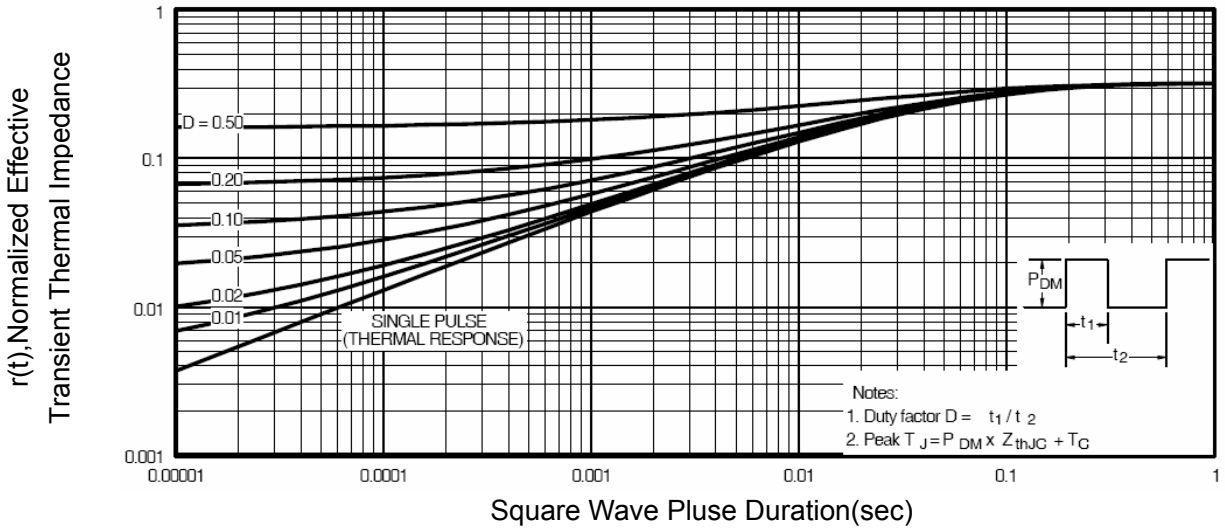
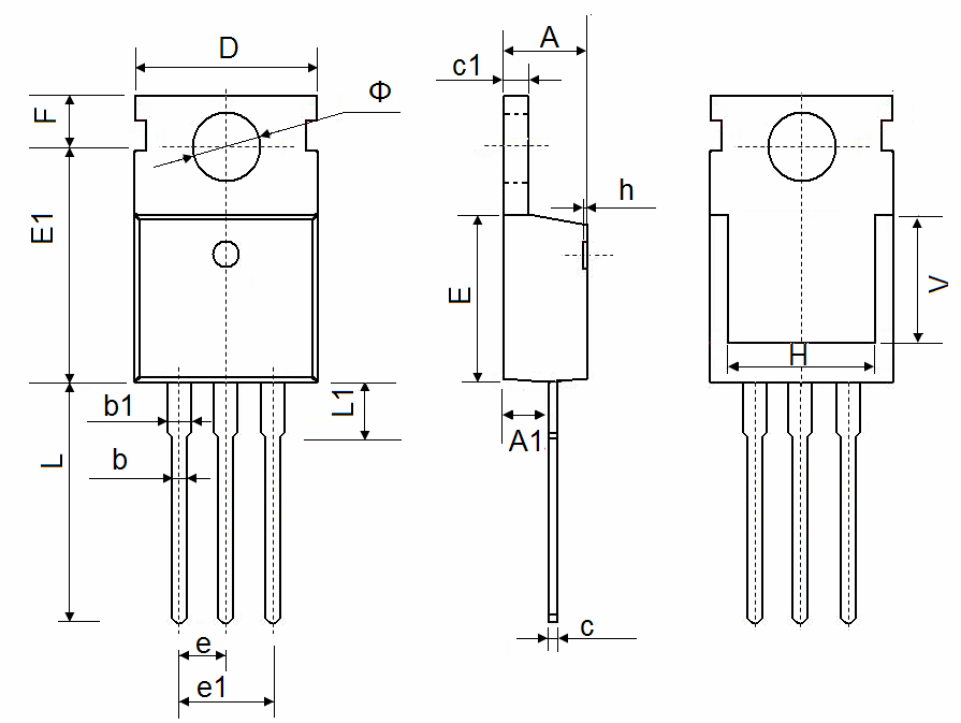


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

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