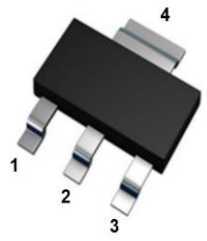
LN03N100TZHG

N-Channel Logic Level Enhancement Mode Field MOSFET

1. FEATURES

- We declare that the material of product compliance with RoHS requirements and Halogen Free.



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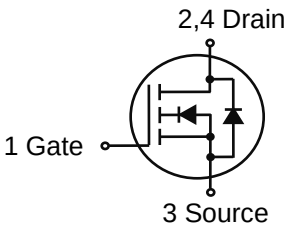
2. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LN03N100TZHG	TH	1000/Tape&Reel

3. MAXIMUM RATINGS(Ta = 25ºC)

Parameter		Symbol	Limits	Unit
Drain–Source Voltage		VDSS	100	V
Gate–to–Source Voltage – Continuous		VGS	±20	V
Continuous Drain Current(Note 1)	Ta=25℃	ID	4	A
Pulsed Drain Current(Note 2)		IDM	16	
Power Dissipation(Note 1)	Ta=25℃	PD	1.9	W
Junction Temperature		Tj	-55~+150	℃
Storage Temperature Range		Tstg	-55~+150	℃



4. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Thermal Resistance,Junction–to–Ambient(Note 1)	RΘJA	65	℃/W
Thermal Resistance,Junction-to-Case (Note 3)	RθJA	150	℃/W
Thermal Resistance,Junction-to-Case (Note 3)	RθJC	15	℃/W

1.Surface−mounted on FR4 board using 1 sq−in pad, 2 oz Cu.

2.Pulse width limited by maximum junction temperature

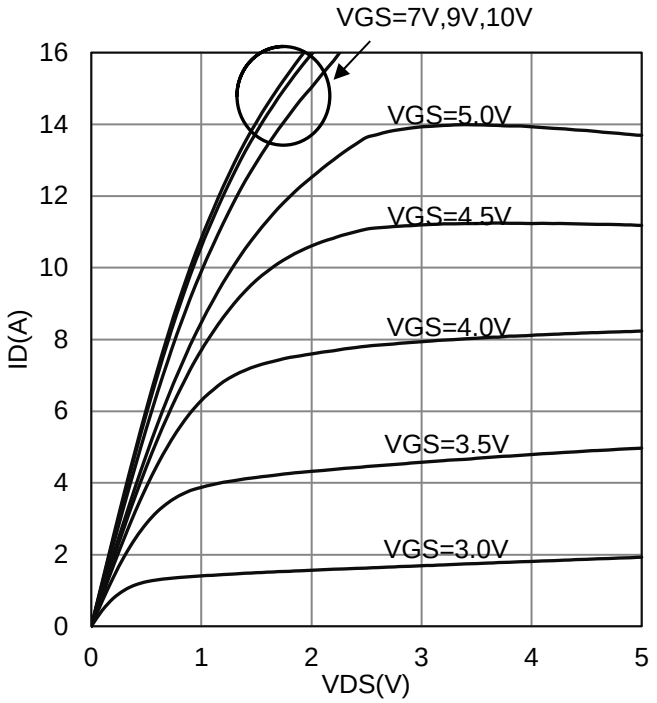
3.Surface−mounted on FR4 board using the minimum recommended pad size.

5. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

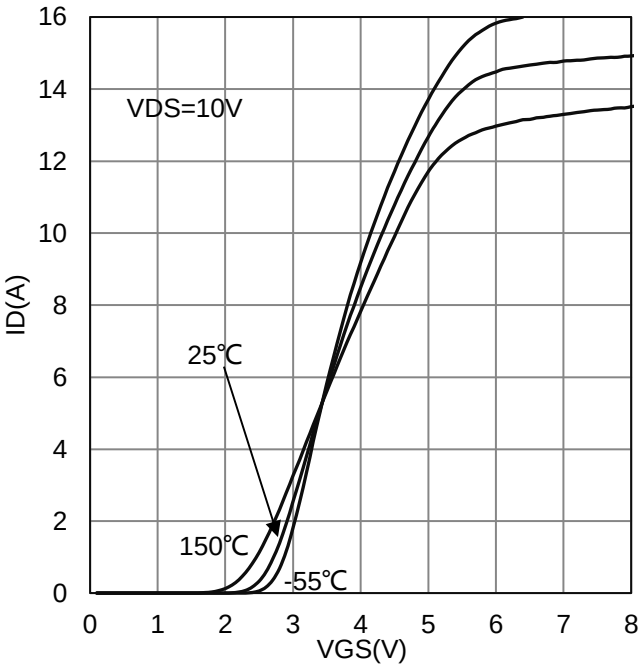
Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain to Source Breakdown Voltage (VGS =0V, ID =250μA)		VDSS	100	-	-	V
Zero Gate Voltage Source Current (VDS =80V, VGS =0V)		IDSS	-	-	1	uA
Gate to Source Leakage Current (VDS =0V, VGS = ±20V)		IGSS	-	-	±100	nA
Gate Threshold Voltage (VDS = VGS , ID = 250μA)		VGS(th)	1	1.8	3	V
Drain-to-Source On-Resistance(Note 4) (VGS=10V, ID=8A) (VGS=4.5V, ID=5A)		RDS(ON)	- -	80 105	100 150	mΩ
Diode Forward Voltage(Note 4) (IF = 1 A, VGS = 0 V)		VSD	-	-	1.3	V
Dynamic						
Input Capacitance	(VGS = 0V ,VDS = 50V, f = 1MHz)	Ciss	-	202	-	pF
Output Capacitance		Coss	-	36	-	
Reverse Transfer Capacitance		Crss	-	2.5	-	
Turn-on Delay Time	(VDD=50V,VGS =10V,RG = 6.8 Ω,ID= 14 A)	td(on)	-	4.6	-	nS
Rise Time		tr	-	4.3	-	
Turn-Off Delay Time		td(off)	-	12.9	-	
Fall Time		tf	-	1.7	-	
Total Gate Charge	(VDS=50V,VGS =10V,ID=8A)	Qg	-	6.4	-	nC
Gate to Source Charge		Qgs	-	0.6	-	
Gate to Drain Charge		Qgd	-	2.4	-	
Gate Resistance		Rg	-	TBD	-	Ω

4.Pulse test : Pulse Width ≤300 μs, Duty Cycle≤2%.

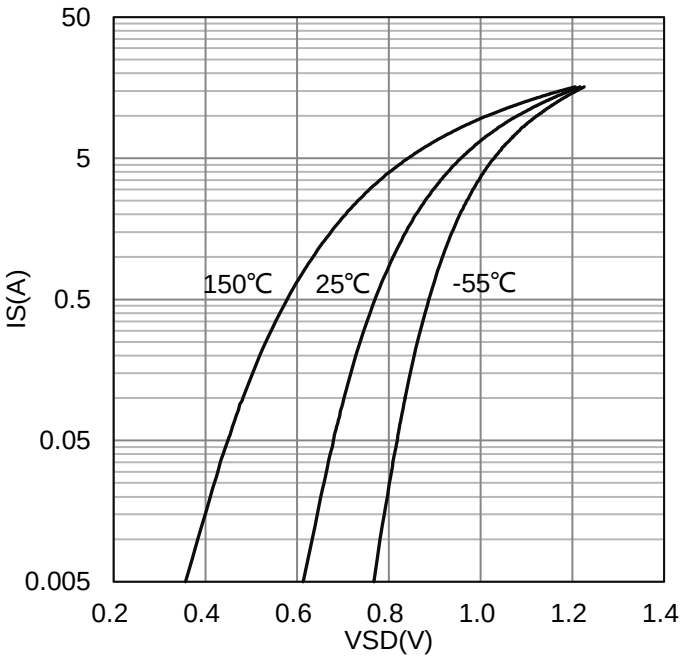
6. ELECTRICAL CHARACTERISTICS CURVES



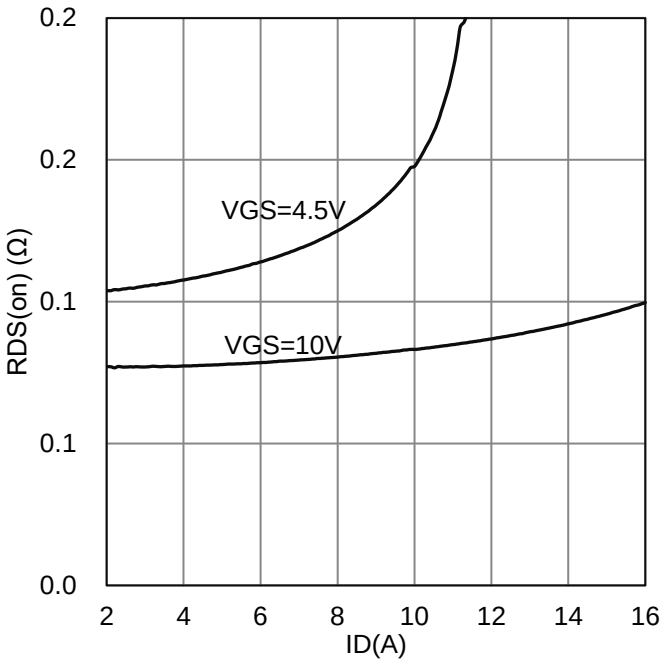
ID vs. VDS



ID vs. VGS

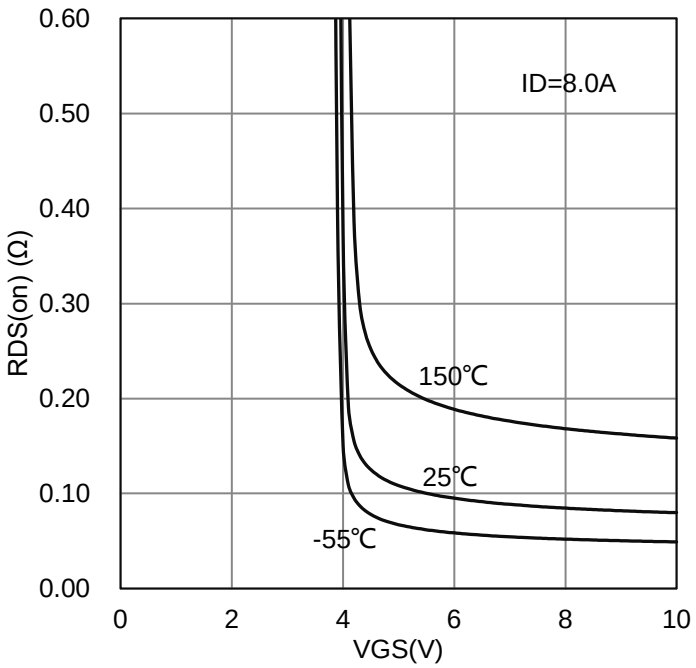


IS vs. VSD

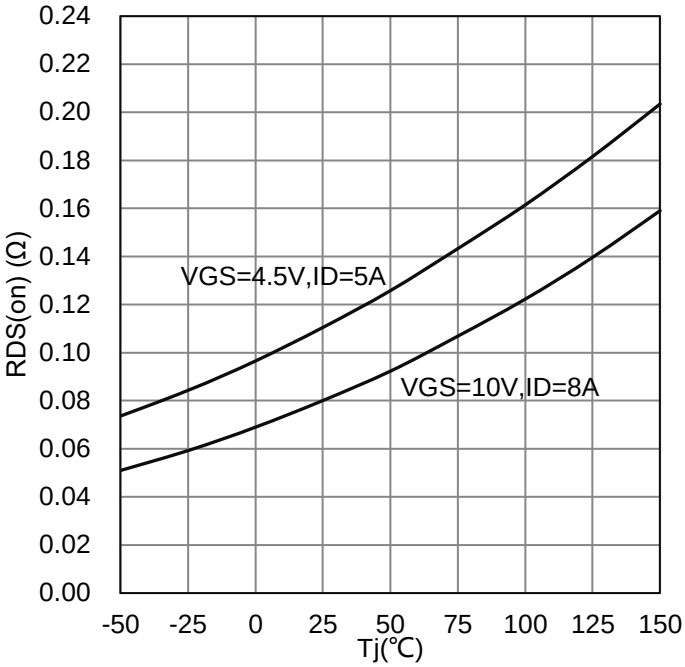


RDS(on) vs. ID

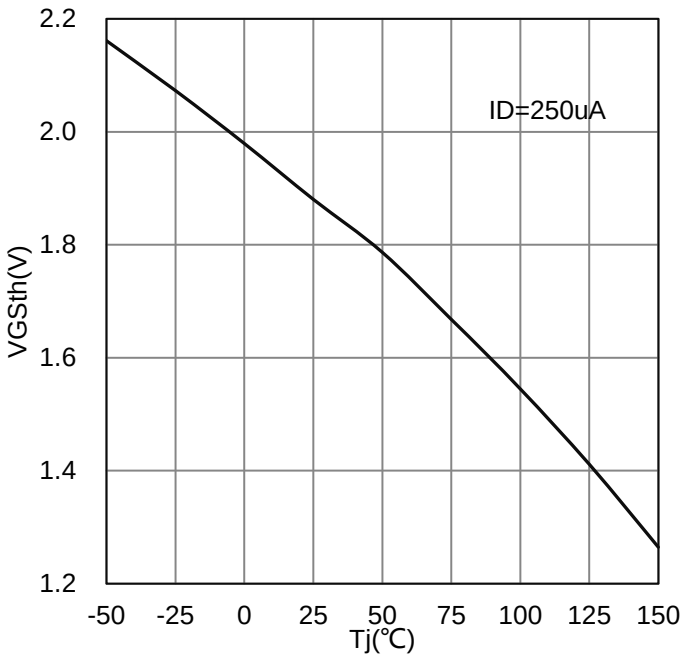
6. ELECTRICAL CHARACTERISTICS CURVES(Con.)



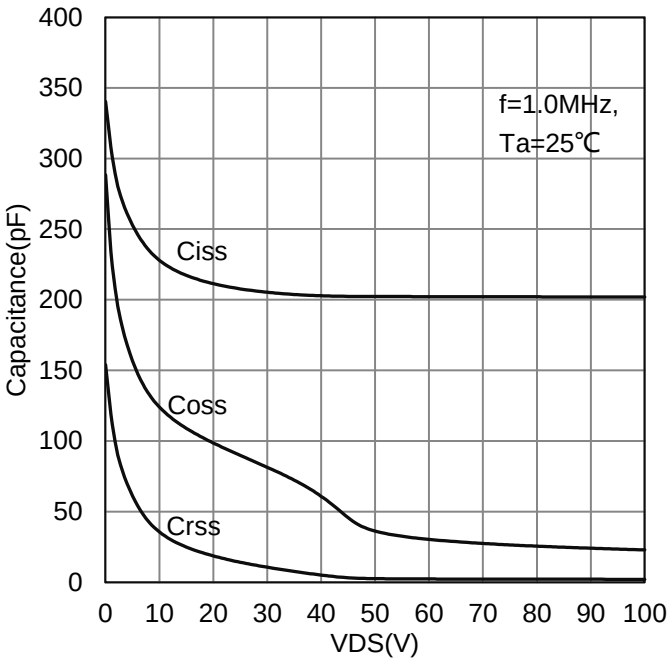
RDS(on) vs. VGS



RDS(on) vs. Tj

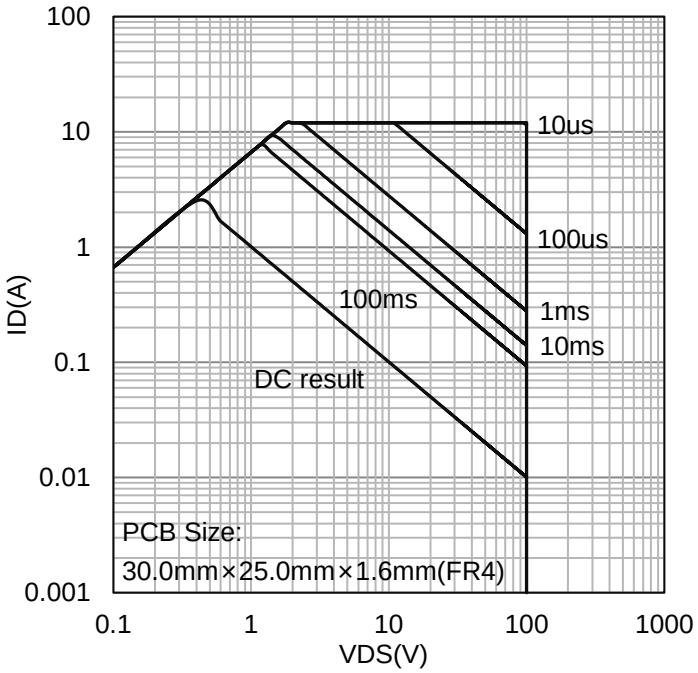


VGSth vs. Tj

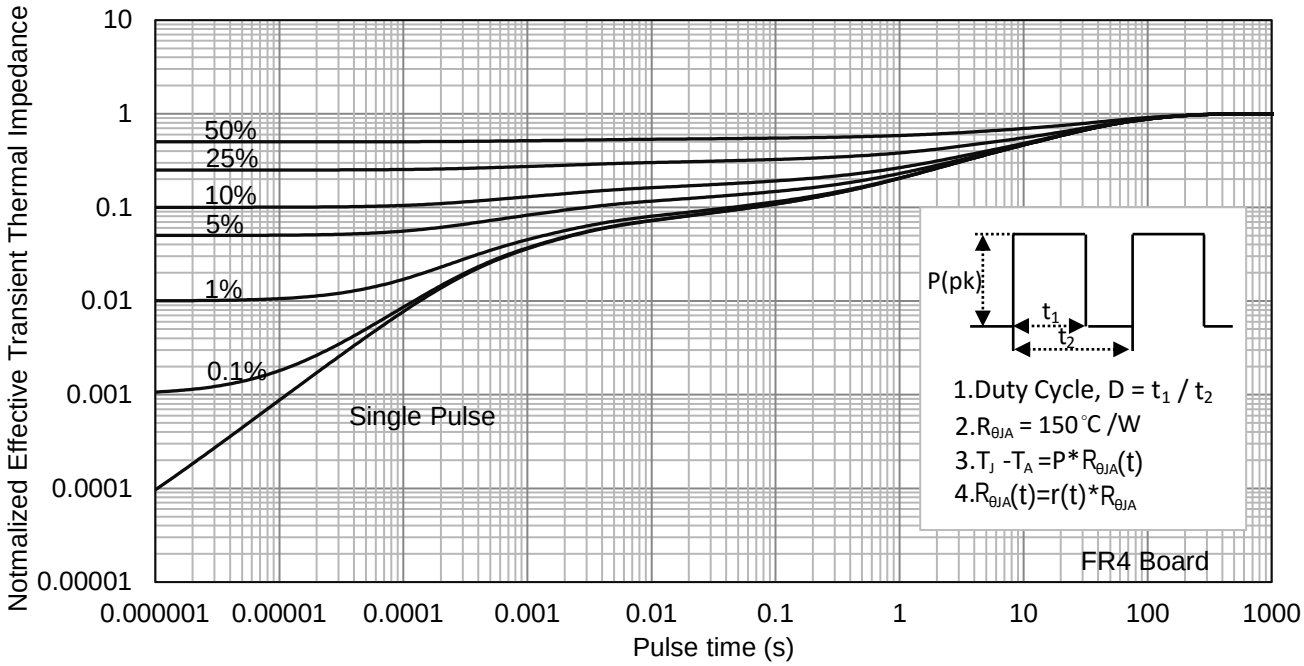


Capacitance

6. ELECTRICAL CHARACTERISTICS CURVES(Con.)



Safe Operating Area



Thermal Response

7.OUTLINE AND DIMENSIONS

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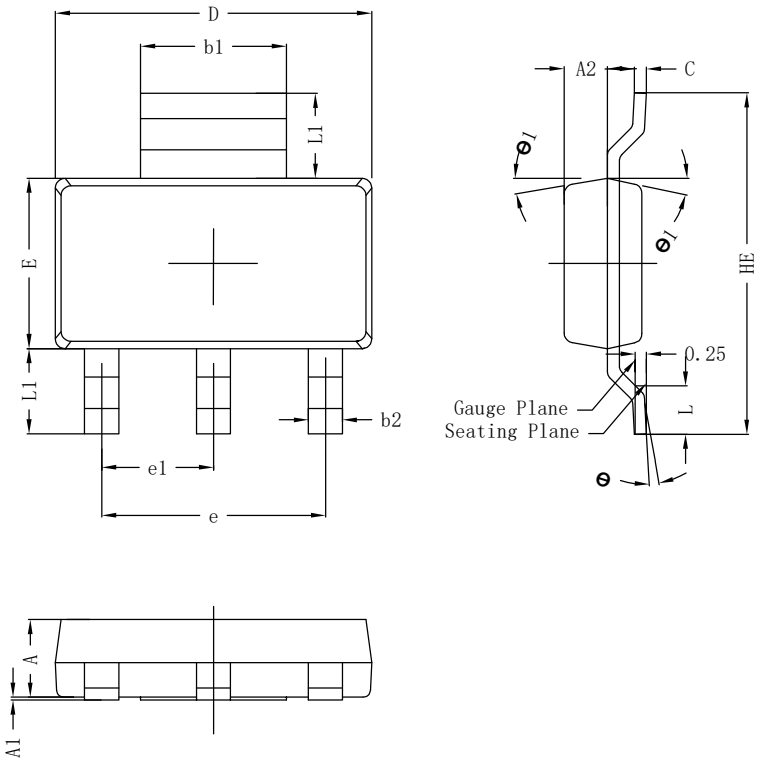

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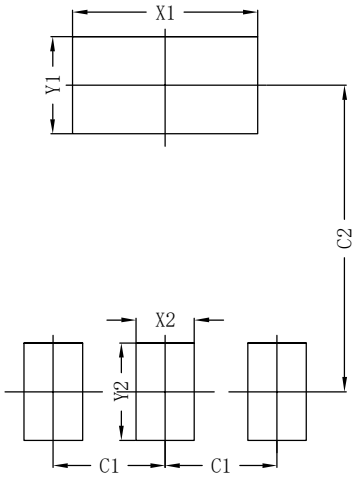
DIM	MIN	NOR	MAX
A	1.50	1.60	1.70
A1	0.00	0.05	0.10
A2	0.80	0.90	1.00
b1	2.90	3.02	3.10
b2	0.60	0.72	0.80
c	0.20	0.27	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	4.60BSC		
e1	2.30BSC		
HE	6.80	7.00	7.20
L	0.80	1.00	1.20
L1	1.75(REF)		
θ	0°~8°		
θ 1	8°	10°	12°
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.10mm per side.

8.SOLDERING FOOTPRINT



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DIM	(mm)
X1	3.80
Y1	2.00
X2	1.20
Y2	2.00
C1	2.30
C2	6.30

DISCLAIMER

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