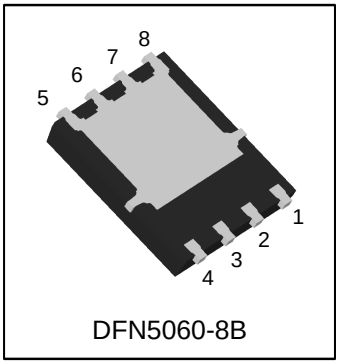
LN7616DT1WG

N-Channel Enhancement Mode MOSFET



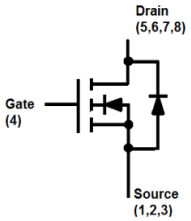
DFN5060-8B

1. FEATURES

- Advanced trench cell design
- Low Thermal Resistance
- We declare that the material of product compliance with RoHS requirements and Halogen Free.

2. APPLICATIONS

- Motor drivers
- DC-DC Converter



3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
LN7616DT1WG	LN7616	3000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
Drain-to-Source Voltage	VDS	100	V
Gate-to-Source Voltage	VGS	±20	V
Continuous Drain Current(TC = 25 ℃, VGS =10 V)	ID	59	A
Pulsed Drain Current(TC = 25 ℃, VGS = 10 V)	IDM	236	A
Single Pulse Avalanche Energy L=0.1mH	EAS	13	mJ
Power Dissipation(TC = 25 ℃)	PD	35	W
Operating Junction and Storage Temperature Range	Tj/Tstg	-55~+150	℃
Diode Forward Current	IS	55	A

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-to-Ambient	RθJA	62.5	℃/W
Thermal Resistance Junction-to-Case	RθJC	3.5	

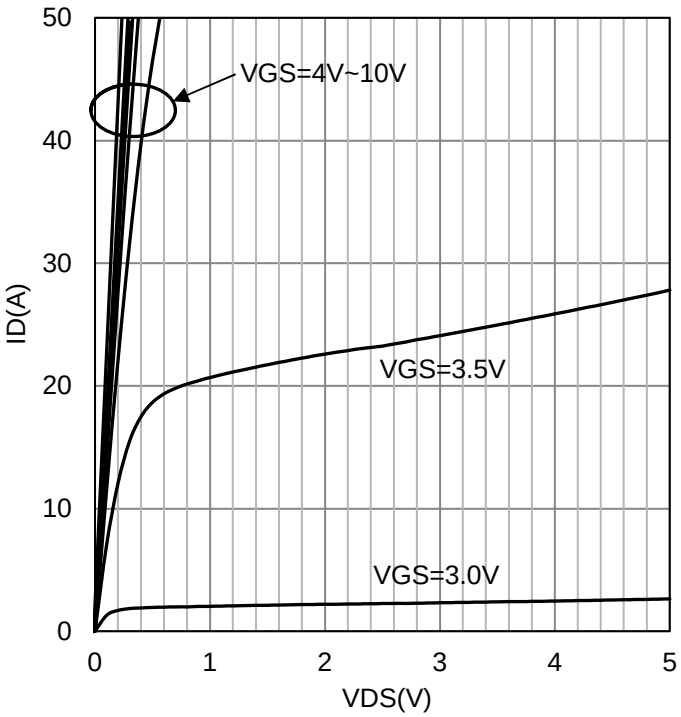
1. Surface Mounted on 1 in^2 pad area, t ≤ 10 sec

6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

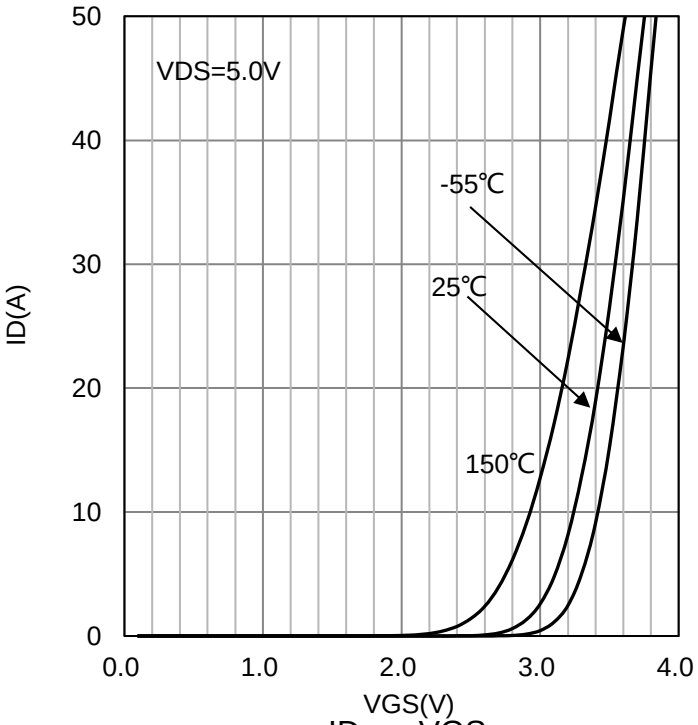
Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain to Source Breakdown Voltage (VGS =0V, ID =250μA)		VDSS	100	-	-	V
Zero Gate Voltage Source Current (VDS =80V, VGS =0V) (VDS =80V, VGS =0V, TJ = 85 ℃)		IDSS	- -	- -	1 30	uA
Gate-Body current (VDS =0V, VGS = ±20V)		IGSS	-	-	±100	nA
Gate Threshold Voltage (VDS = VGS , ID = 250μA)		VGS(th)	1.5	-	2.5	V
Drain-to-Source On-Resistance (VGS = 10 V, ID = 20 A) (VGS = 6 V, ID = 10 A) (VGS = 4.5 V, ID = 10 A)		RDS(ON)	- - -	4.5 5.3 6	5.2 8 9	mΩ
Diode Forward Voltage (ISD = 20 A, VGS = 0 V)		VSD	-	0.8	1.2	V
Dynamic						
Input Capacitance	(VGS = 0V ,VDS = 50V, f = 1MHz)	Ciss	-	3353	-	pF
Output Capacitance		Coss	-	520	-	
Reverse Transfer Capacitance		Crss	-	5.2	-	
Turn-on Delay Time	(VDS=50 V, VGEN=10V,RG = 6 Ω ID=13A)	td(on)	-	19	-	nS
Rise Time		tr	-	4.7	-	
Turn-Off Delay Time		td(off)	-	59.5	-	
Fall Time		tf	-	21	-	
Total Gate Charge (VDD=50V,VGS=10V,ID=13A)		Qg	-	55.7	72	nC
Total Gate Charge (VDD=50V,VGS=5V,ID=13A)		Qg	-	32	-	
Gate to Source Charge (VDD=40V,VGS=5V,ID=68A)		Qgs	-	11.8	-	
Gate to Drain Charge (VDD=40V,VGS=5V,ID=68A)		Qgd	-	14.4	-	
Gate Resistance (VDS=0V,VGS=0V,f=1.0MHz)		Rg	-	1	3	Ω
Reverse Recovery Time (VR=30V,IF=20 A, dI/dt = 100 A/us)		trr	-	65	-	ns
Reverse Recovery Charge (VR=30V,IF=20 A, dI/dt = 100 A/us)		Qrr	-	105	-	nC

2.Pulse test ; pulse width ≤ 300μs, duty cycle ≤ 2 %

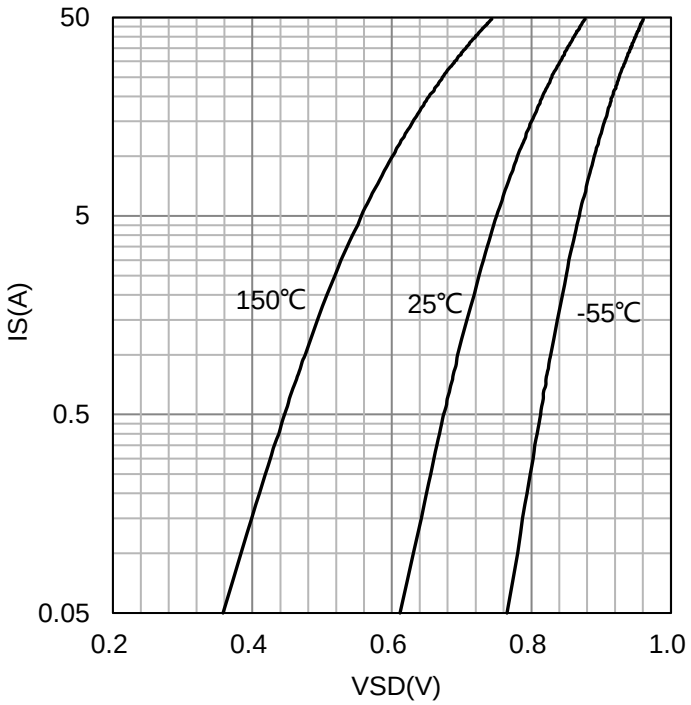
7.ELECTRICAL CHARACTERISTICS CURVES



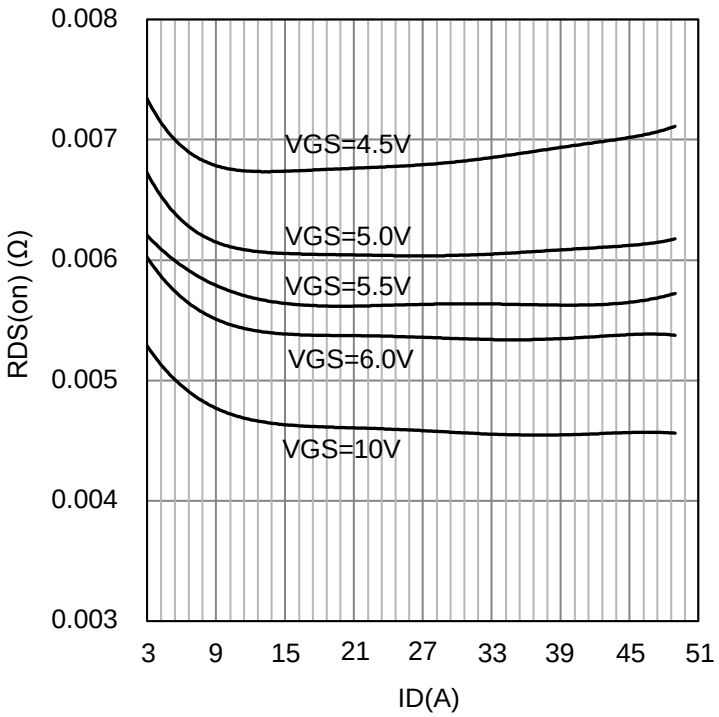
ID vs. VDS



ID vs. VGS

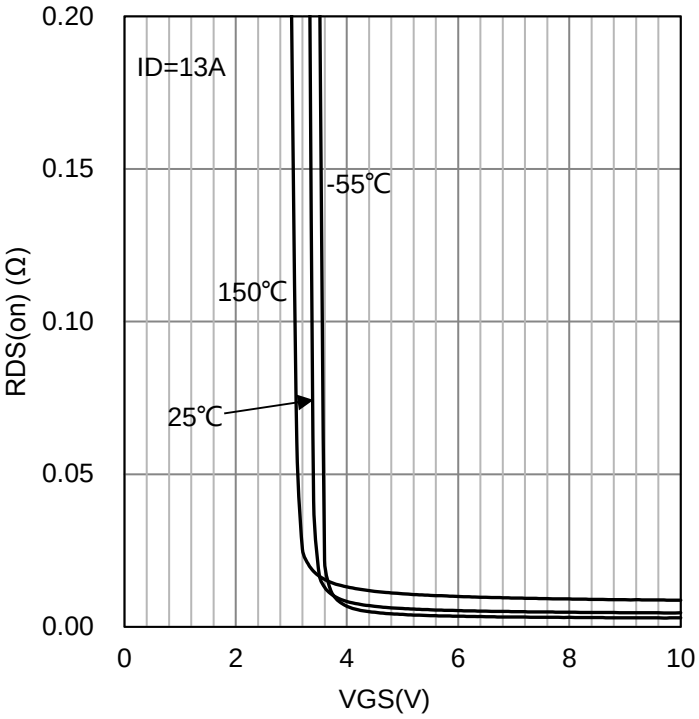


IS vs. VSD

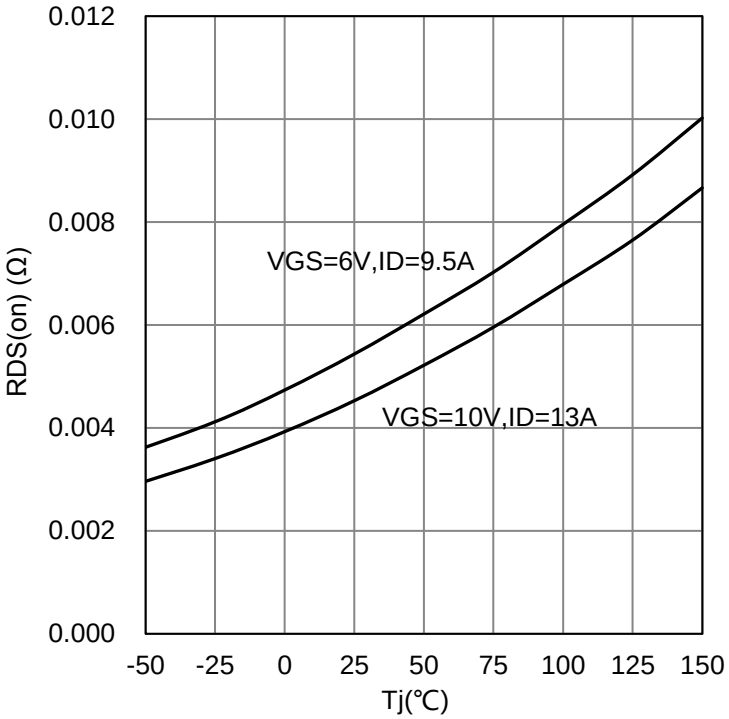


RDS(on) vs. ID

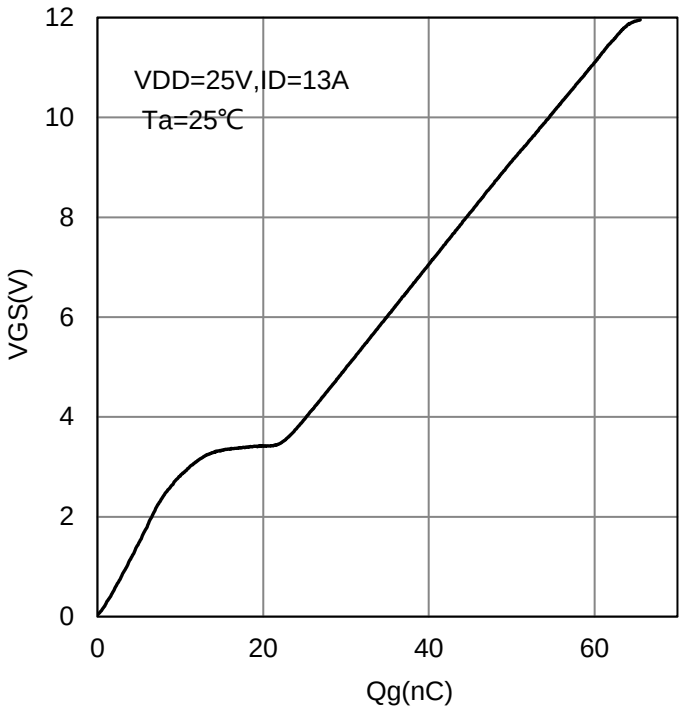
7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



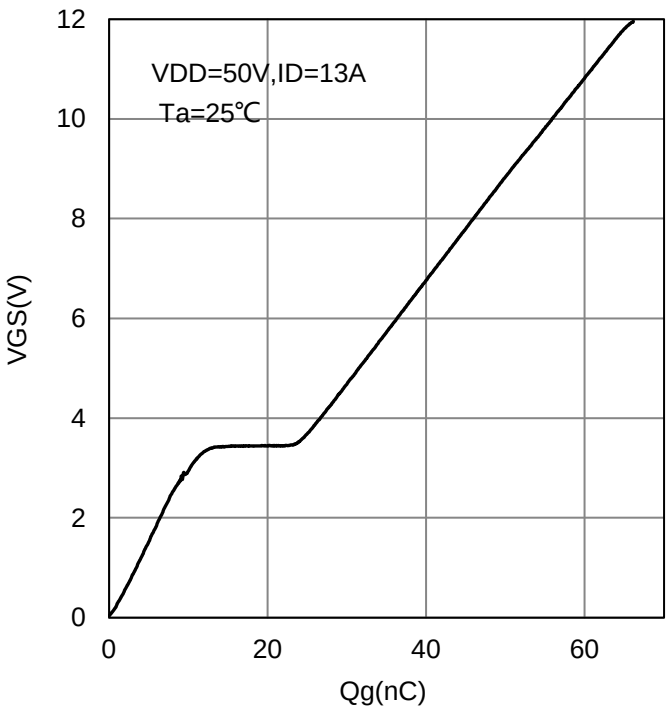
RDS(on) vs. VGS



RDS(on) vs. Tj

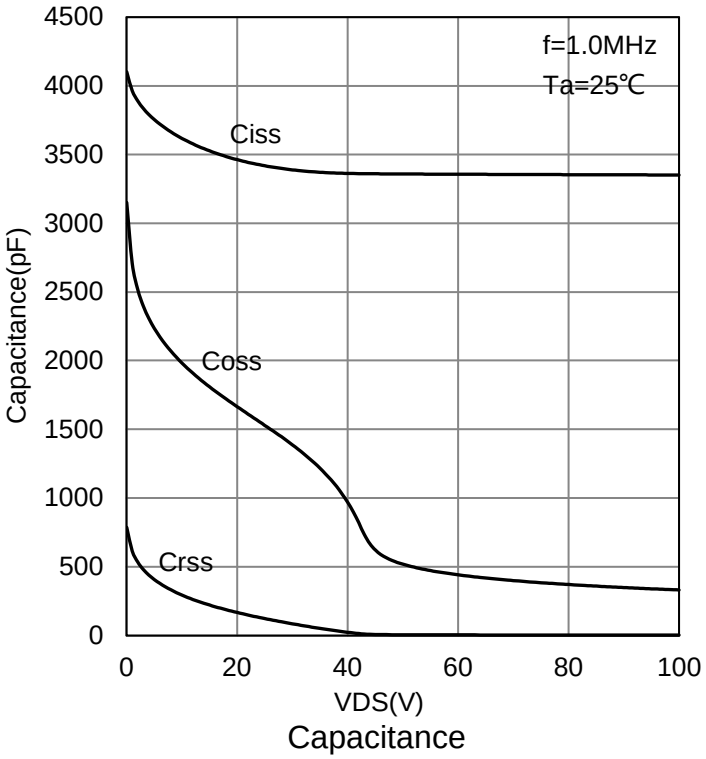


VGS vs. Qg（VDD=25V,ID=13A)

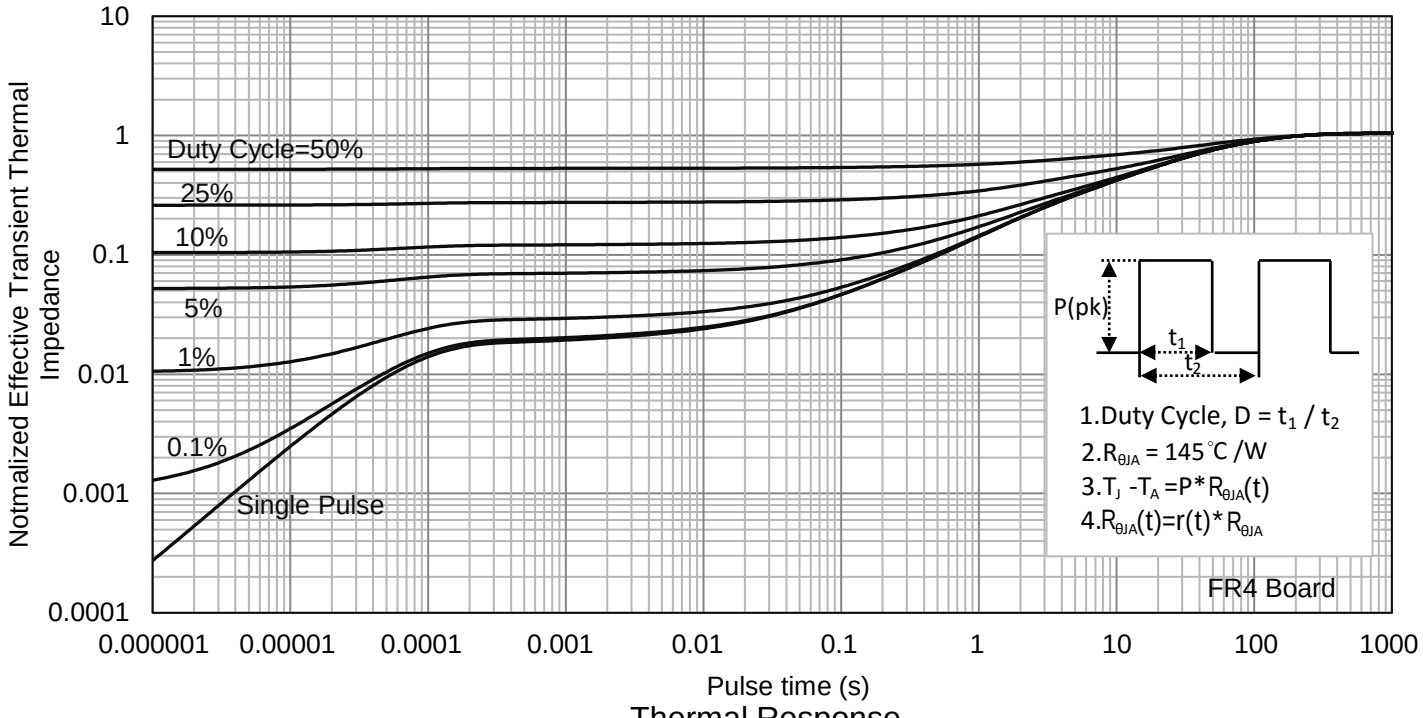


VGS vs. Qg（VDD=50V,ID=13A)

7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



Capacitance



Thermal Response

8.OUTLINE AND DIMENSIONS

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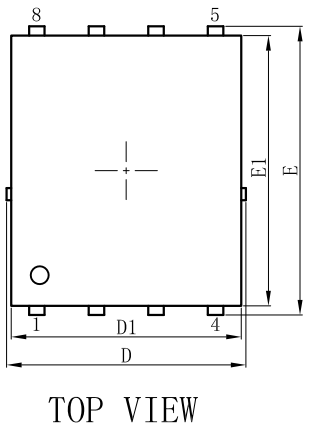
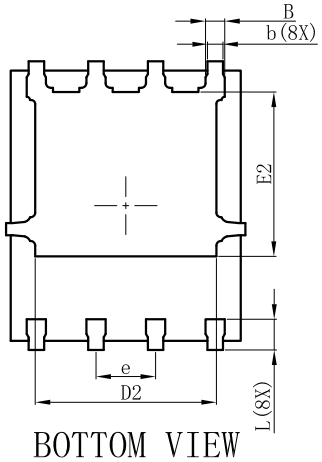
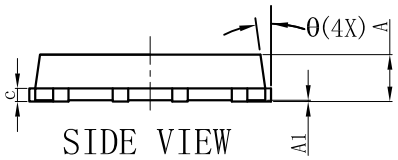


TOP VIEW



BOTTOM VIEW

DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0°	-	12°
All Dimensions in mm			

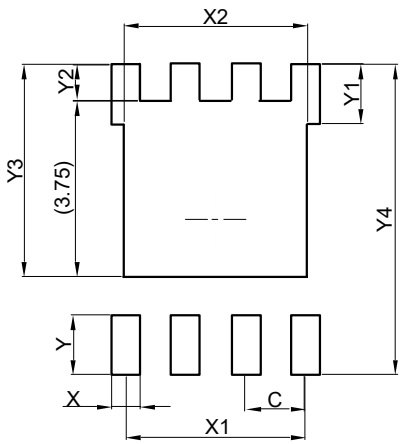


SIDE VIEW

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61

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