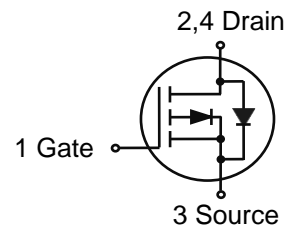
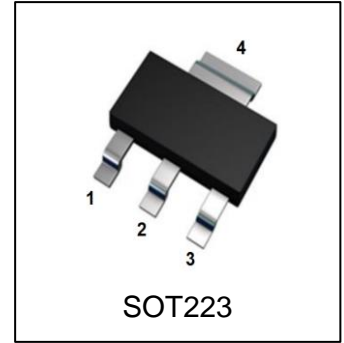


LP20N100TZHG

P-Channel 100-V Power MOSFET



1. FEATURES

- $R_{DS(ON)} \leq 1.2\Omega$, $V_{GS@-10V}$
- $R_{DS(ON)} \leq 1.3\Omega$, $V_{GS@-4.5V}$
- Logic-Level Gate Drive
- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- We declare that the material of product compliance with RoHS requirements and Halogen Free.

2. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP20N100TZHG	2P	1000/Tape&Reel

3. MAXIMUM RATINGS($T_a = 25^\circ\text{C}$)

Parameter		Symbol	Limits	Unit
Drain–Source Voltage		VDSS	-100	V
Gate–to–Source Voltage – Continuous		VGS	± 20	V
Continuous Drain Current(Note 1)	$T_a=25^\circ\text{C}$	ID	1.2	A
Pulsed Drain Current(Note 2)		IDM	4.8	
Power Dissipation(Note 1)	$T_a=25^\circ\text{C}$	PD	1.9	W
Junction Temperature		Tj	-55~+150	$^\circ\text{C}$
Storage Temperature Range		Tstg	-55~+150	$^\circ\text{C}$

4. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Thermal Resistance,Junction–to–Ambient(Note 1)	$R_{\theta JA}$	65	$^\circ\text{C}/\text{W}$
Thermal Resistance,Junction-to-Case (Note 3)	$R_{\theta JA}$	150	$^\circ\text{C}/\text{W}$
Thermal Resistance,Junction-to-Case (Note 3)	$R_{\theta JC}$	15	$^\circ\text{C}/\text{W}$

1.Surface–mounted on FR4 board using 1 sq–in pad, 2 oz Cu.

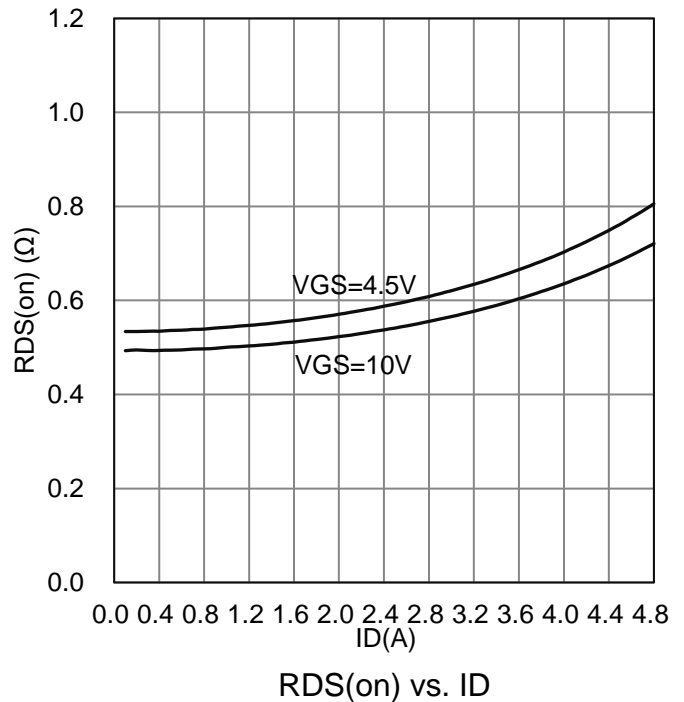
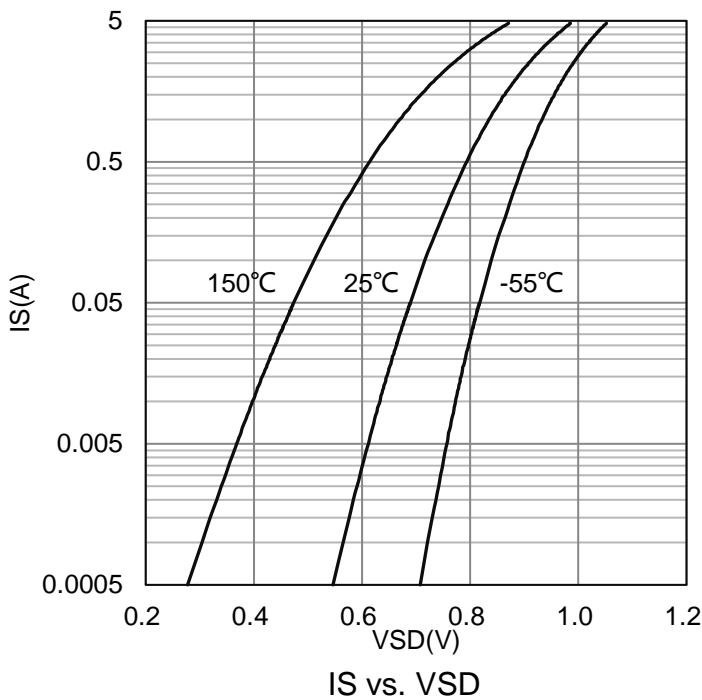
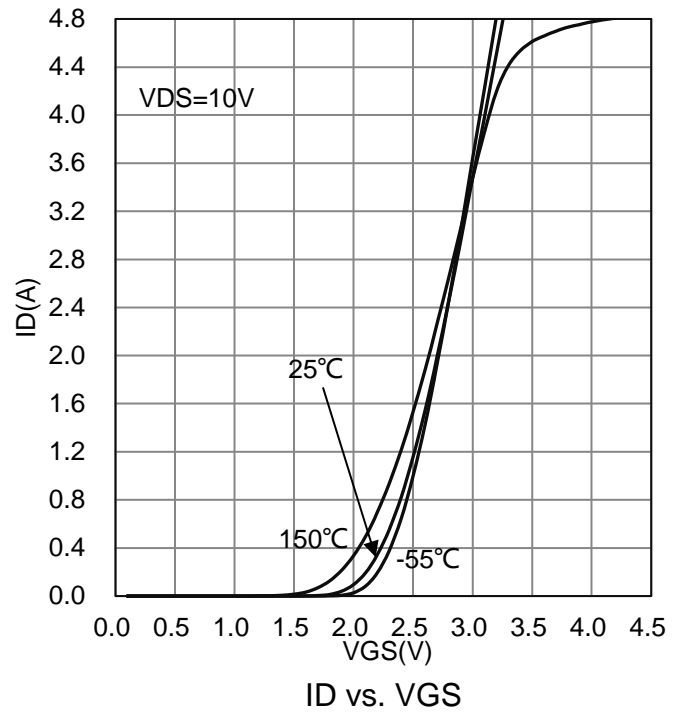
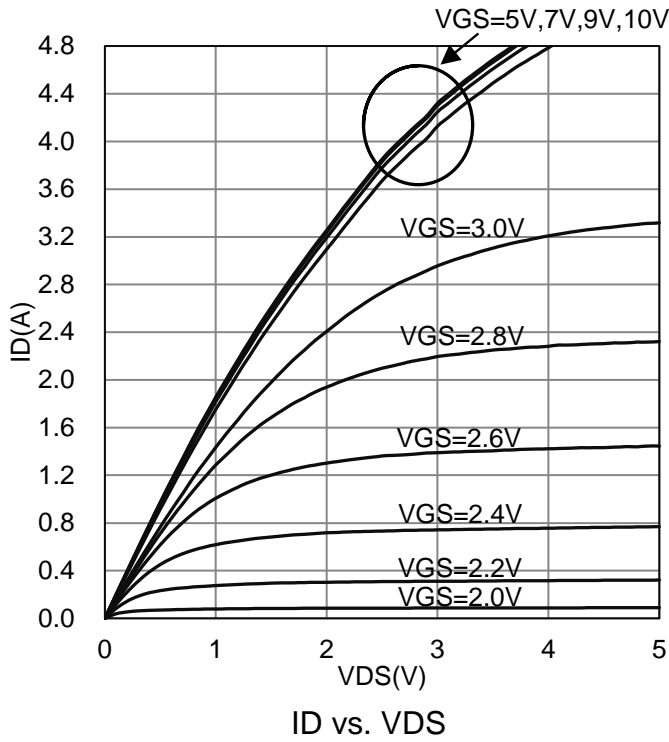
2.Pulse width limited by maximum junction temperature

3.Surface–mounted on FR4 board using the minimum recommended pad size.

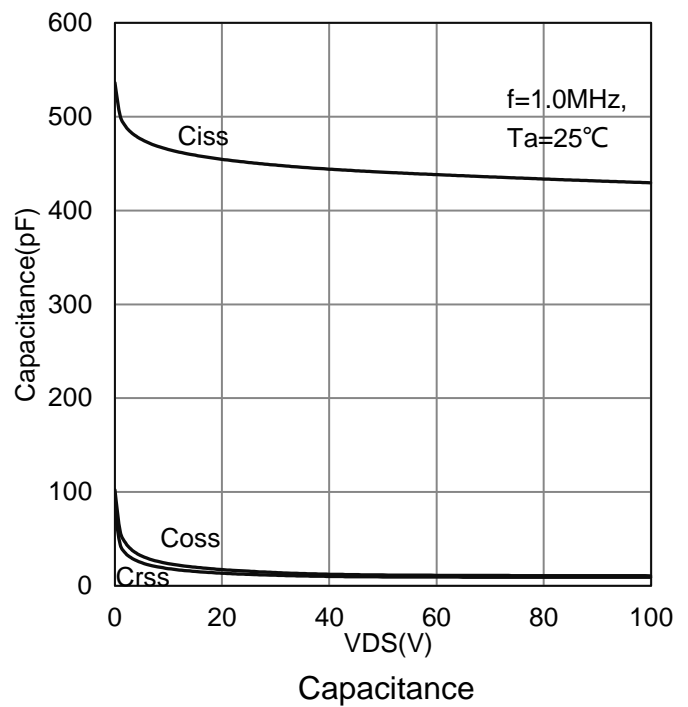
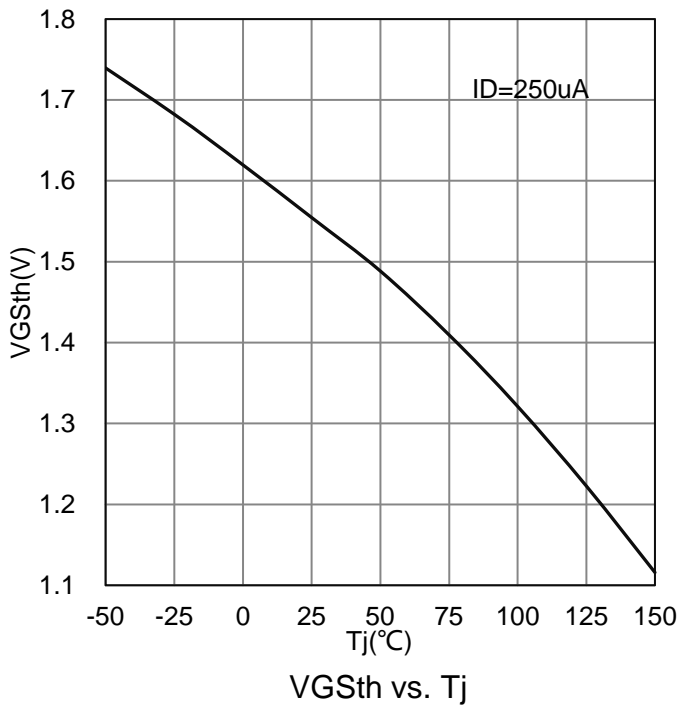
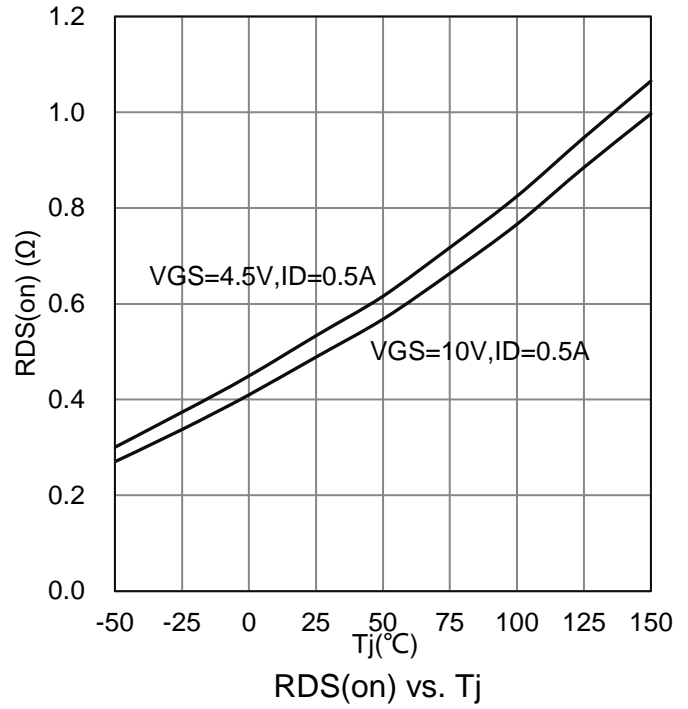
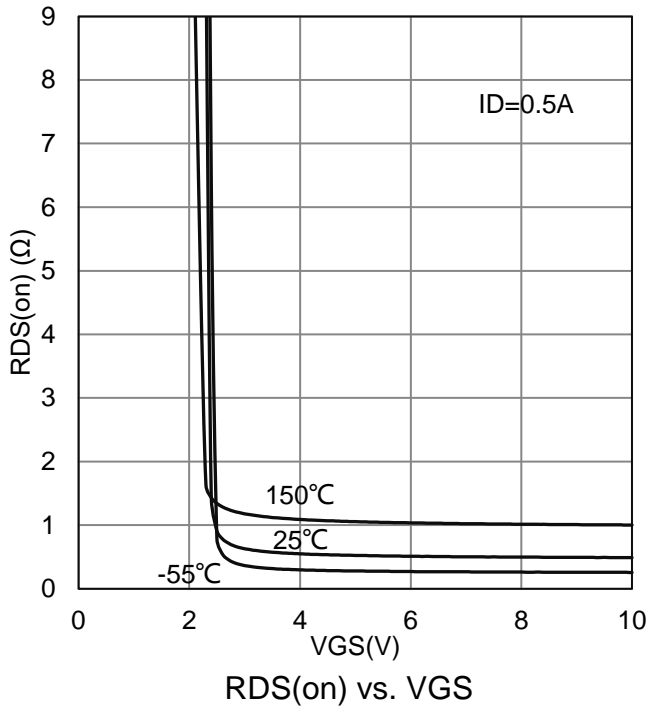
5. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
STATIC					
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)	VBRDSS	-100	-	-	V
Gate Threshold Voltage (VDS = VGS, ID = -250μA)	VGS(th)	-1	-	-3	V
Gate Leakage Current (VDS = 0V, VGS = ±20V)	IGSS	-	-	±100	nA
Zero Gate Voltage Drain Current (VGS = 0V, VDS = -80 V) (VGS = 0V, VDS = -80 V, TJ = 55°C)	IDSS	-	-	-1 -25	μA
Static Drain–Source On–State Resistance (VGS = -10 V, ID = -0.5 A) (VGS = -4.5 V, ID = -0.5 A)	RDS(on)	-	-	1.2 1.3	Ω
DYNAMIC					
Total Gate Charge (VGS = -4.5 V, ID = -1A, VDS = -50 V)	Qg	-	3.6	-	nC
Gate–Source Charge (VGS = -4.5 V, ID = -1A, VDS = -50 V)	Qgs	-	1.1	-	
Gate–Drain Charge (VGS = -4.5 V, ID = -1A, VDS = -50 V)	Qgd	-	1.7	-	
Input Capacitance (VGS = 0 V, f = 1.0MHz, VDS = -15 V)	Ciss	-	459	-	pF
Output Capacitance (VGS = 0 V, f = 1.0MHz, VDS = -15 V)	Coss	-	20	-	
Reverse Transfer Capacitance (VGS = 0 V, f = 1.0MHz, VDS = -15 V)	Crss	-	15.2	-	
Turn-On Delay Time	(VDD = -50V, RL = 50Ω ID = -1A, VGEN = -10V RG = 6.2Ω)	td(on)	-	4.1	ns
Rise Time		tr	-	12.4	
Turn-Off Delay Time		td(off)	-	22.6	
Fall Time		tf	-	19.7	
Gate Resistance (VDS = 0V, VGS = 0V, f = 1.0MHz)	Rg	-	6.5	-	Ω

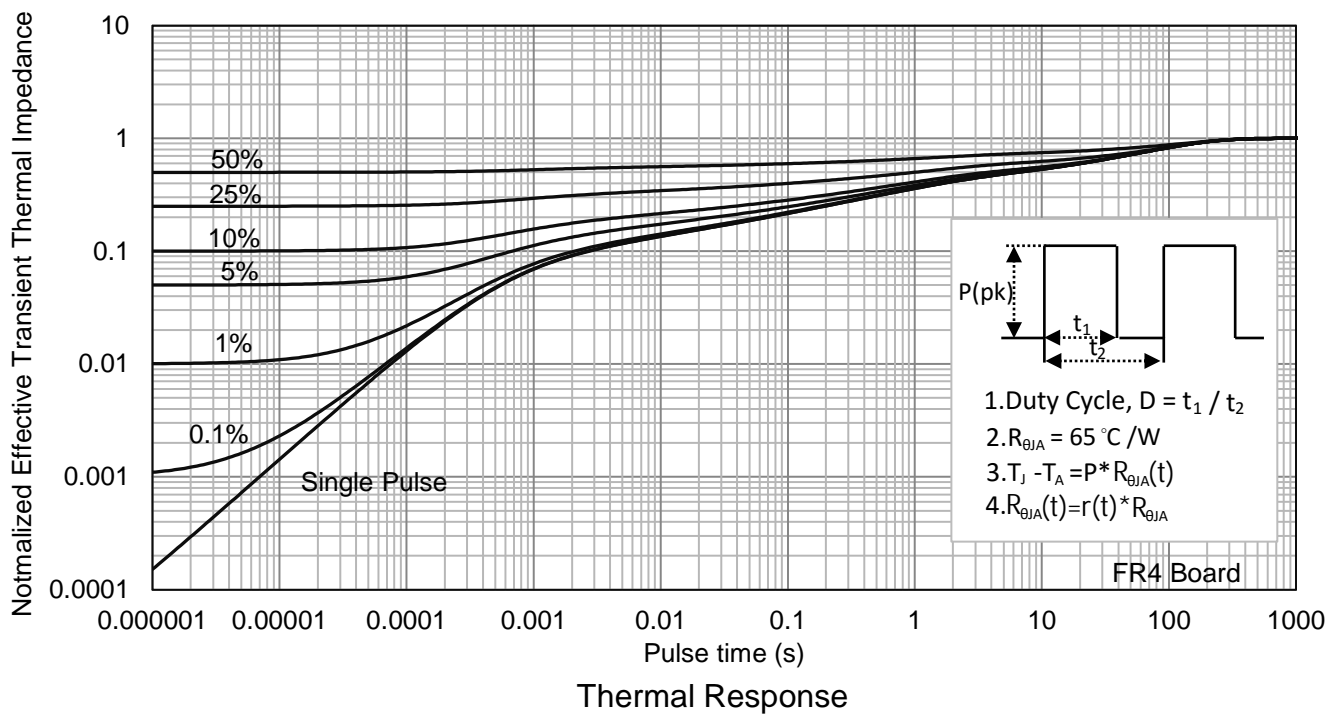
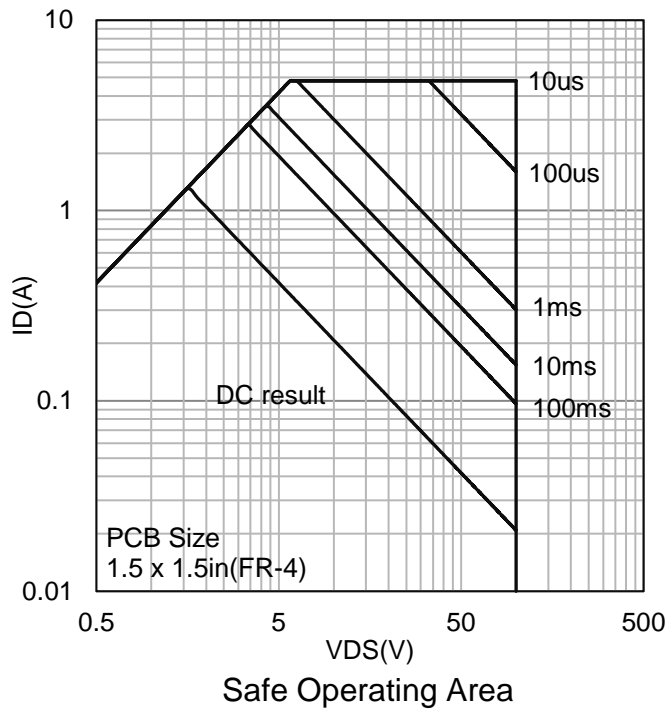
6. ELECTRICAL CHARACTERISTICS CURVES



6. ELECTRICAL CHARACTERISTICS CURVES(Con.)

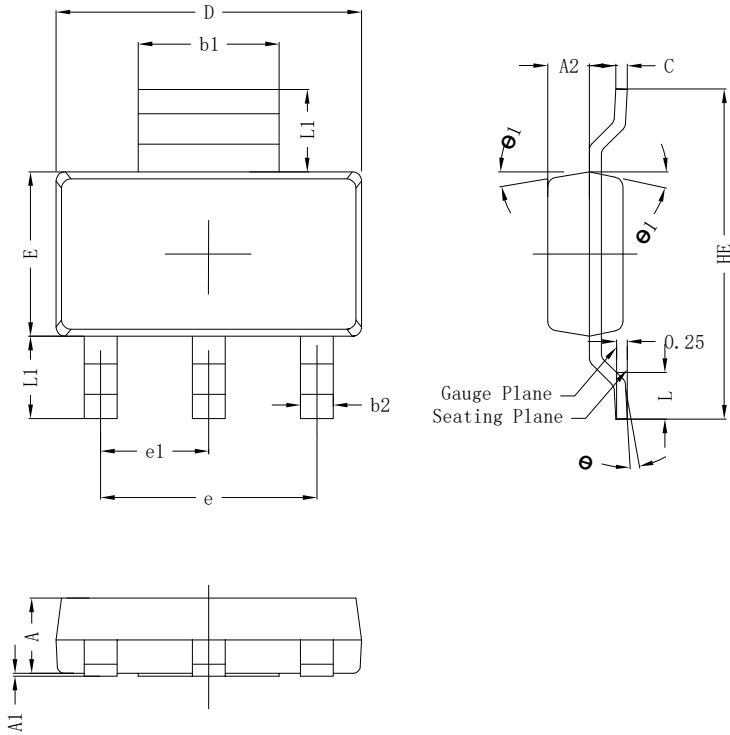


6. ELECTRICAL CHARACTERISTICS CURVES(Con.)



7. OUTLINE AND DIMENSIONS

SOT223

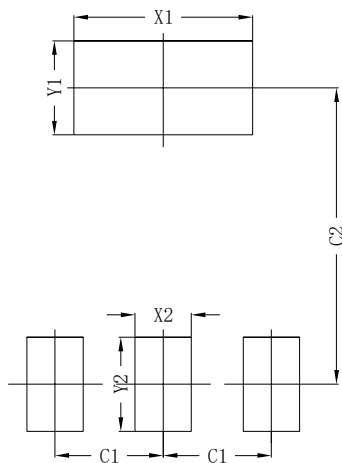


SOT223			
DIM	MIN	NOR	MAX
A	1.50	1.60	1.70
A1	0.00	0.05	0.10
A2	0.80	0.90	1.00
b1	2.90	3.02	3.10
b2	0.60	0.72	0.80
c	0.20	0.27	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	4.60BSC		
e1	2.30BSC		
HE	6.80	7.00	7.20
L	0.80	1.00	1.20
L1	1.75(REF)		
θ	0°~8°		
θ 1	8°	10°	12°
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish $Ra0.4 \pm 0.2\mu m$
2. Bottom package surface finish $Ra0.7 \pm 0.2\mu m$
3. Side package surface finish $Ra0.4 \pm 0.2\mu m$
4. Protrusion or Gate Burrs shall not exceed 0.10mm per side.

8. SOLDERING FOOTPRINT



SOT223	
DIM	(mm)
X1	3.80
Y1	2.00
X2	1.20
Y2	2.00
C1	2.30
C2	6.30

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