NM5A02G01A Datasheet

2Gbit 3.3V x1, x2, x4
Serial Peripheral Interface
NAND Flash Memory

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1. Features

- **2Gbit SLC Technology SPI NAND Flash**
  - Page size: 2048 bytes + 128 bytes = 2176 bytes
  - Block size: 64 pages = 128K bytes + 8K bytes
  - Plane size: 1024 blocks = 128M bytes + 8M bytes
  - Device size: 2 planes = 2G bits + 128M bits
- **Standard, Dual and Quad SPI Protocols Supported**
  - Command on 1 pin, address on 1 pin, data output on 1, 2, 4 pins
  - Command on 1 pin, address on 2 or 4 pins, data output on 2 or 4 pins
  - Command on 1 pin, address on 1 pin, data input on 1 or 4 pins
- **Internal ECC**
  - User selectable
  - 8 bits per sector
- **Device Performance**
  - 133MHz maximum clock frequency
  - Page Read:
    - ◆ 25μs max with internal ECC Off
    - ◆ 70μs max with internal ECC On
  - Page Program:
    - ◆ 200μs typical with internal ECC Off
    - ◆ 220μs typical with internal ECC On
  - Block Erase: 2ms typical
- **Single Supply Voltage**
  - V_{CC}: 2.7~3.6V
- **Advanced Feature for NAND**
  - Read Unique ID
  - Read Parameter Page
  - Read Page Cache Mode
- **Write Protection Features**
  - Software protection with lock register
  - Hardware protection to freeze BP bits
  - Lock tight to protect control bits in the current power cycle
- **Security Feature**
  - Blocks 0 through 7 are valid upon delivery with ECC On
- **OTP Space**
  - 10 Pages of One-Time-Programmable NAND Flash memory space
- **Temperature Range**
  - Industrial: -40℃ to +85℃
- **Reliability**
  - Endurance: 100,000 Program/Erase Cycles
  - Data Retention: JESD47H-compliant
  - Data Retention (Uncycled): 10 Years at 85℃
- Industry Standard Packaging
  - WSON8 8*6

2. General Description

The NM5A02G01A is a 2Gbit Serial Peripheral Interface (SPI) NAND Flash memory device which supports standard SPI interface with Dual/Quad capabilities. This low pin count device has totally six signal pins: SCLK, CS#, SI (IO0), SO (IO1), WP# (IO2), HOLD# (IO3), which follows industry standard SPI interface and allows the user to easily migrate to other densities without PCB redesign.

The command set of this device is based on conventional SPI NOR Flash command set with modifications to accommodate the specific needs of NAND Flash memory architecture. As an alternative to SPI NOR Flash memories, this device offers storage capacities at lower price per bit.

The main array of the device is organized in planes, blocks and pages. Each page has 2048 bytes of data area and 128 bytes of spare area; the spare area is typically used for memory management and error management. The device has two registers on data input/output path, which includes a cache register placed near IO control logic, and a data register placed near the main memory array.

The device has internal ECC logic which is enabled by default after power-up. When a page of data is written to the memory array, an ECC code is also internally generated and automatically written to the spare area of the corresponding page. When a page of data is read from the main array to cache register, a new ECC code is automatically calculated, and the device compares the new ECC code and the one in spare area, corrects errors if necessary, and outputs corrected data or reports an ECC error status.

The device is read in read and programmed in page operations, and erased in block operations.

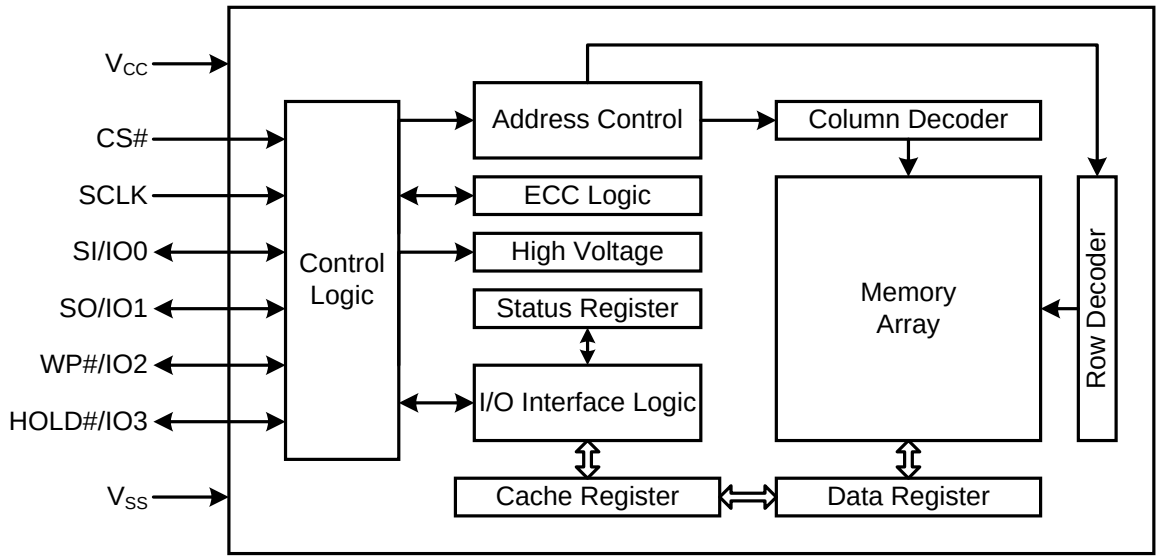
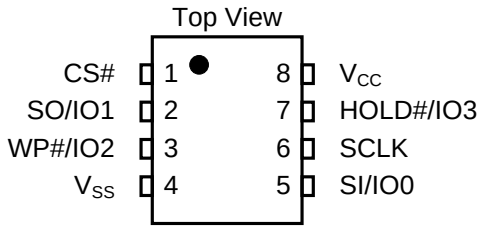


Figure 1: **NM5A02G01A SPI NAND Flash Block Diagram**

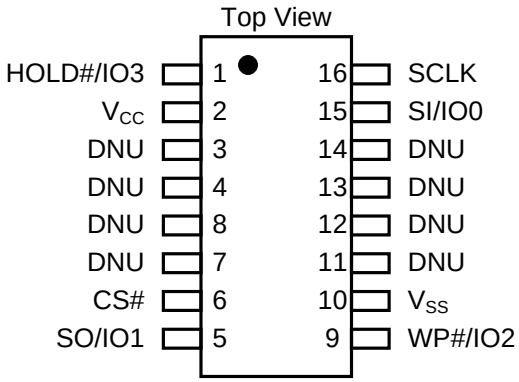
3. Pin Configuration

The NM5A02G01A device has the following pin configurations.

8-PIN U-PDFN



16-PIN SOP2



24-Ball T-PBGA

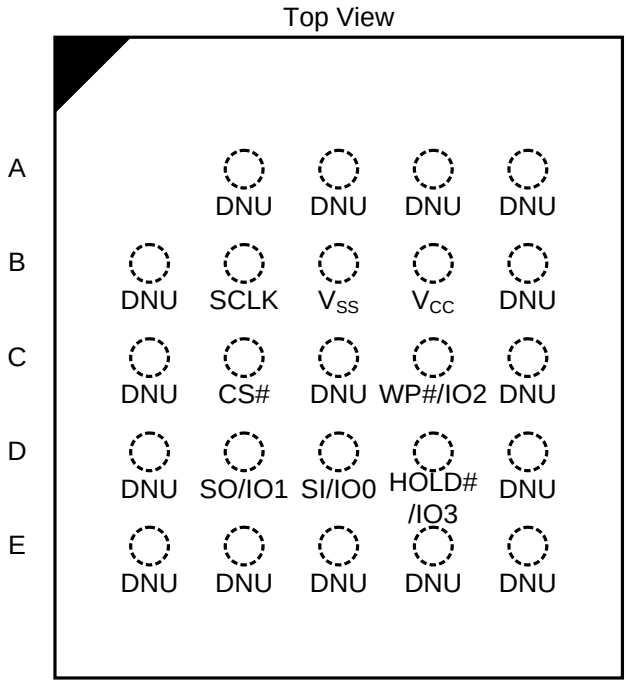


Figure 2: **Pin Map**

4. Pin Description

The NM5A02G01A SPI Flash memory device operates with a single power supply of 3.3V typical.

Table 1: **Pin Definitions**

Signal	Direction	Description
CS#	Input	Chip Select, active low
SCLK	Input	Clock Input
SI/IO0	Input/Output	Serial Data Input in standard SPI; IO0 in Dual and Quad modes.
SO/IO1	Input/Output	Serial Data Output in standard SPI; IO1 in Dual and Quad modes.
WP#/IO2	Input/Output	Active low Write Protect in standard SPI and Dual SPI; IO2 in Quad modes.
HOLD#/IO3	Input/Output	Active low Hold Input in standard SPI and Dual SPI; IO3 in Quad modes. For devices with hold functionality enabled, the HOLD# pin needs an external

		pullup resistor to avoid unexpected hold operations.
V_{CC}	-	Power Supply.
V_{SS}	-	Ground.
NC	-	Do Not Use. These pins should be left floating.

4.1. Chip Select (CS#)

The Chip Select (CS#) pin enables and disables device operations.
When CS# is high, the device is deselected and SO pin is at high impedance state; the device is in standby mode with standby level of power consumption if Write Status Register, Program or Erase operations are absent.
When CS# is low, the device is selected, available for incoming commands.

4.2. Clock Input (SCLK)

The clock input provides a reference of the synchronization of the SPI interface.
All inputs are latched on the rising edge of SCLK, while all data output are triggered by SCLK falling edge.

4.3. Serial Input (SI/IO0)

Serial input is a unidirectional pin in Standard SPI mode, which is the input for all commands, address and data. In Dual SPI and Quad SPI modes, SI functions as an bidirectional IO0, which transfers command, address and data information.

4.4. Serial Output (SO/IO1)

SO is unidirectional in Standard SPI mode for the output of all internal status and data. In Dual SPI and Quad SPI modes, SO functions as an bidirectional IO1, which transfers command, address and data information.

4.5. Write Protect (WP#/IO2)

The WP# Write Protect pin, when asserted low, protects BP[3:0] and TB bits from modifications if BRWD bit is set. When the device is deselected, this pin functions as an input.
When the device is in Quad mode, the WP# function is disabled and this pin functions as a dedicated IO2 pin. The host should not drive the WP# pin in Quad read operation, otherwise the device may be damaged due to signal contention.

4.6. HOLD (HOLD#/IO3)

The HOLD# function is enabled by default only for specific part numbers. For these devices, an external pullup resistor is required on HOLD# pin to avoid unexpected behavior.
Driving the HOLD# pin low halts all serial communications of the device, without affecting any ongoing Write, Program or Erase operations in progress. During hold state, SO is released to high impedance, and SI and SCLK are ignored by the device. Deasserting CS# while HOLD# is low will reset the internal logic of the device.
SCLK and HOLD# controls the entrance and exit of hold state. A falling edge of HOLD# during SCLK=0, or falling edge of SCLK during HOLD#=0 brings the device into HOLD state; a rising edge of HOLD# while SCLK=0, or falling edge of SCLK while HOLD#=1 brings the device out of HOLD state. The CS# should keep low during HOLD state.

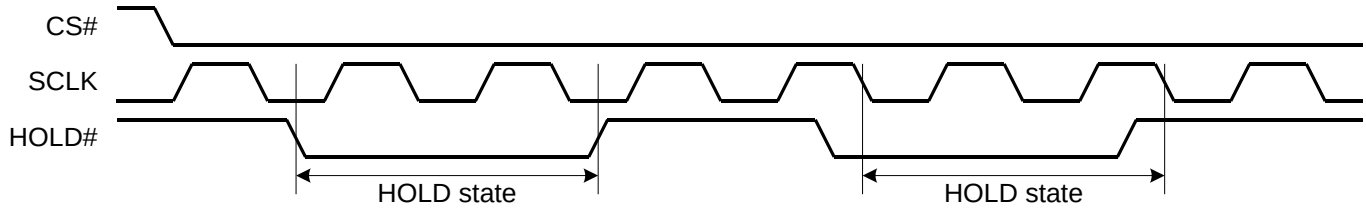


Figure 3: **HOLD Condition**

When the device is in Quad mode, the HOLD# function is disabled and this pin functions as dedicated IO3 pin; in such case, the host must not drive the HOLD# pin, otherwise the device may be damaged due to signal contention.

5. SPI Bus Operation

5.1. SPI Modes

The NM5A02G01A device supports two SPI modes, depending on CPOL (clock polarity) and CPHA (clock phase):

SPI Mode 0: CPOL = 0, CPHA = 0, SCLK remains at 0 during standby.

SPI Mode 3: CPOL = 1, CPHA = 1, SCLK remains at 1 during standby.

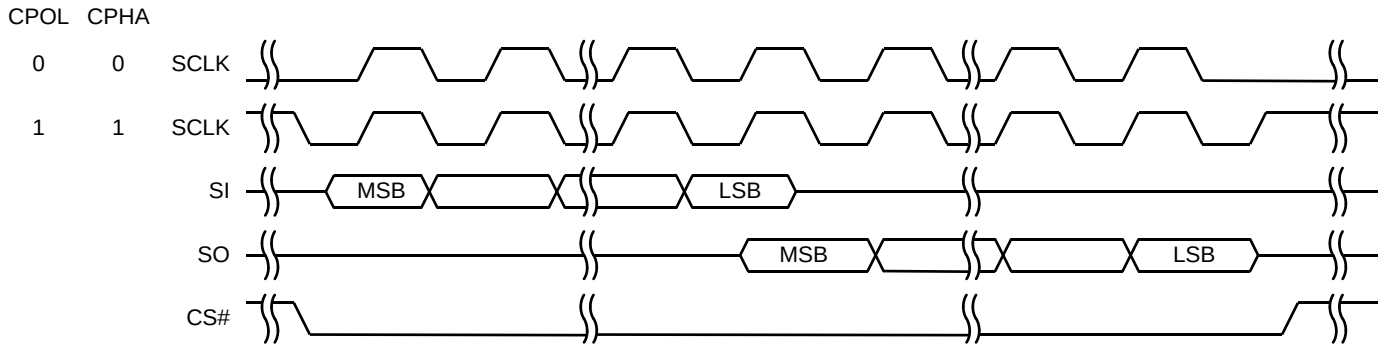


Figure 4: **SPI Mode 0 and Mode 3 Timing**

Depending on SPI being in mode 0 or mode 3, the SCLK pin should stay at V_{CC} or GND while the device is deselected with CS# asserted high. For simplicity's sake, all SPI timing diagrams in this document follow mode 0.

5.2. SPI Protocols

5.2.1. Standard SPI

The device supports standard SPI with a four signal bus: CS#, SCLK, SI and SO. Both mode 0 and mode 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.
In standard SPI mode, SI is input, SO is output, and an incoming command spans 8 SCLK cycles.

5.2.2. Dual SPI

The device features Dual SPI operations in which SI and SO pins become IO0 and IO1. Data is transferred using IO0 and IO1, doubling the throughput of Standard SPI protocol.

5.2.3. Quad SPI

The device also features Quad SPI operations in which SI, SO, WP# and HOLD# become IO0, IO1, IO2 and IO3, respectively. Data is transferred using IO0 through IO3, offering four times the throughput of Standard SPI protocols.
If Quad SPI is activated, it is strictly forbidden to tie WP# and HOLD# to power supply or GND to prevent signal

conflict which may damage the device permanently.

5.3. SPI NOR Read Protocol

This device uses a modification of conventional SPI NOR Flash command set to cater to the specific needs of NAND Flash architecture. However, this device can also follow the 03h/0Bh commands of conventional SPI NOR Read protocol for backward compatibility with systems deployed with SPI NOR Flash for boot.
For more details, see *Section 9.11 SPI NOR Read Configuration*.

6. Device Organization

The NM5A02G01A utilizes a variety of registers and memory array to store control information and user data.

6.1. Identification

The NM5A02G01A device has two bytes of identifier code that can be accessed by the user. They include ID information and device configuration information.

Table 2: **Identification Definitions**

Byte	Bit Value								Byte Value	Description
	7	6	5	4	3	2	1	0		
Byte 0	0	0	1	0	1	1	0	0	2Ch	Device Manufacturer ID.
Byte 1	0	0	1	0	0	1	0	0	24h	2Gbit 3.3V Device ID.

6.2. Main Array Organization

The address space distribution for the main memory array is given below.

Table 3: **NM5A02G01A Memory Organization**

A device has	A Plane has	A Block has	A page has	—
2	—	—	—	**Planes**
2,048	1,024	—	—	**Blocks**
131,072	65,536	64	—	**Pages**
285,212,672	142,606,336	139,264	2,176	**Bytes**

Notes:

1. The column address is 12 bits wide, and only address 0 through 2175 are valid. Address range from 2176 to 4095 is invalid.
2. Block RA6 selects a specific plane.

The device address is explained as follows:

Row Address[16:6] : Selects a specific block.
Row Address [5:0] : Selects a page within a block.
Column Address[11:0]: Selects a specific byte within a page.

The array organization of the device is shown below.

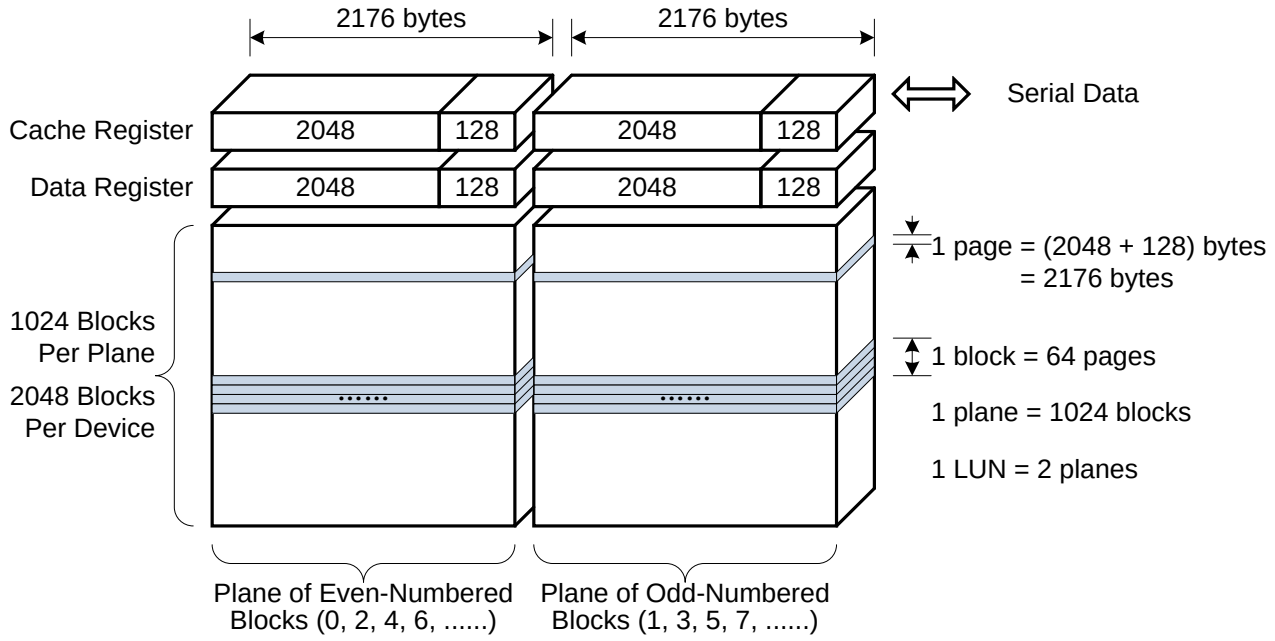


Figure 5: **Array Organization**

6.3. Parameter Page

The NM5A02G01A devices features an internal Parameter Table which includes flash device characteristics, providing a means for the host to interrogate and make appropriate adjustments while accessing the device.

Table 4: **Parameter Page Data Structure Table**

Byte	Description	Value(hex)
0-3	Parameter page signature	4Fh, 4Eh, 46h, 49h
4-5	Revision number	00h
6-7	Feature support	00h
8-9	Optional commands support	06h, 00h
10-31	Reserved	00h
32-43	Device manufacturer	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44-63	Device model: NM5A02G01AYI	4Dh, 54h, 32h, 39h, 46h, 32h, 47h, 30h, 31h, 41h, 42h, 41h, 47h, 44h, 53h, 46h, 20h, 20h, 20h, 20h
64	Manufacturer ID	2Ch
65-66	Date code	00h
67-79	Reserved	00h
80-83	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	Number of spare bytes per page	80h, 00h
86-89	Number of data bytes per partial page	00h, 02h, 00h, 00h
90-91	Number of spare bytes per partial page	20h, 00h
92-95	Number of pages per block	40h, 00h, 00h, 00h
96-99	Number of blocks per unit	00h, 08h, 00h, 00h
100	Number of logical units	01h
101	Number of address cycles	00h

102	Number of bits per cell	01h
103-104	Bad blocks maximum per unit	28h, 00h
105-106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	08h
108-109	Block endurance for guaranteed valid blocks	00h
110	Number of programs per page	04h
111	Partial programming attributes	00h
112	Number of ECC bits	00h
113	Number of interleaved address bits	00h
114	Interleaved operation attributes	00h
115-127	Reserved	00h
128	I/O pin capacitance	08h
129-130	Timing mode support	00h
131-132	Program cache timing	00h
133-134	tPROG maximum page program time	58h, 02h
135-136	tERS maximum block erase time	10h, 27h
137-138	tR maximum page read time	46h, 00h
139-140	tCCS minimum	00h
141-163	Reserved	00h
164-165	Vendor-specific revision number	00h
166-179	Vendor specific	01h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 02h, 02h, B0h, 0Ah, B0h
180-247	Reserved	00h
248	ECC maximum correct ability	08h
249	Die select feature	00h
250-253	Reserved	00h
254-255	Integrity CRC	Set at Test
256-512	2nd copy of the parameter table	
513-768	3rd copy of the parameter table	
769-2048	Additional redundant parameter pages	

6.4. Unique ID

The device has sixteen copies of unique ID in its internal storage, each copy being 32 bytes in length. Within each copy, the first 16 bytes are the unique data, with the second 16 bytes being its complement, which enables the host to utilize XOR operation to check for data integrity. Should the XOR data check fail, the host can repeat the XOR operations on subsequent copies until a correct copy is detected.

6.5. Feature Register

The device has four 1-byte internal feature registers that can both be polled by the host to detect the device status, or be written by the host to modify device configuration from their default values. During read or write operations, each feature register is be addressed by a 1-byte feature address.

Using Set Features 1Fh command, the host can set internal control bits of the device, including block locking,

ECC correction, protocol configuration, OTP protect. Once a feature bit is written by the host, it will remain active until device power-down or the bit is written again, and it will remain active even a Reset command FFh is issued (unless otherwise specified). An exception is bits CFG[2:0]; a reset operation can clear CFG[2:0] to 000 and bring the device back to normal operation.

6.5.1. Block Lock

Table 5: **Feature Register: Block Lock**

Feature Address	Access	Feature Data Bit Definition							
		7	6	5	4	3	2	1	0
A0h	R/W	BRWD	BP3	BP2	BP1	BP0	TB	WP#/HOLD# Disable	—

When WP#/HOLD# bit is 0, BRWD bit is 1, and WP# pin is Low, bits [7:2] of Block Lock register is protected against modifications.

6.5.1.1. BRWD Bit

The Block Register Write Disable bit is used for data protection. The power-up default value is 0.

For details, see *Section 8.2 Hardware Write Protection* and *Section 8.3 Device Lock Tight (LOT)*.

6.5.1.2. BP3, BP2, BP1 and BP0 Bits

BP[3:0] are Block Protect bits. Default values are all 1s.

Block lock bits include BP[3:0] and TB bits; they together define the protection scheme of the device main memory array. For details, see *Section 8.1 Volatile Block Protection of Main Array*.

6.5.1.3. TB Bit

TB is the Top/Bottom bit. It determines whether the memory protection mechanism starts from the Top or Bottom address of the memory array.

0: Top area protect.

1: Bottom area protect (default value).

For more details, see *Section 8.1 Volatile Block Protection of Main Array*.

6.5.1.4. WP#/HOLD# Disable Bit

This bit is used for security and data protection. The power-up default value is 0.

For details, see *Section 8.2 Hardware Write Protection*.

6.5.2. Configuration

Table 6: **Feature Register: Configuration**

Feature Address	Access	Feature Data Bit Definition							
		7	6	5	4	3	2	1	0
B0h	R/W	CFG2	CFG1	LOT_EN	ECC_EN	—	—	CFG0	—

6.5.2.1. CFG2, CFG1 and CFG0 Bits

The CFG[2:0] bits are Configuration Registers for Security purposes.

CFG[2:0]=000: Normal operation

CFG[2:0]=010: Access OTP area/Parameter/Unique ID

CFG[2:0]=110: Access to OTP data protection bit to lock OTP area

CFG[2:0]=101: Access to SPI NOR read protocol enable mode

CFG[2:0]=111: Access to permanent block lock protection disable mode

6.5.2.2. LOT_EN Bit

This bit enables the Device Lock Tight (LOT) feature.

0: LOT feature disabled.

1: LOT feature enabled.

See *Section 8.3* Device Lock Tight (LOT) for details.

6.5.2.3. ECC_EN Bit

This bit enables the internal ECC feature for error detection and correction.

0: ECC feature disabled.

1: ECC feature enabled.

6.5.3. Status

The status register at feature address C0h is typically polled by the host to detect the status of device while the device is in operations. This register is read-only, with the exception of WEL bit which can be affected by the Write Enable 06h and Write Disable 04h commands.

Table 7: **Feature Register: Status**

Feature Address	Access	Feature Data Bit Definition							
		7	6	5	4	3	2	1	0
C0h	R	CRBSY	ECCS2	ECCS1	ECCS0	P_Fail	E_Fail	WEL	OIP

The status register bits cannot be changed by Set Feature command 1Fh, but can be read using Get Features command 0Fh with feature address C0h.

6.5.3.1. CRBSY Bit

The Cache read busy bit indicates the status of Read Page Cache Random command 30h.

0: Device is in ready state; read page cache operation in background is complete.

1: Read Page Cache Random command 30h is still in progress. This bit remains at 1 until the device has internally transferred the page specified by 30h command from main array to data register.

While the CRBSY bit is 1, a Reset command pauses the read page cache operation in background, and loads the first page of block 0 into cache register by default.

6.5.3.2. ECCS2, ECCS1 and ECCS0 Bits

The ECC status bits provide a means to indicate the error correction and detection status of internal ECC operations for Program and Read commands.

ECCS[2:0]=000: No errors are detected.

ECCS[2:0]=001: 1-3 bits of error is detected and corrected.

ECCS[2:0]=010: Bit errors greater than 8 bits are detected and not corrected.

ECCS[2:0]=011: 4-6 bits of error is detected and corrected. It is suggested to perform data refreshment.

ECCS[2:0]=101: 7-8 bits of error is detected and corrected. Data refreshment is needed for data retention.

ECCS[2:0]=Others: Reserved

After device power up reset, ECCS bits indicate the contents of page 0 in block 0. At the beginning of a Read operation, or after a Reset command, ECCS bits are set to 000b; they are then updated to reflect the result of ECC operation after a valid Read operation completes.

ECCS bits are invalid if ECC is disabled.

6.5.3.3. P_Fail Bit

P_Fail bit indicates a program failure.

0: No program failure is present.

1: A program failure is detected.

This bit is cleared to 0 during Program Execute command or after a Reset command.

This bit is set to 1 when a program operation fails, or the host seeks to program an invalid address, a lock address, a protected address, including OTP area.

6.5.3.4. E_Fail Bit

E_Fail bit indicates an erase failure.

0: No erase failure is present.

1: An erase failure is detected.

This bit is cleared to 0 at the beginning of a Block Erase command or after a Reset command.
This bit is set to 1 when an erase operation fails, or the host seeks to erase a locked area.

6.5.3.5. WEL Bit

This bit indicates the current value of the Write Enable Latch:

0: Write Enable Latch is 0.
1: Write Enable Latch is 1.

This bit is set to 1 by the Write Enable command, and cleared to 0 by the Write Disable command or the successful completion of a Program / Erase operation.

6.5.3.6. OIP Bit

The Operation In Progress bit indicates whether a Program Execute, Page Read, Read Page Cache Last, Block Erase, Read Page Cache Random is in execution, which falls within tRCBSY and waits for the cache register to become ready. It also signifies the state of Reset command or a power-up initialization process.

0: The device is ready.
1: The device is busy.

6.5.4. Die Select

Table 8: **Feature Register: Die Select**

Feature Address	Access	Feature Data Bit Definition							
		7	6	5	4	3	2	1	0
D0h	R/W	—	DS0	—	—	—	—	—	—

6.5.4.1. DS0 Bit

This bit is for die selection.

7. ECC Protection

The NM5A02G01A device provides internal ECC function to improve data integrity. The built-in ECC is enabled upon power-up by default, and it can be turned off using the ECC_EN bit, but is not affected by Reset command. The ECC mechanism protects the main memory array without the unique ID and parameter page. The data integrity of unique ID and parameter page is guaranteed by storing multiple copies of the same data; besides, XOR method can be used to verify the correctness of unique ID data.
With ECC enabled, the Program and Read operations are executed with error detection and correction capabilities which can correct up to 8 bits of error in a page. The host can poll the ECC status register bits for the result of ECC error detection and correction operations.

7.1. ECC in Program Operations

For Program operations, before data is transferred to the main memory array, the device automatically calculates an ECC code from the ECC-protected area in cache register, and stores the code in the spare area of the page.

7.2. ECC in Read Operations

During Read operations, when data is transferred to the cache register, the device automatically calculates the ECC code and compare it with the one stored in the main array. If 1 to 8 bits of error is found, then the cache register is loaded with corrected data; however, if 9 or more error bits exist in a single page, it is beyond the ECC capabilities and there will be no attempts to correct the data.

7.3. ECC Protection Rules

When internal ECC is enabled, users should consider the spare area definitions. Write operations are acceptable for main and spare areas (user meta data I and II); Write operation to ECC area is prohibited.
For partial-page programming, the following rules should be observed:

(1) In main and user meta data I areas, single partial-page programming should be used.
(2) Within a single page, it is acceptable to perform a maximum of four partial-page programming operations.

Table 9: **ECC Protection**

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh	000h	Yes	Main 0	User Main data 0
3FFh	200h	Yes	Main 1	User Main data 1
5FFh	400h	Yes	Main 2	User Main data 2
7FFh	600h	Yes	Main 3	User Main data 3
803h	800h	No	Spare 0	Reserved (bad block data)
807h	804h	No	Spare 1	User meta data II
80Bh	808h	No	Spare 2	User meta data II
80Fh	80Ch	No	Spare 3	User meta data II
813h	810h	No	Spare 0	User meta data II
817h	814h	No	Spare 1	
81Bh	818h	No	Spare 2	
81Fh	81Ch	No	Spare 3	
827h	820h	Yes	Spare 0	User meta data I
82Fh	828h	Yes	Spare 1	
837h	830h	Yes	Spare 2	
83Fh	838h	Yes	Spare 3	
84Fh	840h	Yes	Spare 0	ECC for Main/Spare 0
85Fh	850h	Yes	Spare 1	ECC for Main/Spare 1
86Fh	860h	Yes	Spare 2	ECC for Main/Spare 2
87Fh	870h	Yes	Spare 3	ECC for Main/Spare 3

8. Security and Data Protection

As a nonvolatile memory device the NM5A02G01A may suffer from the compromise of data integrity in the event of noise and other adverse system conditions. To improve the robustness of the device, certain methods are adopted to protect the data from inadvertent Write, Program or Erase operations.

8.1. Volatile Block Protection of Main Array

A combination of feature register bits define the area space of the memory array that is protected from program and erase operations. A program or erase operation targeted at a locked block is not executed, and the P_Fail or E_fail bit in status register will be internally asserted to indicate such failure.
A detailed protection scheme is specified in the table below.

Table 10: **NM5A02G01A Memory Protection Pattern**

Status Register Bits					Memory Space in Protection	
TB	BP3	BP2	BP1	BP0	Protected Portion	Protected Blocks
0	0	0	0	0	None—all unlocked	None
0	0	0	0	1	Upper 1/1024 locked	2046:2047
0	0	0	1	0	Upper 1/512 locked	2044:2047
0	0	0	1	1	Upper 1/256 locked	2040:2047
0	0	1	0	0	Upper 1/128 locked	2032:2047
0	0	1	0	1	Upper 1/64 locked	2016:2047
0	0	1	1	0	Upper 1/32 locked	1984:2047

0	0	1	1	1	Upper 1/16 locked	1920:2047
0	1	0	0	0	Upper 1/8 locked	1792:2047
0	1	0	0	1	Upper 1/4 locked	1536:2047
0	1	0	1	0	Upper 1/2 locked	1024:2047
1	0	0	0	0	All unlocked	None
All others					All locked	0:2047
1	0	0	0	1	Lower 1/1024 locked	0:1
1	0	0	1	0	Lower 1/512 locked	0:3
1	0	0	1	1	Lower 1/256 locked	0:7
1	0	1	0	0	Lower 1/128 locked	0:15
1	0	1	0	1	Lower 1/64 locked	0:31
1	0	1	1	0	Lower 1/32 locked	0:63
1	0	1	1	1	Lower 1/16 locked	0:127
1	1	0	0	0	Upper 1/8 locked	0:255
1	1	0	0	1	Lower 1/4 locked	0:511
1	1	0	1	0	Lower 1/2 locked	0:1023
1	1	1	1	1	All locked (default)	0:2047

The device is default to power up in locked state with BP[3:0] and TB all being 1s; these bits are not affected by reset operations. To unlock all blocks after power up, the Set Features command 1Fh should be used with feature address A0h and data 00h.

8.2. Hardware Write Protection

A hardware write protection scheme protects the block lock register bits from unexpected modifications: The host issues the Set Feature command 1Fh with feature address A0h, and set the Block Lock register to appropriate data pattern.

When BRWD bit is 1 and WP# pin is low, Block Lock register bits [7:2] are protected against modifications regardless of their unlock/lock status; when the WP#/HOLD# Disable bit is 1, the hardware protection mode is disabled.

8.3. Device Lock Tight (LOT)

When the LOT_EN bit is set to 1, the device is in lock tight (LOT) mode, in which the PB, TB and BRWD bits are protected against software modifications until device power down, which further prevents a change in the block protection pattern. Once entered, the LOT mode cannot be disabled by any software command; it can only be disabled by power cycling the device.

8.4. Permanent Block Lock Protection

Permanent Block Lock Protection is a series of Protect command sequence that can be used to permanently and irreversibly protect up to 48 blocks per die. This protection is implemented in terms of groups. In this device, a group is composed of four blocks; consequently, a minimum of one group or four blocks can be permanently protected. Once taken effect, such protection mechanism is nonvolatile and irreversible; power cycling the device cannot disable the protection scheme.

The device is shipped without Permanent Block Lock Protection, so that the entire memory space is available for program or erase operations.

See *Section 9.8 Protection* for details.

8.5. One Time Programmable (OTP) Area

For this device, each die offers ten full pages (10 pages×2176 bytes per page) of one-time programmable (OTP)

Nand Flash memory space which is under protection. The row address of OTP pages are 02h through 0Bh. The OTP pages can be programmed only once, but cannot be erased. OTP data can be protected by ECC if ECC is enabled.

The host can use OTP area for serial number or whatever that needs permanent storage.

See *Section 9.9 OTP Operations* for details.

9. Command Definitions

All commands, addresses and data are shifted in and out of the device with MSB first.

Every command sequence starts with a one-byte command code. Depending on the operation, the command byte might be followed by address bytes, data bytes, dummy bytes, or their combination. CS# must be driven high after the last bit of the command sequence is completed.

9.1. Command Summary

Table 11: **Command Definitions**

Command	Command Byte	Address Bytes	Dummy Bytes	Data Bytes	Description
Reset	FFh	0	0	0	Perform reset on the device.
Get Features	0Fh	1	0	1	Read feature table.
Set Features	1Fh	1	0	1	Write feature table.
Read ID	9Fh	0	1	2	Read device ID code.
Page Read	13h	3	0	0	Array read.
Read Page Cache Random	30h	3	0	0	Cache read.
Read Page Cache Last	3Fh	0	0	0	End of cache read.
Read From Cache x1	03h, 0Bh	2	1	1 - 2176	Read cache data from specified address.
Read From Cache x2	3Bh	2	1	1 - 2176	Read cache data and output at two pins: IO0 and IO1.
Read From Cache x4	6Bh	2	1	1 - 2176	Read cache data and output at four pins: IO0 through IO3.
Read From Cache Dual IO	BBh	2	1	1 - 2176	Input address and output data are communicated via IO0 and IO1.
Read From Cache Quad IO	EBh	2	2	1 - 2176	Input address and output data are communicated via IO0 through IO3.
Write Enable	06h	0	0	0	Asserts WEL bit to 1. Prerequisite for any command that changes data in the memory array.
Write Disable	04h	0	0	0	Clears WEL bit to 0. Disables the device for any changes in the memory array.
Block Erase	D8h	3	0	0	Erase the data contents of a specified block.
Program Execute	10h	3	0	0	Program the memory array.
Program Load x1	02h	2	0	1 - 2176	Load program data into cache register from SI.
Program Load x4	32h	2	0	1 - 2176	Load program data into cache register from IO0 through IO3.
Program Load Random Data x1	84h	2	0	1 - 2176	Write cache register with incoming data from SI.
Program Load Random Data x4	34h	2	0	1 - 2176	Write cache register with incoming data from IO0 through IO3.
Permanent Block Lock Protection	2Ch	3	0	0	Permanently prevent a group of blocks from any modifications.

9.2. Reset Operation (FFh)

The Reset commands aborts all on-going internal Read, Program, Erase operations, and brings the device back to a known state. After Reset command is issued, it takes a duration tPOR for the command to take effect; during tPOR, the Get Feature command can be used to monitor the status register for OIP bit.

After the device is reset, the cache register is automatically loaded with the data from the first page of the first block. The impact of Reset command on device registers is listed as below:

Status register:

ECC bits: Updated.

Other bits: Cleared.

Configuration register:

CFG[2:0]: Cleared.

Other bits: Not reset.

Block lock register:

Not cleared until power cycling or written by Set Feature command.

Data corruption may occur if Reset command is used to interrupt an ongoing Program or Erase operation.

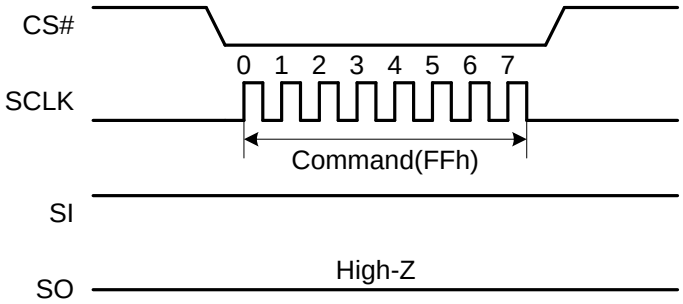


Figure 6: **Reset (FFh) Command Timing**

9.3. Write Operations

9.3.1. Write Enable (WREN) (06h)

The WREN command sets the WEL bit to 1, which is a prerequisite prior to any command that modify the device contents:

Page Program

OTP Area Program

Block Erase

Permanent Block Lock Protection

These commands are ignored by the device without prior WREN command.

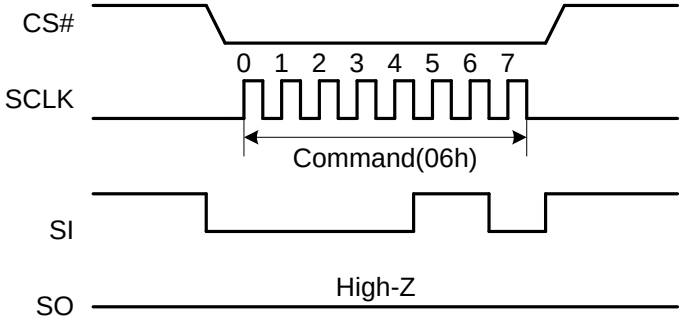


Figure 7: **Write Enable (WREN) (06h) Command Timing**

9.3.2. Write Disable (WRDI) (04h)

The WRDI command clears the WEL bit to 0, which disables the page Program, OTP Area Program or Block

Erase commands.

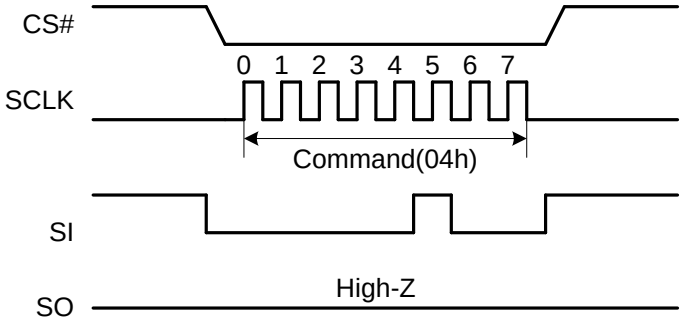


Figure 8: **Write Disable (WRDI) (04h) Command Timing**

9.4. Read Operations

9.4.1. Page Read (13h)

A Page Read 13h command reads data from main memory array to cache register, which requires a busy time duration of tRD. During tRD, the Get Features command can be used to monitor the status of the operation. After Page Read has successfully transferred data to the cache register, the host should use the Read From Cache command to read the data from cache register.

Table 12: **Page Read (13h) Command Sequence**

Step	Opcode	Command	Description
1	13h	Page Read	Move data from main memory array to cache register.
2	0Fh	Get Features	Poll the status of the operation.
3	03h or 0Bh	Read From Cache	Any one of these commands can be used to enable the device to output data from cache register.
	3Bh	Read From Cache x2	
	6Bh	Read From Cache x4	
	BBh	Read from Cache Dual IO	
	EBh	Read From Cache Quad IO	

The Page Read command 13h require a 24-bit address, which consists of 7 dummy bits and 17 bits of block/page address.

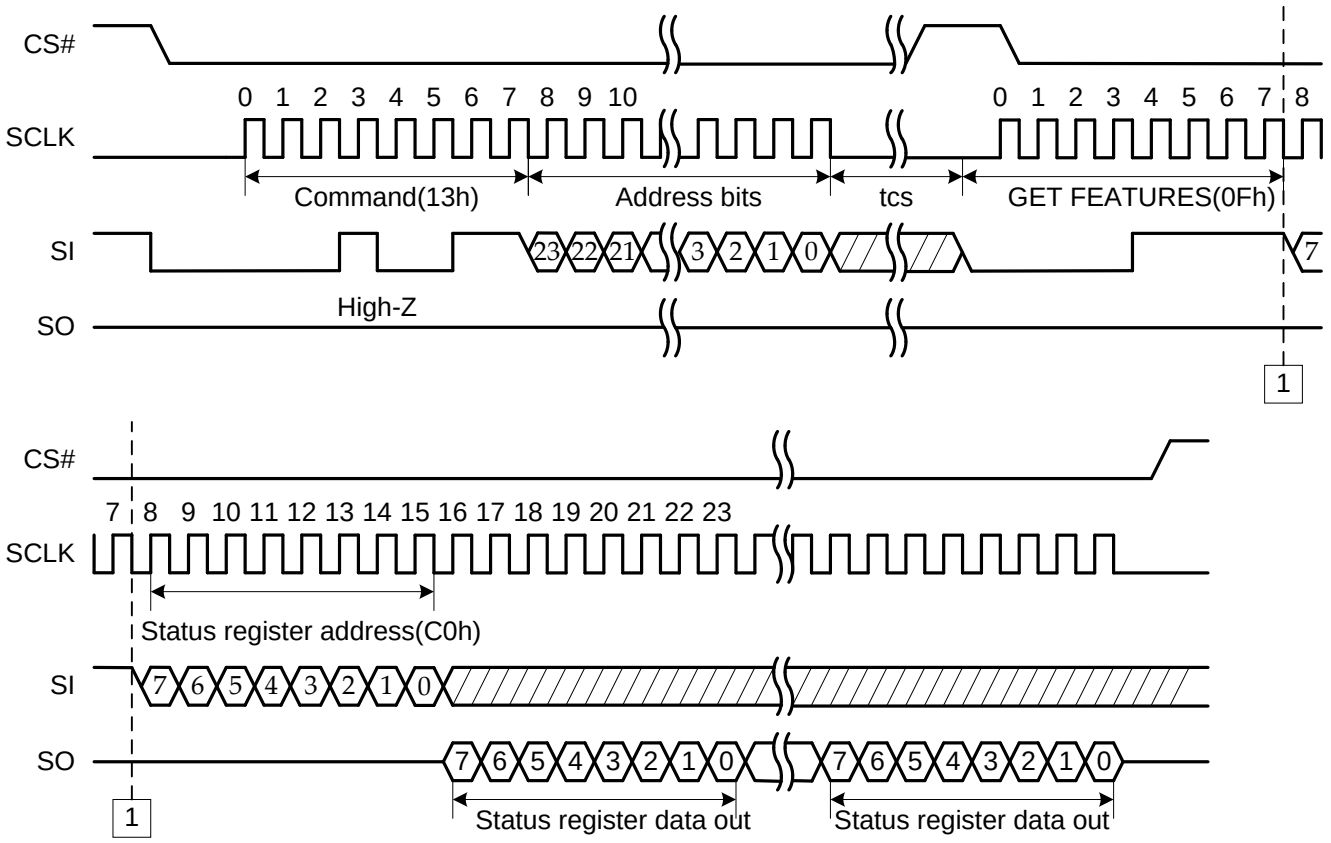


Figure 9: **Page Read (13h) Command Timing**

9.4.2. Read From Cache x1 (03h or 0Bh)

The Read From Cache x1 command 03h or 0Bh reads data bytes from the cache register; data is output with MSB first. After each byte is shifted out, the address automatically increments to the next byte location, creating a continuous output data stream. Both 03h and 0Bh commands operate in fast mode.

The command sequence is:

Drive CS# pin low --> Shift in command byte --> Shift in 16 bits of column address --> Shift in 8 bits of dummy clock --> Shift out read data starting from the specified address --> The host may terminate the command by driving CS# high at any time during data output.

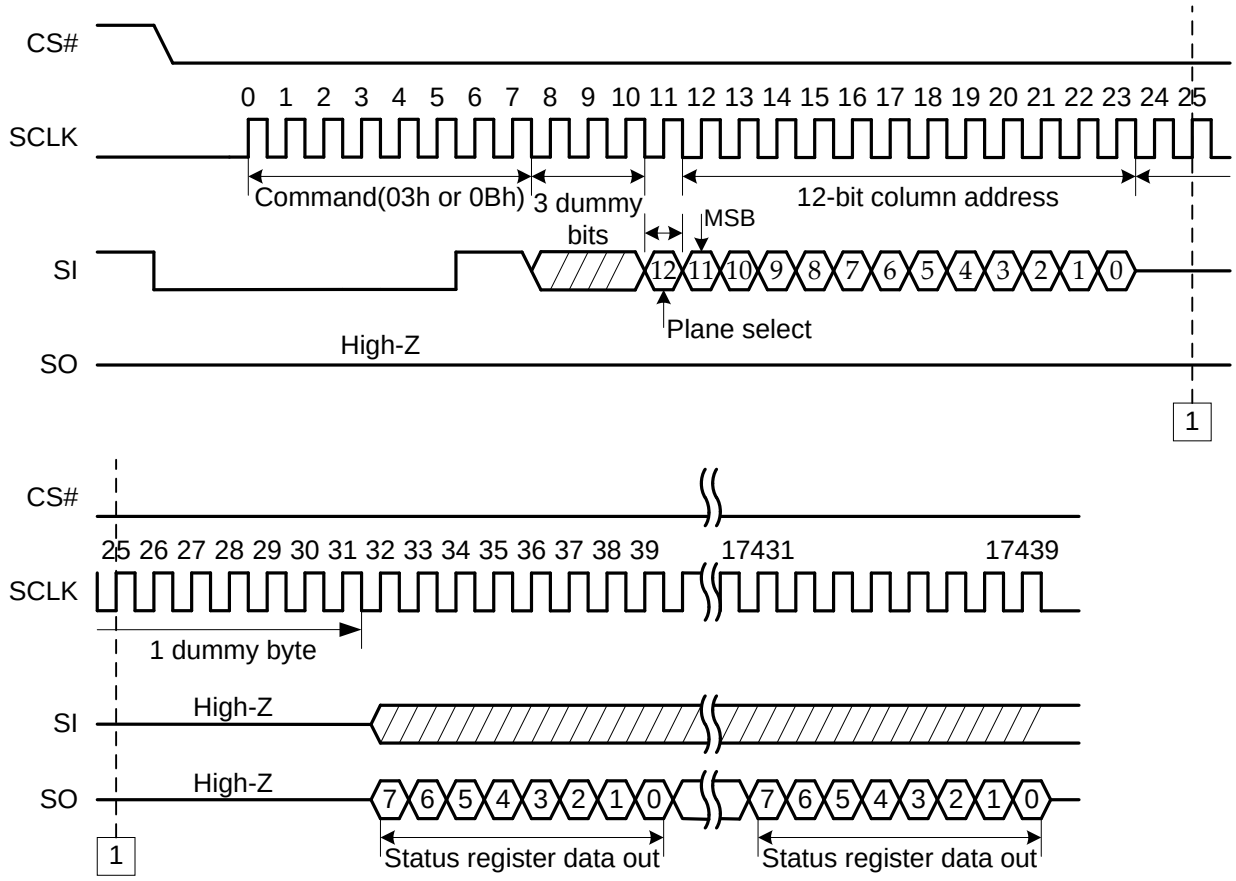


Figure 10: **Read From Cache (03h or 0Bh) Command Timing**

9.4.3. Read From Cache x2 (3Bh)

The Read From Cache x2 command 3Bh functions similar to Read From Cache x1 (03h or 0Bh) command, with the exception that data outputs on IO0(SI) and IO1(SO), allowing output data to be transferred at twice the throughput.

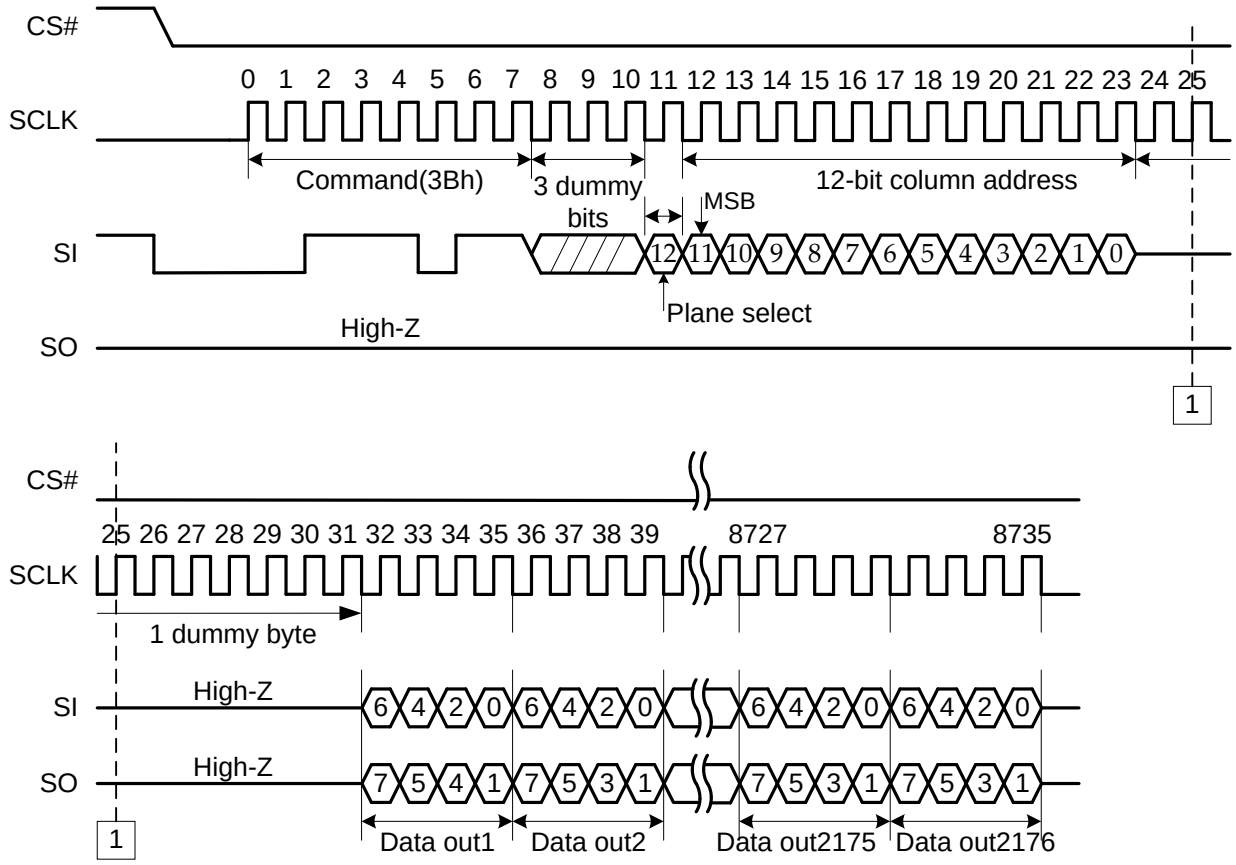


Figure 11: **Read From Cache x2 (3Bh) Command Timing**

9.4.4. Read From Cache x4 (6Bh)

The Read From Cache x4 command 6Bh functions similar to Read From Cache x1 (03h or 0Bh) command, with the exception that data outputs on IO0, IO1, IO2 and IO3, allowing output data to be transferred at four times the throughput.

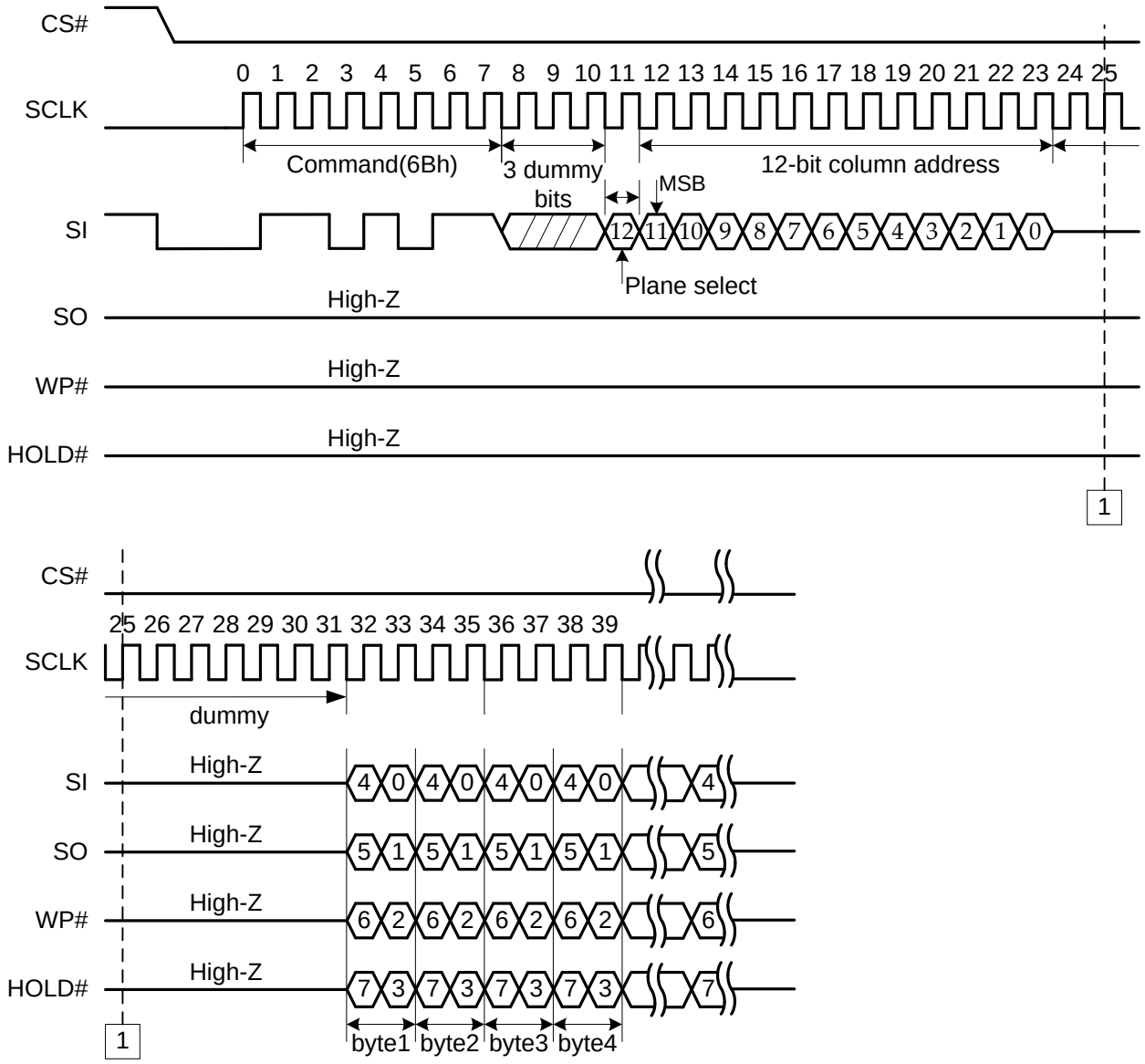


Figure 12: **Read From Cache x4 (6Bh) Command Timing**

9.4.5. Read From Cache Dual IO (BBh)

The Read From Cache Dual IO command BBh functions similar to Read From Cache x2 command 3Bh, with the exception that the column address and dummy clocks are communicated using IO0(SI) and IO1(SO), allowing command overhead to be reduced.

The clock frequency supported by BBh command is listed in *Section 12 Electrical Characteristics*.

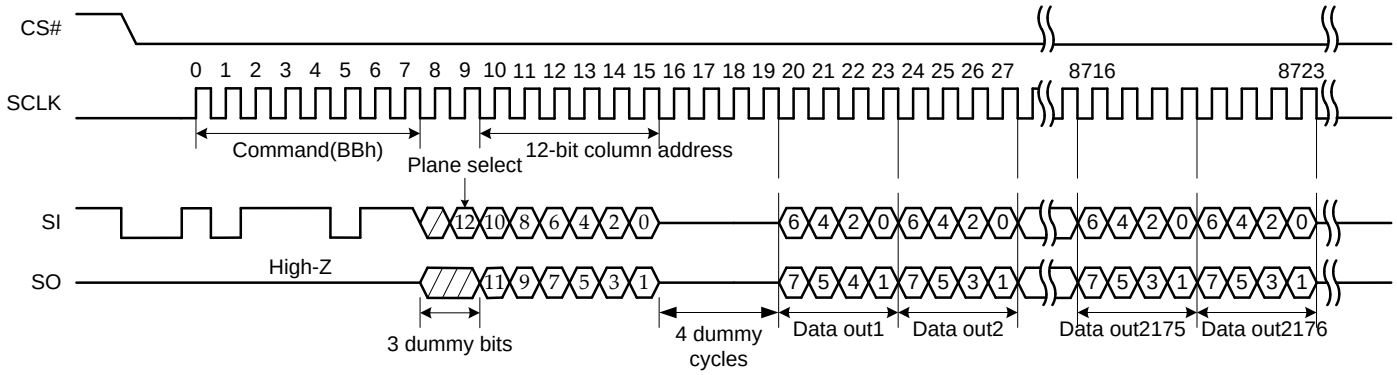


Figure 13: **Read From Cache Dual IO (BBh) Command Timing**

9.4.6. Read From Cache Quad IO (EBh)

The Read From Cache Quad IO command EBh functions similar to Read From Cache Dual IO command BBh, with the exception that address and data are communicated using pins IO0 through IO3, allowing command overhead to be further reduced for faster random access into cache register.

The clock frequency supported by EBh command is listed in *Section 12 Electrical Characteristics*.

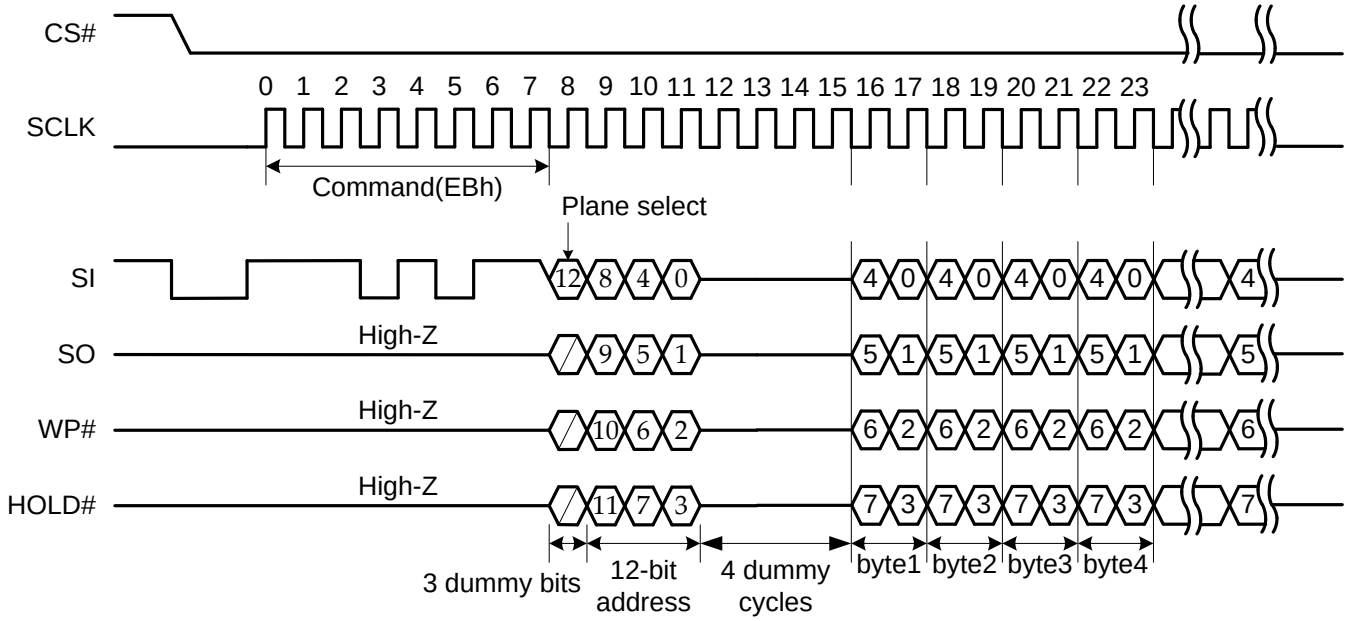


Figure 14: **Read From Cache Quad IO (EBh) Command Timing**

9.4.7. Read Page Cache Random (30h)

The Read Page Cache Random command 30h improves read throughput by reading data from specified address in the main array into data register, while the device outputs data of the previous page from cache register. The 30h command is accepted when the die is ready with OIP=0 and CRBSY=0.

Table 13: **Read Page Cache Random (30h) Command Sequence**

Step	Opcode	Command	Description
1	13h	Page Read	Move data from main memory array to cache register.
2	0Fh	Get Feature	Poll the status until OIP bit changes from 1 to 0.
3	30h	Read Page Cache Random	1. Move data from data register to cache register; 2. Read the next page of data from main array to data register.
4	0Fh	Get Feature	Poll the status until OIP bit changes from 1 to 0.
5	03h, 0Bh, 3Bh, 6Bh, BBh or EBh	Read From Cache to Output	The device outputs data from the cache register.
6	0Fh	Get Feature	Poll the status until CRBSY is 0.
7	Repeat Steps 3 through 6 to output all pages except the last page.		
8	3Fh	Read Page Cache Last	1. Copy the last page from data register to cache register. 2. Terminate the read page cache sequence.
9	0Fh	Get Feature	Poll the status until OIP bit changes from 1 to 0.
10	03h, 0Bh, 3Bh, 6Bh, BBh or EBh	Read From Cache to Output	The device outputs data of the last page from the cache register.

The Read Page Cache Random command 30h require a 24-bit address, which consists of 7 dummy bits followed by 17 bits of block/page address.

For 30h command, after the address bits are input, it takes tRCBSY for the device to move data from data register to cache register; after tRCBSY, OIP bit changes from 0 to 1 (which can be checked by the Get Feature command),

which indicates that the cache register is ready to output data, and the page addressed by 30h command is being copied from the main array to the data register. During tRCBSY, the device internally performs error detection and correction.

After OIP becomes 1, the host may use Read From Cache commands to output data from the cache register. The CRBSY bit remains 1 to indicate that the page addressed by 30h command is being copied from the main array to data register; after data copy is complete, CRBSY bit returns to 0.

For devices with on-die ECC-enabled, ECC is performed after data is copied from data register to cache register; such ECC execution time is included in tRCBSY, which should be taken into consideration when polling for OIP bit value.

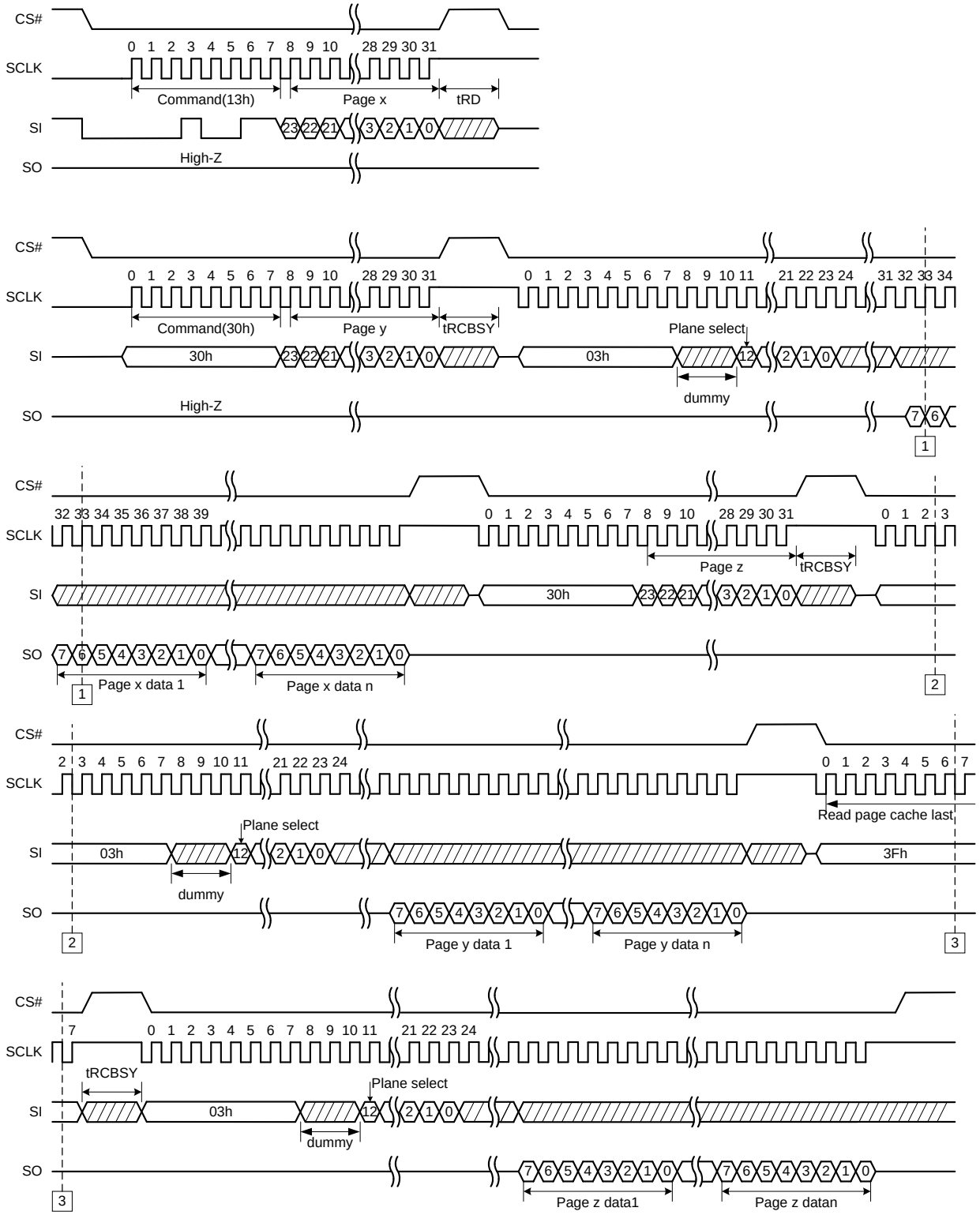


Figure 15: **Read Page Cache Random (30h) Command Timing**

9.4.8. Read Page Cache Last (3Fh)

The Read Page Cache Last command 3Fh copies a page of data from data register to cache register, and terminates the Read Page Cache Random 30h command. The host can send this command when the die is ready with OIP=0, CRBSY=0; after the 3Fh command is sent, OIP bit becomes 1 and the device becomes busy with OIP=1, CRBSY=0 for a duration of tRCBSY. After data has been copied into cache register, OIP bit becomes 0 and the device is ready to output data from cache register.

9.4.9. Read ID (9Fh)

The Read ID command 9Fh reads the 2-byte ID information from the device. The ID values are defined in *Table **2**:* Identification Definitions.

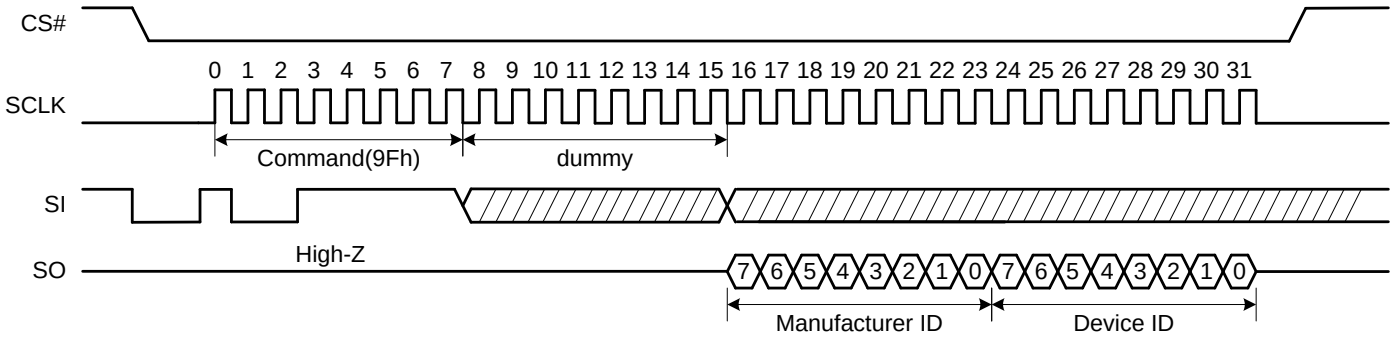


Figure 16: **Read ID (9Fh) Command Timing**

9.4.10. Read Parameter Page

The following procedure is used to access the parameter page of the device.

Table 14: **Read Parameter Page Command Sequence**

Step	Opcode	Command	Description
1	1Fh	Set Features	Use with feature address B0h and data with CFG[2:0] being 010b to access OTP / Parameter / Unique ID pages.
2	13h	Page Read	Issue this command with block/page address of 0x01h.
3	0Fh	Get Features	Use with feature address C0h to check the status of read operation.
4	03h	Read From Cache	Use with address 0x00h to read data from the device. See *Table **4**: Parameter Page Data Structure Table* for details regarding the parameter page.
5	1Fh	Set Features	Use with feature address B0h and data being 00h to exit the parameter page read process.

9.4.11. Read Unique ID Page

The following procedure is used to access the unique ID page of the device.

Table 15: **Read Unique ID Page Command Sequence**

Step	Opcode	Command	Description
1	1Fh	Set Features	Use with feature address B0h and data being 40h to access OTP area / Parameter / Unique ID. ECC disable.
2	13h	Page Read	Issue this command with block/page address of 0x00h.
3	0Fh	Get Features	Use with feature address C0h to check OIP bit until the device is ready.
4	03h	Read From Cache	Use with address 0x00h to read Unique ID data from the device. See *Section 6.4 Unique ID* for details regarding the Unique ID.

5	1Fh	Set Features	Use with feature address B0h and data being 10h or 00h (read main memory array, ECC enable or disable) to exit the Unique ID read process.

9.5. Program Operations

9.5.1. Page Program

A Page Program operation transfers 1 ~ 2176 bytes of data within a page to the cache register, and then further moves the data from cache register to a specified block/page address in the main memory array. A program operation may change data bits from 1 to 0, but not the reverse. To change data bits from 0 to 1, erase operation is required instead.

Prior to program operation, a Write Enable command should be issued set the WEL bit to enable the device.

A single page accepts a maximum of four partial-page program operations. Only the first 2176 bytes are valid and data beyond 2176 bytes are discarded by the device.

Table 16: **Page Program Command Sequence**

Step	Opcode	Command	Description
1	06h	Write Enable	Enable the device for program operation.
2	02h	Program Load	Specifies the target address and data bytes to be loaded into the cache register.
3	10h	Program Execute	Transfer program data from cache register to main memory array.
4	0Fh	Get Features	Poll for the status of program operation.

9.5.2. Program Load x1 (02h)

The Program Load x1 command 02h feeds program data into the cache register of the device. The command sequence is as follows:

Drive CS# pin low --> Shift in command byte --> Shift in 3 dummy bits --> Shift in plane select if available --> Shift in 12 bits of column address --> Shift in program data bytes --> Drive CS# pin high.

Data bytes are loaded into the 2176-byte cache register. Data beyond 2176 bytes are ignored by the device. A single page accepts a maximum of four partial-page program operations.

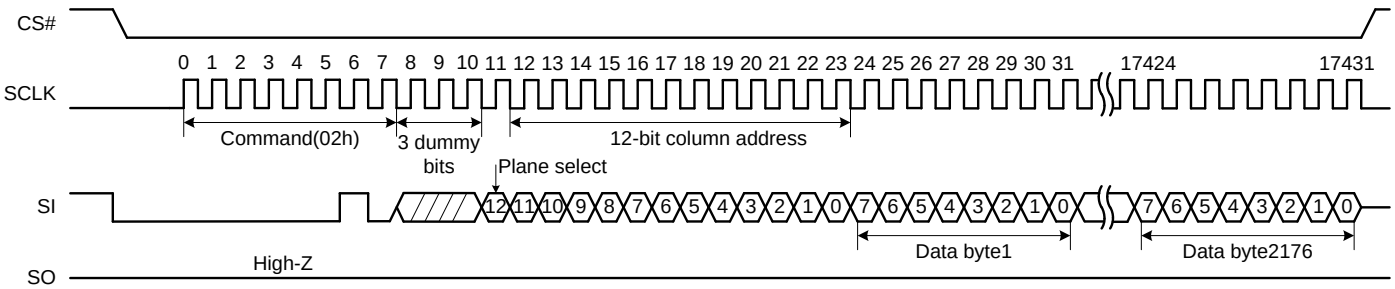


Figure 17: **Program Load (02h) Command Timing**

9.5.3. Program Execute (10h)

The Program Execute 10h command sequence is as follows:

Drive CS# pin low --> Shift in command byte --> Shift in 24 bits of page/block address --> Drive CS# pin high.

This command transfers data from cache register to the specified address in the main array. While the program operation is in progress, the device is busy for a duration of tPROG. The host can poll the status register to detect the completion of this operation, after which an upcoming series of data can be loaded into the device using Program Load command.

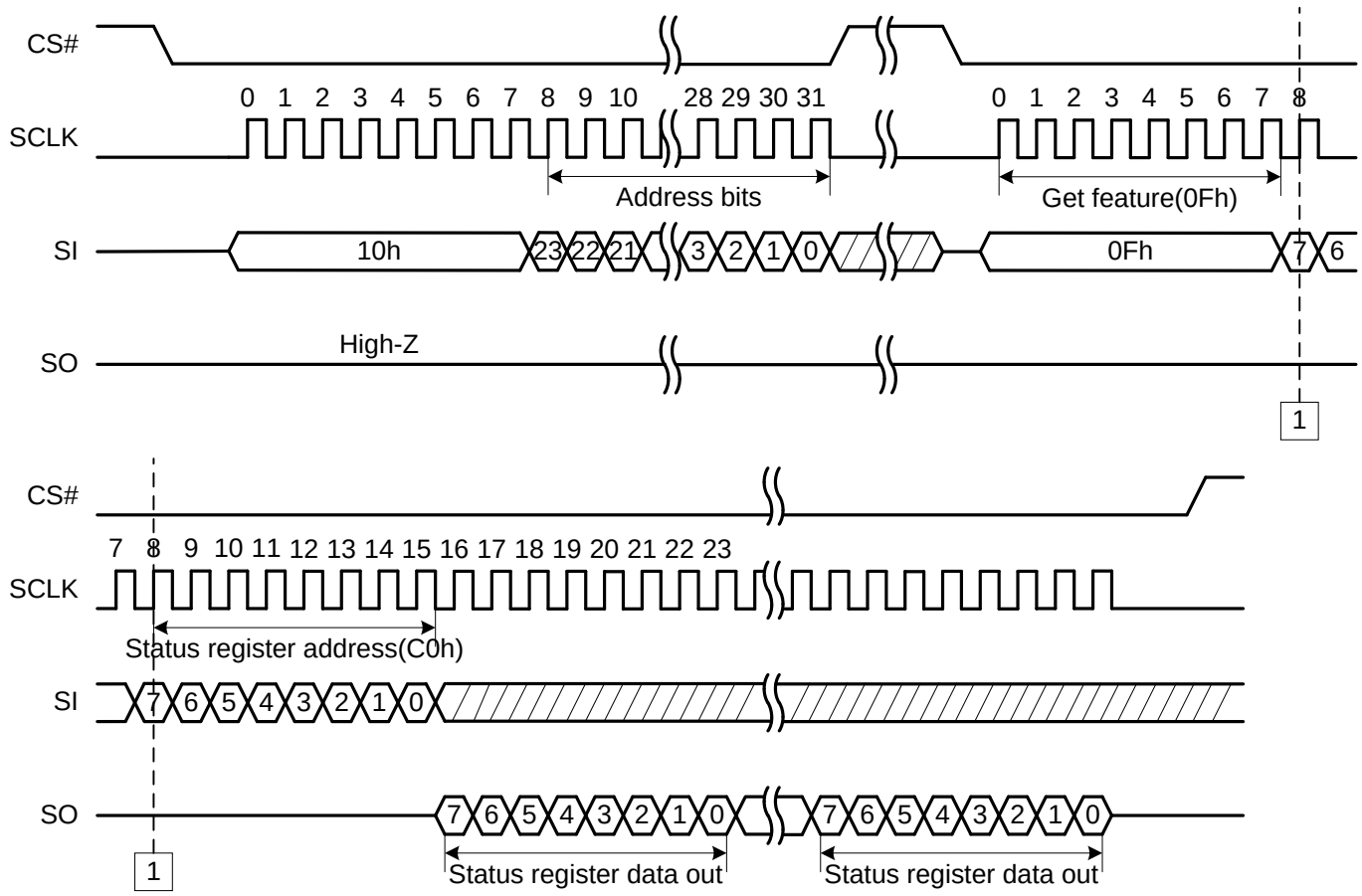


Figure 18: **Program Execute (10h) Command Timing**

9.5.4. Program Load Random Data x1 (84h)

The Random Data Program x1 command 84h programs or replaces data in the cache register. The command sequence is as follows:

Table 17: **Random Data Program Command Sequence**

Step	Opcode	Command	Description
1	06h	Write Enable	Enable the device for program operation.
2	84h	Program Load Random Data	Shift data into the cache register.
3	10h	Program Execute	Transfer data from cache register to main array.
4	0Fh	Get Features	Poll the device for status register.

The 84h command is similar to the Program Load x1 command 02h with the difference being that the 02h command resets the cache register to all FFs before shifting in data, while 84h only updates the data bytes specifically specified by the command without affecting the rest of the cache register. If the input random data occupy multiple segments of sequential address space, then each segment of data should be input by a specific 84h command with its corresponding column address.

After data is loaded, Program Execute command 10h can be used to initiate the programming process.

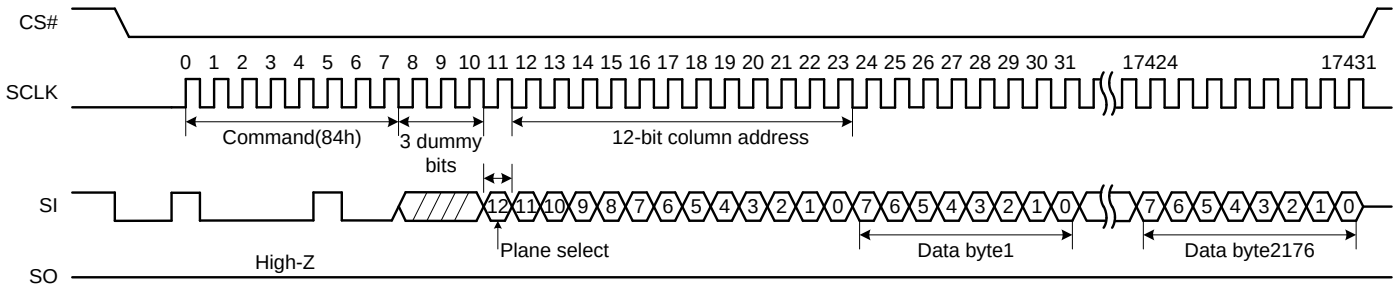


Figure 19: **Program Load Random Data (84h) Command Timing**

9.5.5. Program Load x4 (32h) and Program Load Random Data x4 (34h)

These commands are similar to 02h and 84h commands except that data is input from IO0 through IO3.

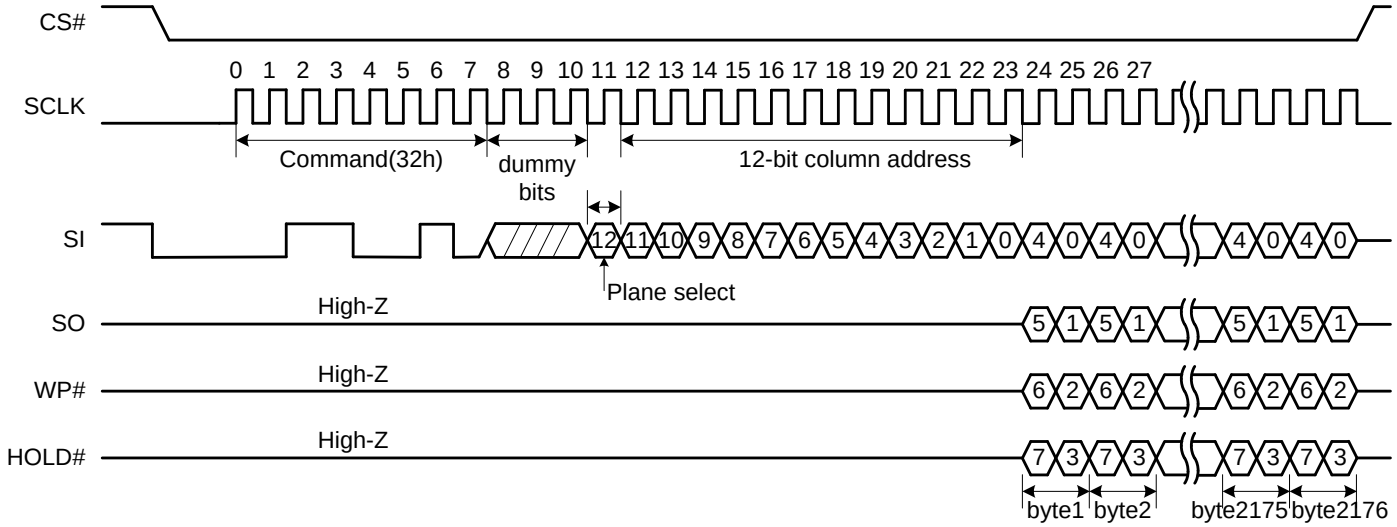


Figure 20: **Program Load x4 (32h) Command Timing**

Notes:

1. The number of dummy bits are dependent on device densities.

9.5.6. Internal Data Move

The Internal Data Move command sequence programs or replaces a data page with expected data. The command sequence is shown below.

Table 18: **Internal Data Move Command Sequence**

Step	Opcode	Command	Description
1	13h	Page Read	Transfer data from main array to cache register.
2	06h	Write Enable	Enable the device for program operation.
3	84h	Program Load Random Data	Shift data into the cache register.
4	10h	Program Execute	Transfer data from cache register to main array.
5	0Fh	Get Features	Poll the device for status register.

If the input random data occupy multiple segments of sequential address space, then each segment of data should be input by a specific 84h command with its corresponding column address.

9.6. Block Erase (D8h) Operations

A Block Erase command D8h changes a specified block of data to all FFs. Before an Erase operation, the WEL bit must be set to enable the device, otherwise the erase command is ignored.

A D8h command erases one block at a time. The command sequence is as follows.

Table 19: **Internal Data Move Command Sequence**

Step	Opcode	Command	Description
1	06h	Write Enable	Enable the device for erase operation.
2	D8h	Block Erase	Perform erase operation on specified block.
3	0Fh	Get Features	Poll the device for status register.

The D8h Block Erase command requires 24 bits of address, which includes dummy bits followed by the block address. After D8h command is issued, the device performs the erase operation and will be busy for a duration of tERS. The Get Features 0Fh command is used to poll for the completion of the operation.

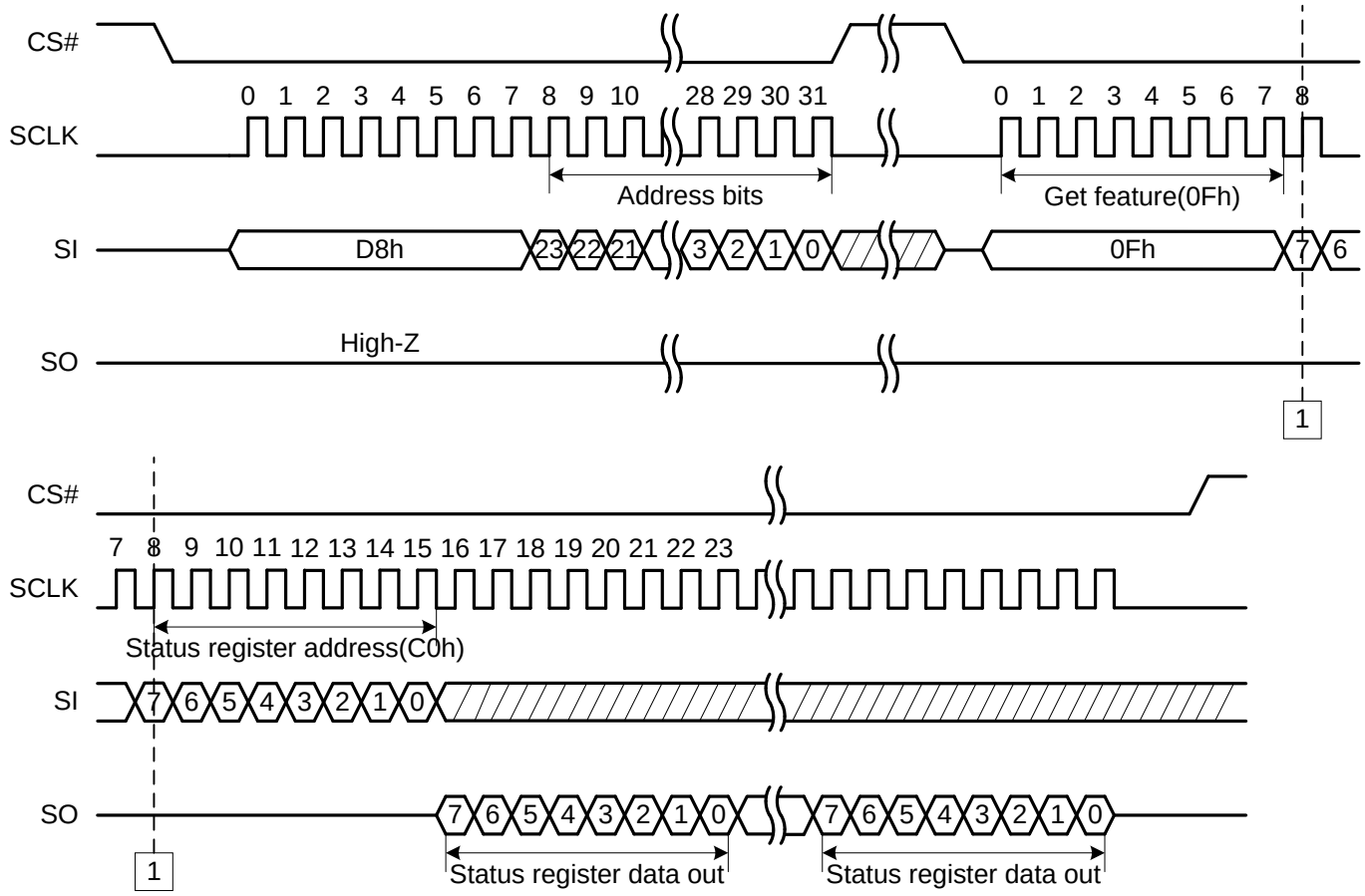


Figure 21: **Block Erase (D8h) Command Timing**

9.7. Feature Operations

9.7.1. Get Features (0Fh)

The Get Features command 0Fh reads the data value of a feature register. The command needs a 1-byte feature address to specify which register to read.

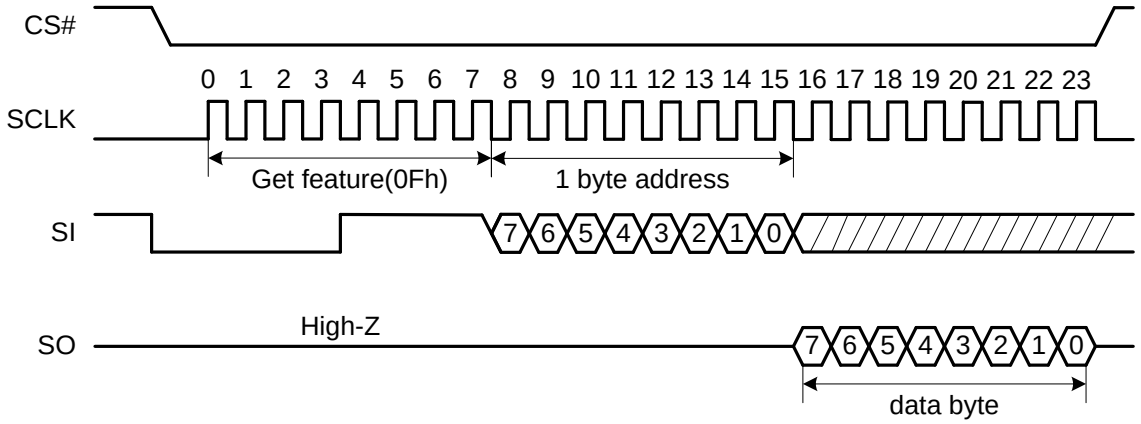


Figure 22: **Get Features (0Fh) Command Timing**

9.7.2. Set Features (1Fh)

The Set Features command 1Fh writes data value into a feature register. The command needs a 1-byte feature address to specify which register to write.

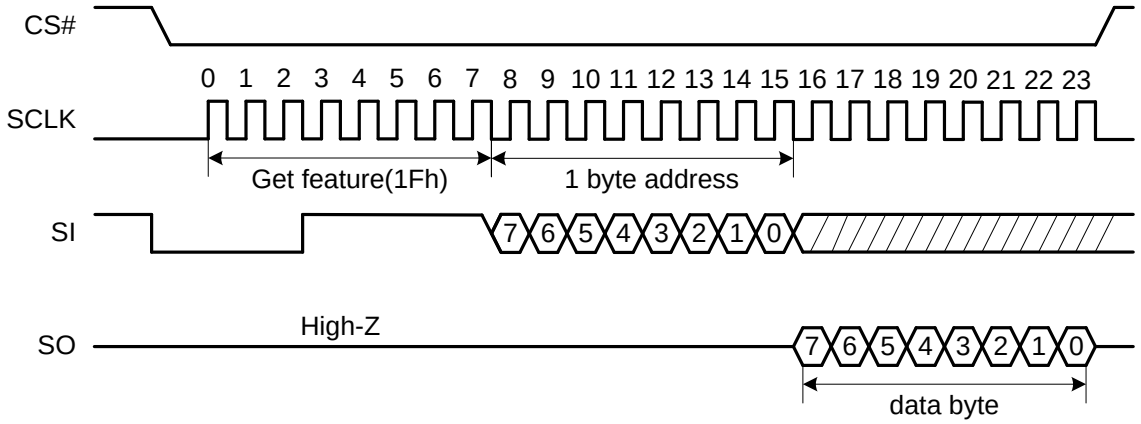


Figure 23: **Set Features (1Fh) Command Timing**

9.8. Protection

9.8.1. Protection Command (2Ch)

Permanent Block Lock Protection is a mechanism that permanently and irreversibly protects a maximum of 48 blocks of data per die. For more details, see *Section 8.4 Permanent Block Lock Protection*.

The protection is performed using the Protect command; one such command takes effect on a specific group (four blocks). Prior to this command, the Write Enable command must be used to set the WEL bit, otherwise the Protect command is ignored by the device.

When permanent lock is disabled, the Protect command is ignored by the device.

The Protection command sequence is as follows:

Table 20: **Protect (2Ch) Command Sequence**

Step	Opcode	Command	Description
1	06h	Write Enable	Enable the device for protect operation.
2	2Ch	Permanent Block Lock Protection	Use with 24-bit address.
3	0Fh	Get Features	After a duration of tPROG, use 0Fh command with feature address C0h to detect the P_Fail bit.

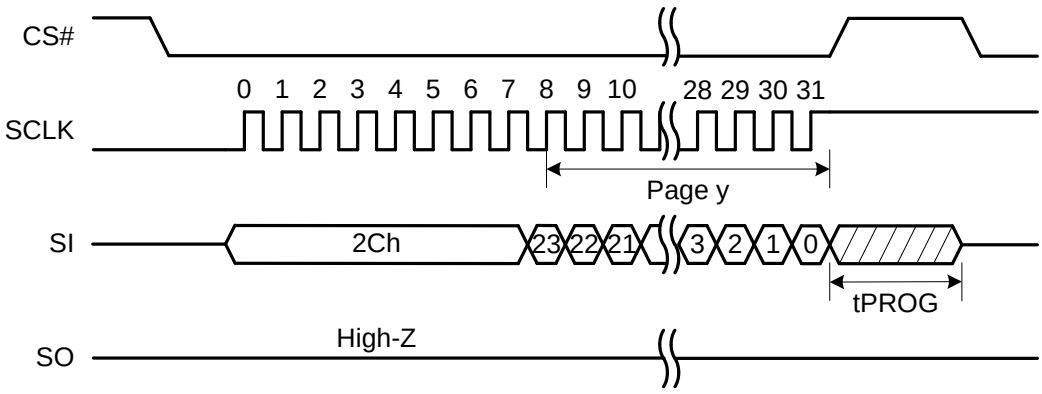


Figure 24: **Protect (2Ch) Command Timing**

The Protection command includes a command byte and 24 bits of address. For a 2Gbit die, the address has 7 dummy bits and 17 bits of page/block address. Row address bits 11 through 8 (henceforth noted as Y) determine which block group to protect:

Y = 0000: Group 0 (Blocks 0, 1, 2, 3) is protected.

Y = 0001: Group 1 (Blocks 4, 5, 6, 7) is protected.

.....

Y = 1011: Group 11 (Blocks 44, 45, 46, 47) is protected.

After ther command is input, it takes a duration of tPROG for the protection to take effect. In case of a Protection failure, the P_FAIL and WEL bits are both 1 (status register = 0Ch); upon successful completion of Protection operation, the status register is 00h.

It should be noted that there is no internal register recording the Protect status of the blocks or groups; it is up to the host controller to create and maintain a table of blocks under permanent protection.

9.8.2. Permanent Block Lock Protection Disable Mode

The host can disable the Permanent Block Lock Protection and instruct the device to ignore the Protection command. The command sequence is as follows.

Table 21: **Permanent Block Lock Protection Disable Command Sequence**

Step	Opcode	Command	Description
1	1Fh	Set Feature	Use with feature address = B0h and data = C2h.
2	06h	Write Enable	Enable the device for protect operation.
3	10h	Program Execute	Execute program operation with block/page address as 0.
4	0Fh	Get Features	After a duration of tPROG, use 0Fh command with feature address C0h to detect the P_Fail bit.

9.9. OTP Operations

9.9.1. Enable OTP Access

Prior to OTP read and write access operations, OTP access should be enabled by a specific command sequence as follows:

Table 22: **Enable OTP Mode Command Sequence**

Step	Opcode	Command	Description
1	1Fh	Set Feature	Use with feature address = B0h and data = 50h (ECC enabled) or 40h(ECC disabled).

After the die is in OTP mode, all upcoming page read and page program commands will be executed on OTP area.

9.9.2. OTP Program

Once the device is in OTP mode, use the following command sequence to Program one or more pages to OTP area:

Table 23: **Program OTP Area Command Sequence**

Step	Opcode	Command	Description
1	06h	Write Enable	Enable the device for program operation.
2	10h	Program Execute	Execute program operation with the row address of the OTP page.
3	0Fh	Get Features	Use 0Fh command with feature address C0h to detect the OIP bit.
4	0Fh	Get Features	Use 0Fh command with feature address C0h to poll for the P_FAIL bit.

9.9.3. OTP Read

Once the device is in OTP mode, use the following command sequence to Read one or more pages from OTP area:

Table 24: **Read OTP Area Command Sequence**

Step	Opcode	Command	Description
1	13h	Page Read	Use this command with the address of the target OTP page.
2	0Fh	Get Features	Use 0Fh command with feature address C0h to detect the OIP bit.
3	03h	Read From Cache	Output read data from the cache register.

9.9.4. OTP Protection and Program Prevention

OTP pages can be protected from further programming operations using the following command sequence:

Table 25: **OTP Protection and Program Prevention Command Sequence**

Step	Opcode	Command	Description
1	1Fh	Set Feature	Use with feature address = B0h and data C0h, in which CFG[2:0] is 110b.
2	06h	Write Enable	Enable the device for upcoming operation.
3	10h	Program Execute	Execute program operation with row address 00h.
4	0Fh	Get Features	Use 0Fh command with feature address C0h to poll for OIP and P_FAIL bits.

9.9.5. OTP Configuration States

The host can use the following command sequence to check various internal status of the device, including SPI NOR read protocol enable, OTP data protect, Permanent Block Lock Protection:

Table 26: **Check Internal Status Command Sequence**

Step	Opcode	Command	Description
1	1Fh	Set Feature	Use with feature address = B0h and data specified as follows: Data = C0h: OTP data protect bit. Data = 82h: NOR read protocol enable bit. Data = C2h: Permanent Block Lock disable bit.
2	13h	Page Read	Use this command with address 0.
3	0Fh	Get Features	Use 0Fh command with feature address C0h to detect the OIP bit.
4	03h	Read From Cache	Use address 0 to output read data from the cache register: If read data are all 0s, then the mode is enabled. If read data are all 1s, then the mode is disabled.

Besides, bits CFG[2:0] can be read by Get Feature 0Fh command with feature address B0h.

9.9.6. Exit OTP

Use the following command sequence to exit from OTP mode and bring the device back to normal main array operation mode:

Table 27: **Exit OTP Mode Command Sequence (1Fh)**

Step	Opcode	Command	Description
1	1Fh	Set Feature	Use with feature address = B0h and data CFG[2:0] = 000b.

Alternatively, issuing the FFh Reset command can also bring the device back to normal operation mode:

Table 28: **Exit OTP Mode Command Sequence (FFh)**

Step	Opcode	Command	Description
1	FFh	Reset	Reset command.

9.10. ECC Operations

The ECC capability is enabled by default after power up. The following command sequence can be used to enable or disable ECC after power up:

Table 29: **Enable / Disable ECC Command Sequence**

Step	Opcode	Command	Description
1	1Fh	Set Feature	Use with feature address = B0h and and data specified as follows: Data bit 4 = 1: ECC is enabled. Data bit 4 = 0: ECC is disabled.

9.11. SPI NOR Read Configuration

The SPI NOR Read Protocol is enabled using the following command sequence:

Table 30: **SPI NOR Read Protocol Command Sequence**

Step	Opcode	Command	Description
1	1Fh	Set Feature	Feature address = B0h, data bits CFG[2:0] = 101b. (Access to SPI NOR read protocol enable mode)
2	06h	Write Enable	Enable Program operation.
3	10h	Program Execute	Block / page address should be all 0s.
4	0Fh	Get Feature	Feature address = C0h, check OIP for operation completion, verify P_FAIL bit for operation status.
5	1Fh	Set Feature	Feature address = B0h, data bits CFG[2:0] = 000b, which returns the device to normal operation mode.
6	0Fh	Get Feature	Feature address = B0h, verify CFG[2:0] bits.

The SPI NOR Read Protocol setting is nonvolatile and will survive a power-cycling process.

9.11.1. Read From Cache (03h)

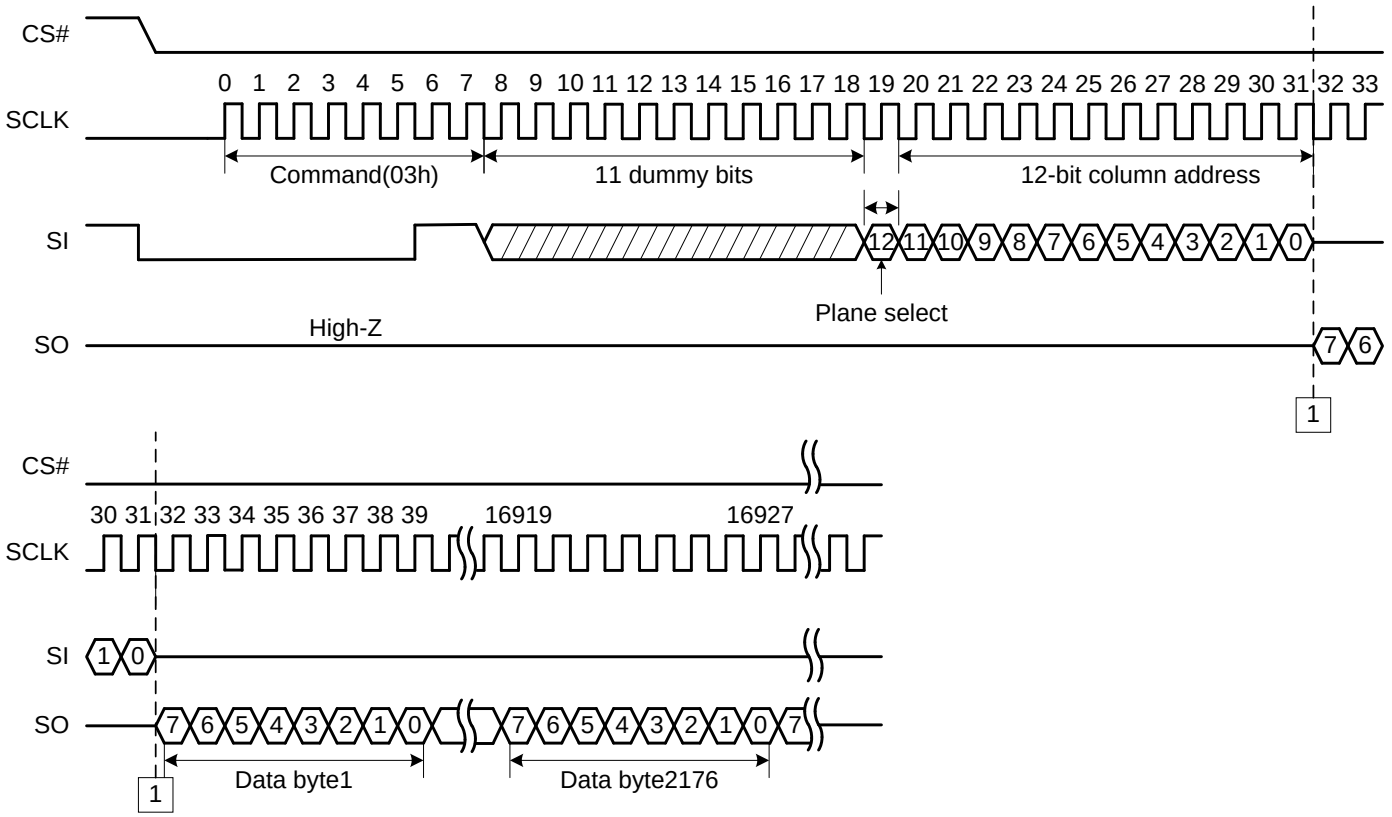


Figure 25: **Read From Cache (03h)**

Notes:

1. This operation is compatible with conventional SPI NOR Flash devices.

9.11.2. Fast Read From Cache (0Bh)

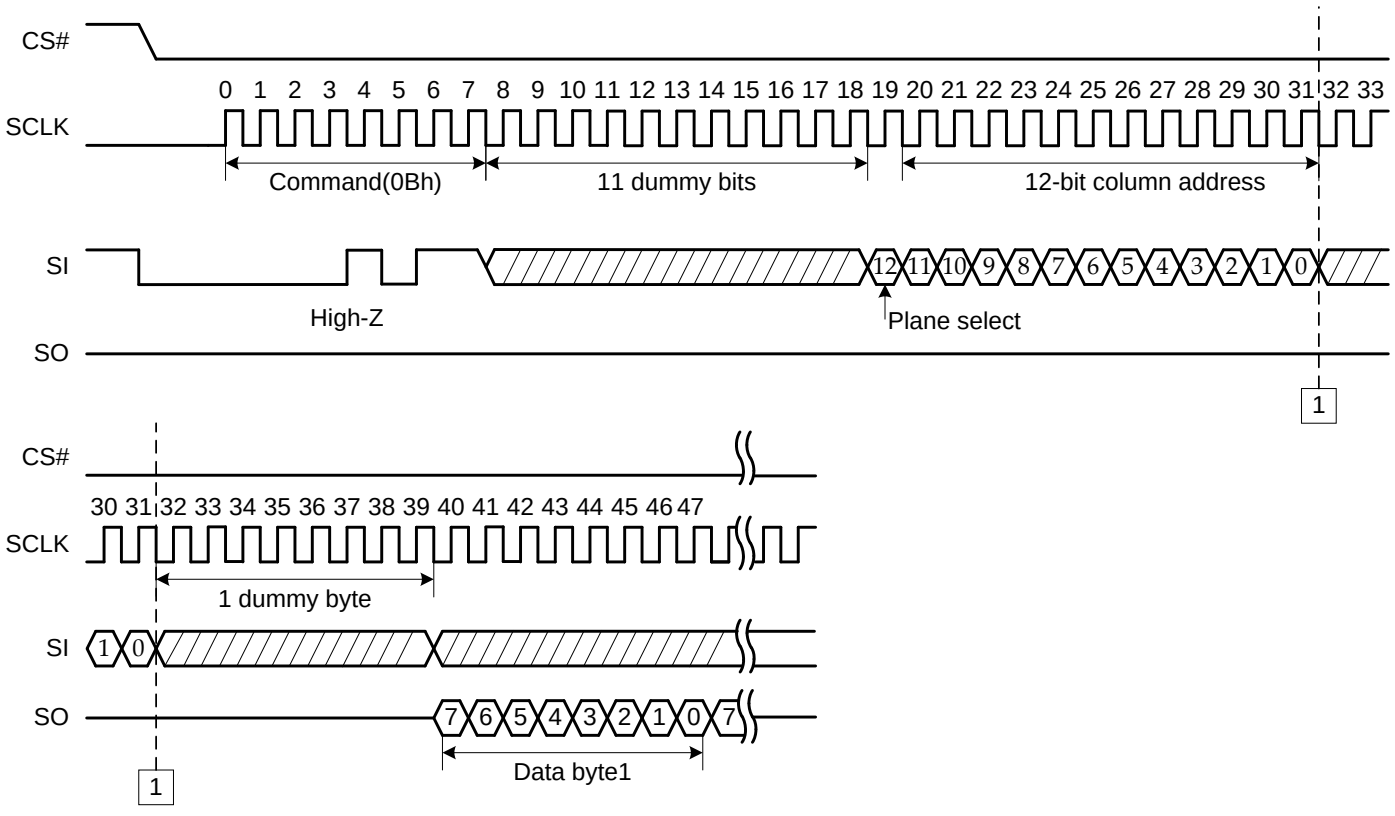


Figure 26: **Fast Read From Cache (0Bh)**

Notes:

1. This operation is compatible with conventional SPI NOR Flash devices.

10. Error Management

10.1. Bad Block

An invalid block or bad block is one that contains at least one page with more bad bits beyond the correction capability of the minimum required ECC. Bad blocks may develop during the device lifetime, but the total number of valid blocks will not fall below N_{VB} during the endurance life of the device.

Inside the NAND Flash device, all blocks are isolated from each other by internal circuitry, so the presence of bad blocks does not affect the operation of the rest of the memory array. With appropriate bad block management and error correction algorithms, NAND Flash devices with bad blocks can provide reliable data storage.

10.2. Factory Bad Blocks

NAND Flash devices are shipped from factory with all locations inside valid blocks erased to FFh. The device may contain invalid blocks upon delivery. These bad blocks are identified before shipping by attempting to program bad block marks at every location in the first page of each bad block, and the first spare area location in a bad block is guaranteed to contain the bad block mark.

Before doing any erase or program operations, the host should check for non-FFh data at the first spare area location on the first page of all blocks in the device and create a bad-block table accordingly, so the bad blocks can be mapped around.

Factory tests are conducted in such a way that marginal bad blocks can be detected and marked; it may be impossible to recover the initial bad block markings after the blocks are programmed or erased by the user.

See the table below for details.

Table 31: **Error Management Details**

Description	Requirement
Minimum number of valid blocks (N_{VB})	2008
Total available blocks per die	2048
First spare area location in the first page of each block	Byte 2048
Bad-block mark	00h
Minimum required ECC	8-bit ECC per sector (544 bytes) of data
Minimum ECC with internal ECC enabled	8-bit ECC per 512 bytes (user data) + 8 bytes (spare) + 16 bytes (ECC data)

11. Power Considerations

11.1. Data Protection During Power Transitions

To ensure proper operation, the device should be deselected during power-up and power-down processes, viz. CS# should follow V_{CC} voltage until V_{CC} reaches $V_{CC,min}$ at power-up or V_{SS} at power-down. During power transitions, an internal circuitry holds internal logic at reset state, thus protecting the device from unexpected data corruptions.

Internal circuitry of the device monitors input V_{CC} voltage; after V_{CC} reaches V_{WI}, the host must wait for a duration of at least 250μs before sending in a Reset command FFh. After FFh command is sent, the host must wait for another 1.25ms before sending in any other command. The Get Feature command should be used to poll the status register for OIP bit before the first access.

For power-cycling tests, the system should wait for V_{CC} to drop down to 0V before initiating the next power-up

sequence.

11.2. V_{CC} Decoupling

In hardware design, a decoupling capacitor of 100nF typical should be placed next to V_{CC} pins to stabilize the power supply.

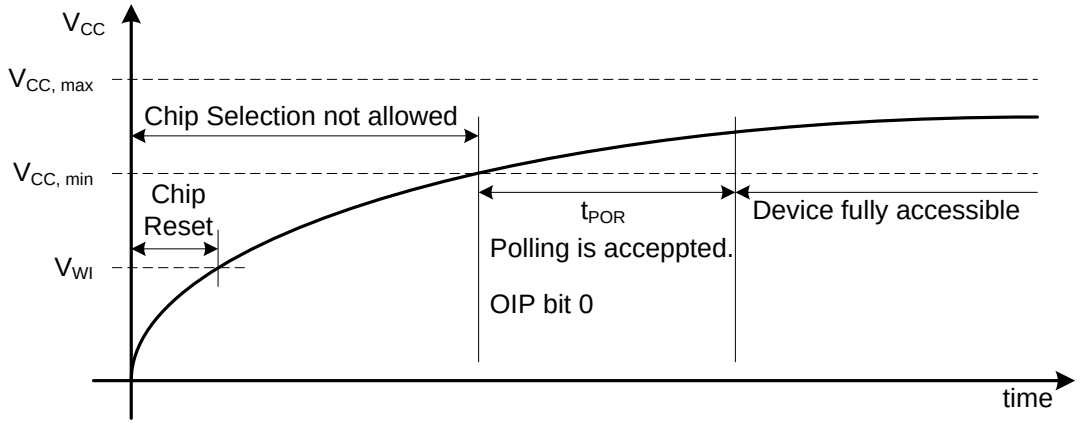


Figure 27: **Device SPI Power-Up**

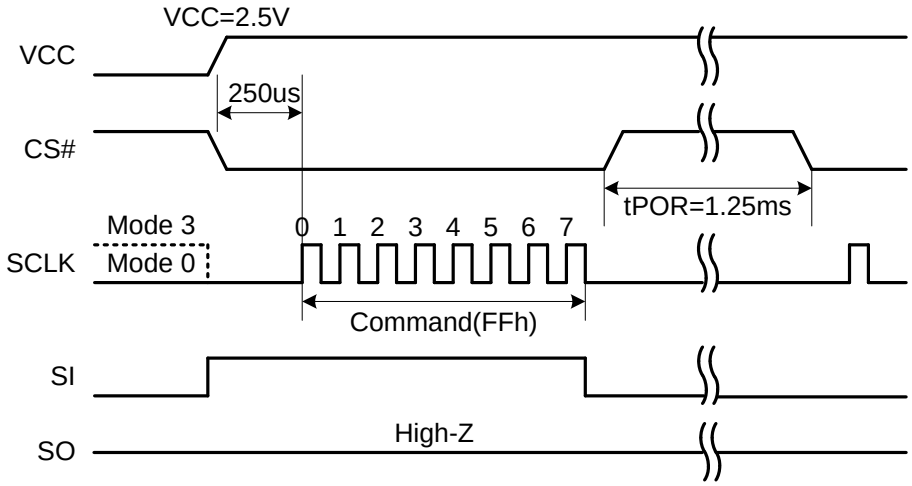


Figure 28: **Device SPI Power-Up Timing**

11.3. Alternative SPI Power-Up Sequence

An alternative SPI NAND sequence does not require an explicit Reset command FFh upon device power-up. In this sequence, after V_{CC} reaches V_{WI}, the device automatically starts the initialization process, and by default the first page is automatically loaded into the cache register.

During the initialization process, the host can wait for 1.25ms after V_{CC} reaches $V_{CC,min}$, or use the Get Feature command to poll the OPI bit before the first access.

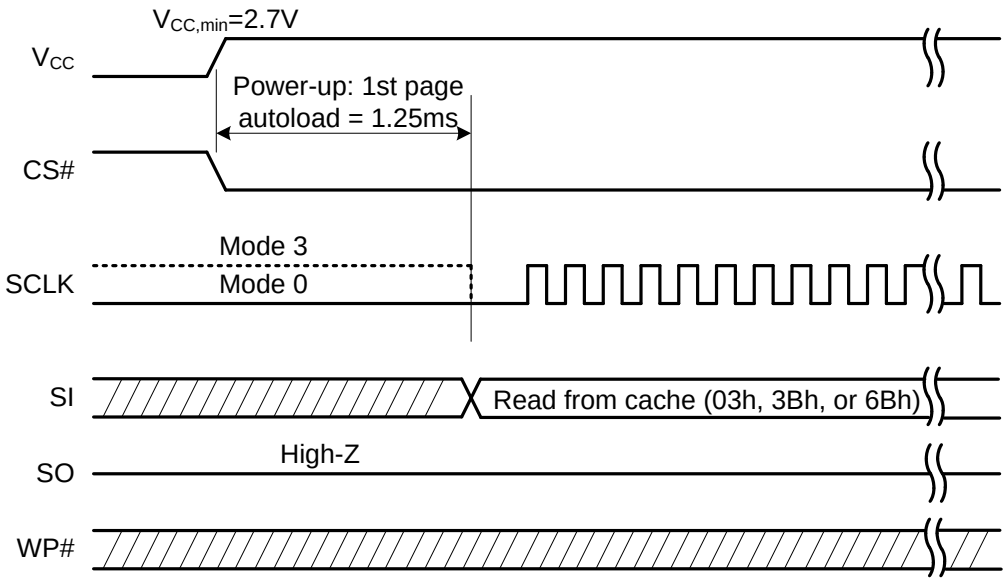


Figure 29: **Alternative SPI Power-Up Sequence Timing**

12. Electrical Characteristics

12.1. Absolute Maximum Ratings

Exposure to stresses greater than those in the table below may lead to permanent damage in the device. They are stress ratings, and device functions are not guaranteed at these or any other conditions with values above the ones below.

Table 32: **Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit
Supply voltage (SPI)	VCC	–0.6	4.6	V
I/O voltage	VCC	–0.6	4.6	V
Operating temperature (ambient)	T_A	–40	85	°C
Storage temperature	T_S	–65	85	°C

Notes:

1. Voltages in this table are with respect to V_{SS} ground.
2. Undershoot to -2.0V or overshoot to V_{CC_MAX}+2.0V may be acceptable if they are nonperiodic, infrequent and with durations of less than 20ns.

12.2. Operating Conditions

Table 33: **Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VCC	2.7	3.3	3.6	V
Ambient operating temperature (industrial)	T_A	–40	25	85	°C

12.3. AC Measurement Conditions

Table 34: **AC Measurement Conditions**

Parameter	Symbol	Min	Max	Unit
Load Capacitance	C_L	30/10		pF
Input rise and fall time	–	–	5	ns
Input rise and fall time (>100 MHz)	–	–	1.5	ns

Input pulse voltage[1]	–	0.2 VCC	0.8 VCC	V
Input timing reference voltages	–	0.3 VCC	0.7 VCC	V
Output timing reference voltages	–	VCC/2		V

Notes:

1. The Min/Max specifications of "Input Pulse Voltage" is for dual / quad operations.

Figure 30: **AC Measurement IO Waveform**

12.4. Input/Output Capacitance

Table 35: **Capacitance**

Description	Symbol	Test Conditions	Typ	Max	Unit
Input/output capacitance (IO0, IO1, IO2, IO3)	C_{IN}	V_{OUT} = 0V	–	9	pF
Input capacitance (other pins)	C_{IN}	V_{IN} = 0V	–	9	pF

Notes:

1. These parameters are not 100% tested.
2. These parameters take into consideration both silicon and the device package.

12.5. DC Characteristics

Table 36: **DC Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage	V_{IH}	–	0.7 × VCC	–	VCC + 0.4	V
Input low voltage	V_{IL}	–	–0.5	–	0.3 × VCC	V
Output high voltage	V_{OH}	I_{OH} = –100µA	VCC - 0.2	–	–	V
Output low voltage	V_{OL}	I_{OL} = 1.6mA	–	–	0.4	V
Input leakage current	I_{LI}	–	–	–	±10	µA
Output leakage current	I_{LO}	–	–	–	±10	µA
Page read current	I_{CC3}	–	–	25	35	mA
Program current	I_{CC4}	–	–	25	25	mA
Erase current	I_{CC5}	–	–	25	25	mA
Standby current	I_{CC1}	CE# = VCC; VIN = VSS or VCC	–	15	50	µA

Notes:

1. This table gives typical values at T_A=25°C.
2. These parameters are verified during device characterization.
3. These parameters are not 100% tested.

12.6. AC Characteristics

Table 37: **AC Characteristics**

Parameter	Symbol	Min	Max	Unit
Clock frequency[1, 2]	f_C	–	133	MHz
Clock LOW time	t_{WL}	3.375	–	ns
Clock HIGH time	t_{WH}	3.375	–	ns
Clock LOW time (SPI NOR read 03h mode at 20 MHz)	t_{WL}	22.5	–	ns
Clock HIGH time (SPI NOR read 03h mode at 20 MHz)	t_{WH}	22.5	–	ns
Clock rise time	t_{CRT}	1.3	–	V/ns
Clock fall time	t_{CFT}	1.3		V/ns
Command deselect time	t_{CS}	30	–	ns
Chip select# active setup/hold time relative to SCK	t_{CSS}/t_{CSH}	3.375	–	ns
Chip select# non-active setup/hold time relative to SCK	t_{CSH}	2.5	–	ns
Output disable time	t_{DIS}	–	6	ns
Data input setup time	t_{SUDAT}	2.5	–	ns
Data input hold time	t_{HDDAT}	1.75	–	ns
Clock LOW to output valid (30pF)	t_V	–	6	ns
Clock LOW to output valid (10pF)	t_V	–	5	ns
Clock LOW to output valid (similar to SPI NOR 20 MHz read 30pF)	t_V	–	30	ns
Clock LOW to output valid (similar to SPI NOR 20 MHz read 10pF)	tV	–	28	ns
Output hold time (30pF)	t_{HO}	2	–	ns
Output hold time (10pF)	t_{HO}	1.5	–	ns
Output hold time (SPI NOR similar to 20 MHz read 30pF)	t_{HO}	0	–	ns
Output hold time (SPI NOR similar to 20 MHz read 10pF)	t_{HO}	0	–	ns
WP# hold time	t_{WPH}	100	–	ns
WP# setup time	t_{WPS}	20	–	ns

Notes:

1. Read from Cache Dual IO (BBh) and Quad IO (EBh) commands support clock frequency up to 108MHz.
2. With SPI NOR read protocol enabled, Read from Cache 03h command support clock frequency up to 20MHz, while Read from Cache 0Bh command support clock frequency up to 133MHz.

12.7. Program, Read and Erase Characteristics

Table 38: **Program / Read / Erase Specifications**

Parameter	Symbol	Typ	Max	Unit
BLOCK ERASE operation time (128KB)	t_{ERS}	2	10	ms
PROGRAM PAGE operation time (ECC disabled)	t_{PROG}	200	600	µs
PROGRAM PAGE operation time (ECC enabled)		220	600	
Page read time (ECC disabled)	t_{RD}	–	25	µs
Page read time (ECC enabled)		46	70	
Data transfer time from data register to cache register (internal ECC disabled)	t_{RCBSY}	–	5	µs
Data transfer time from data register to cache register (internal ECC enabled)		40	50	µs
Power-on reset time (device initialization) from VCC MIN	t_{POR}	–	1.25	ms
Write inhibit voltage	V_{WI}	–	2.5	V
Reset time for READ, PROGRAM, and ERASE operations	$t_{RST}1$	–	30/35/525	µs

(internal ECC disabled)				
Reset time for READ, PROGRAM, and ERASE operations (internal ECC enabled)		–	75/80/570	µs
Number of partial-page programming operations supported	NOP2	–	4	–

Notes:

1. For the first Reset command after device power-up, tRST is 1.25ms maximum. For stack die, the host should not send any commands during tRST.
2. Single partial-page programming operations should be used for the main user area and user meta data area I.
3. Within a single page, the device accepts a maximum of four partial-page program operations.

12.8. AC Timing Diagrams

12.8.1. WP# Timing

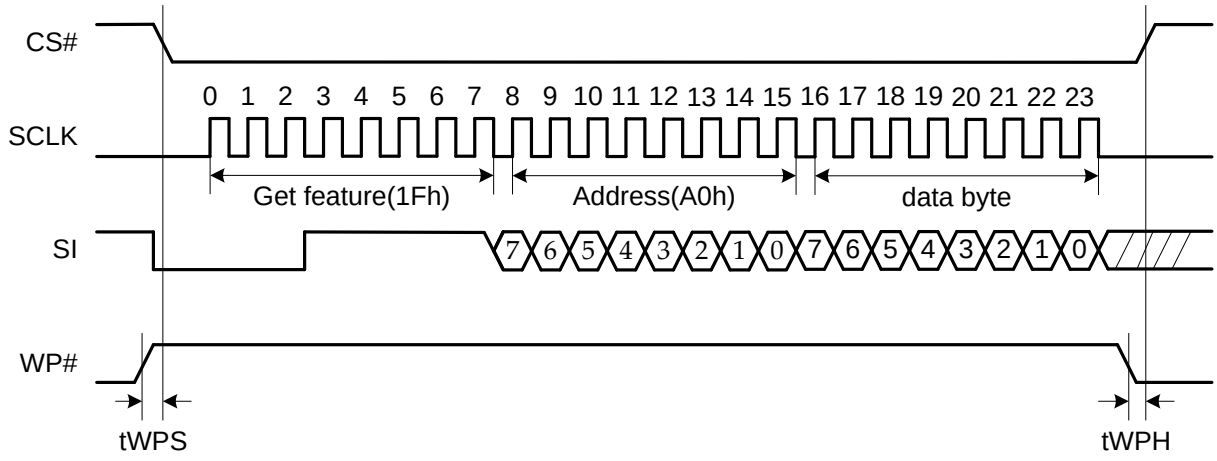


Figure 31: **WP# Timing**

12.8.2. Serial Input Timing

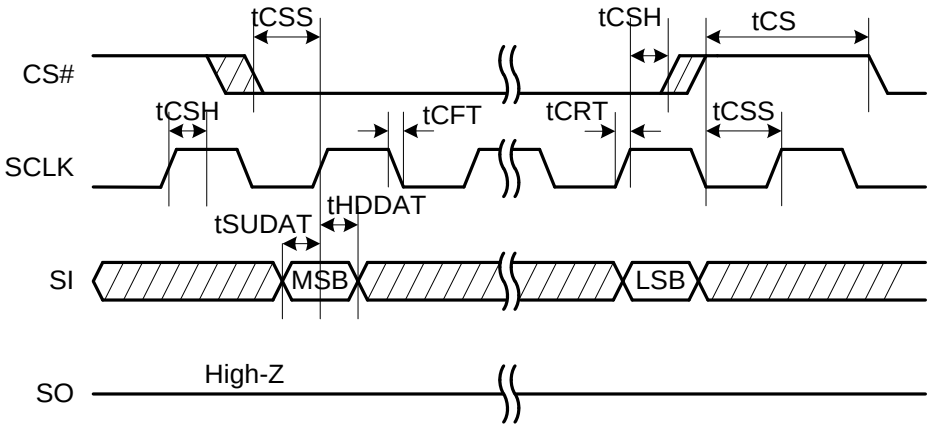


Figure 32: **Serial Input Timing**

12.8.3. Serial Output Timing

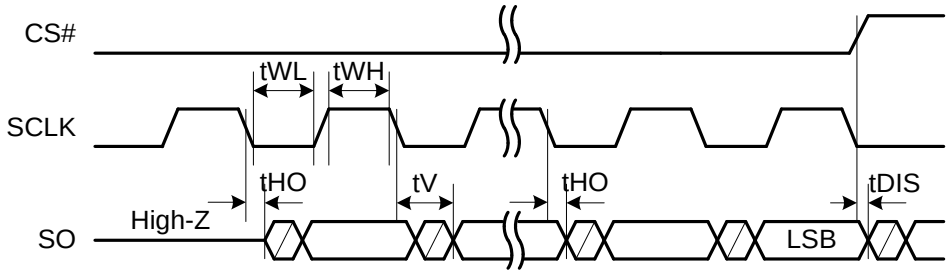


Figure 33: **Serial Output Timing**

13. Ordering Information

NM 5A 02G 01 A X X X X

Manufacturer
NM: NeuMem

Product Family
5A: SPI NAND Flash with internal ECC
5F: SPI NAND Flash without internal ECC

Density
01G: 1Gbit
02G: 2Gbit

Organization
01: x1
04: x4
08: x8

Product Version
A: Version A
B: Version B
C: Version C

Package Type
B: FBGA-24
D: DIP8 300mil
F: FBGA-63
P: SOP16 300mil
Q: WSON8 (6*5mm)
S: SOP8 208mil
U: USON8 (4*4mm, 0.45mm thickness)
W: Wafer
Y: WSON8 (8*6mm)
Z: TFBGA24 (6*4 Ball Array)

Temperature Range
C:Commercial (0°C to +70°C)
I: Industrial (-40°C to +85°C)
J: Industrial Plus (-40°C to +105°C)
A: Automotive (-40°C to +125°C)

Green Code
G: Pb Free & Halogen Free Green Package

Packing Type
T or no mark: Tube
Y: Tray
R: Tape & Reel

Figure 34: **Device Ordering Information**

14. Package Information

14.1. 16-pin SOP (300 mils body width)

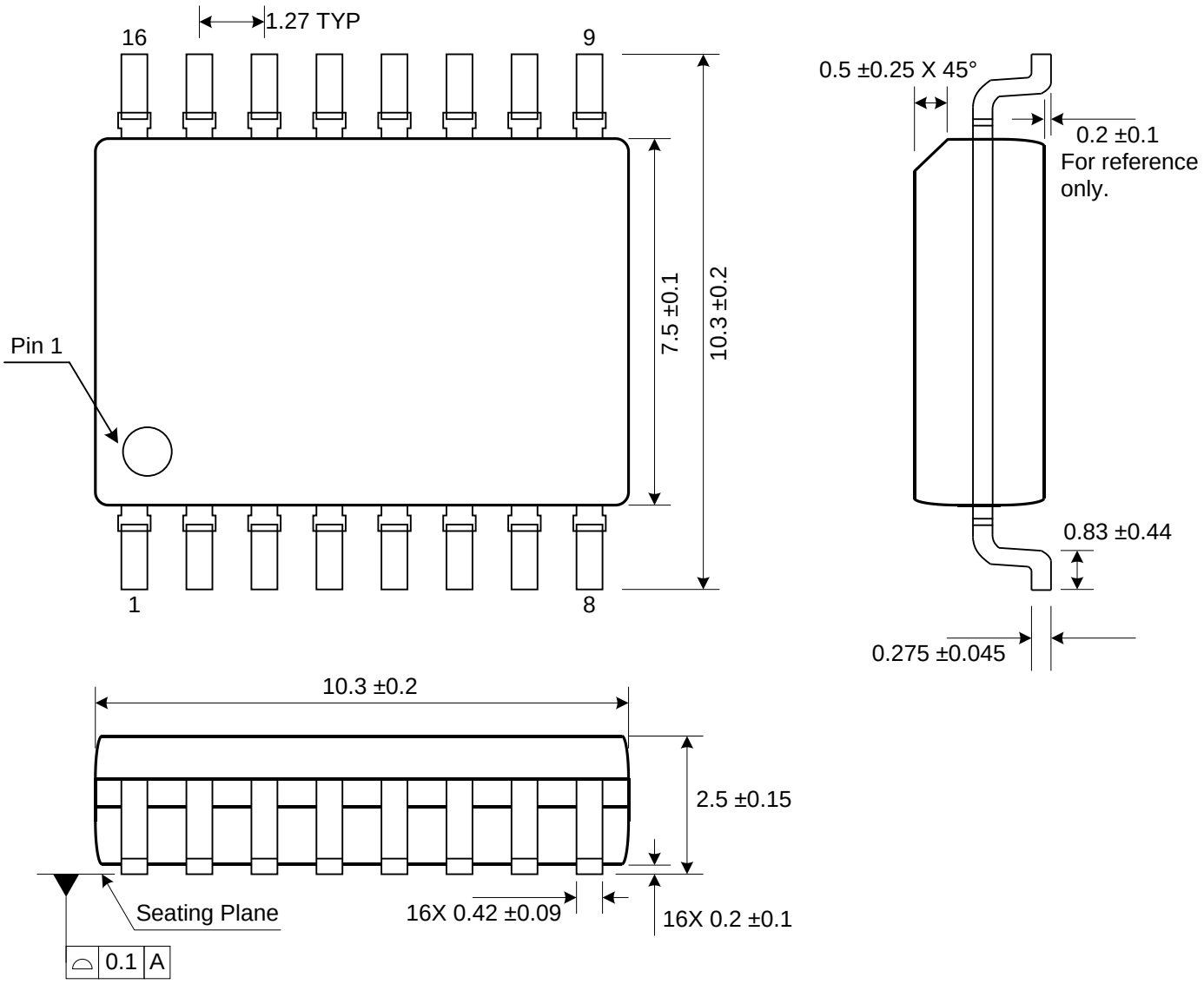


Figure 35: **16-pin SOP (300 mils body width) Package**

Notes:

1. All dimensions are in millimeters.

14.2. 8-pin U-PDFN (MLP8) 8mm x 6mm x 0.65mm

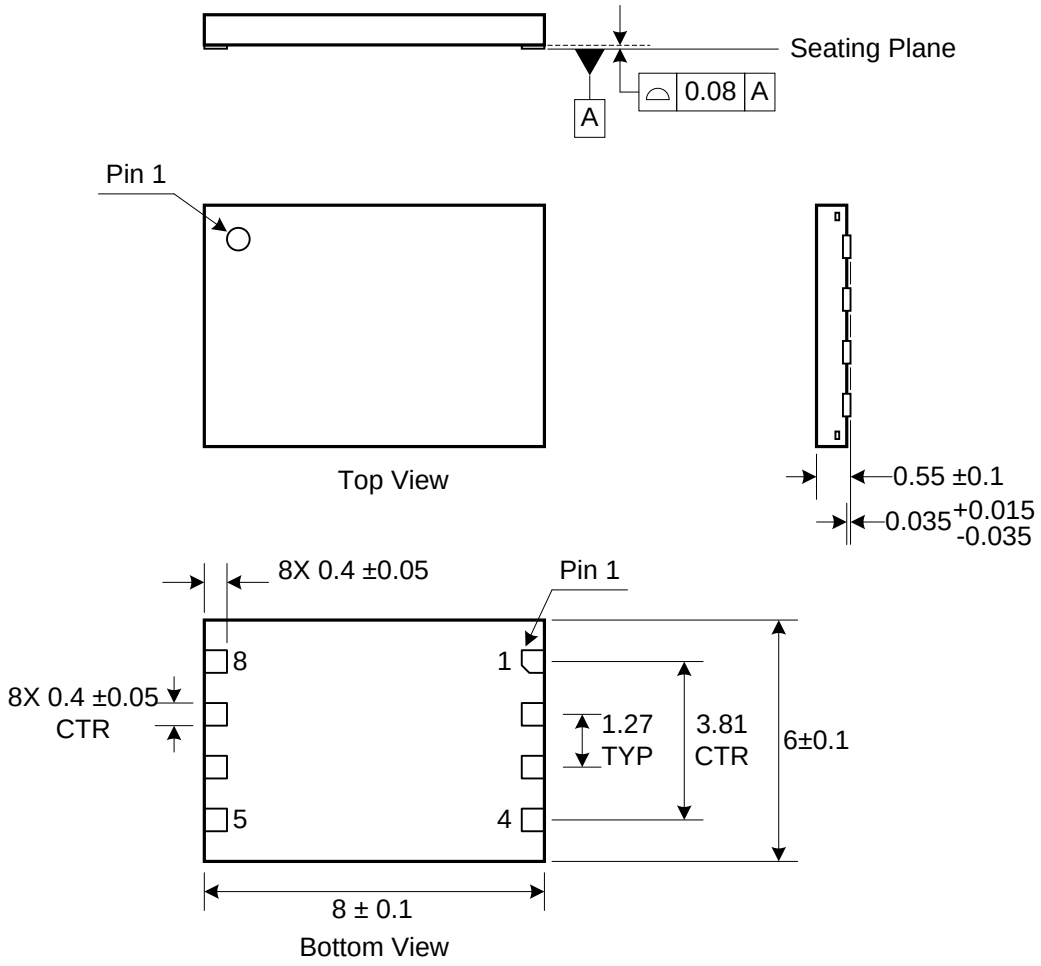


Figure 36: **8-pin U-PDFN (MLP8) 8mm x 6mm x 0.65mm Package**

Notes:

1. All dimensions are in millimeters.

14.3. 24-Pin T-PBGA (5 x 5 Ball Grid Array) 6mm x 8mm

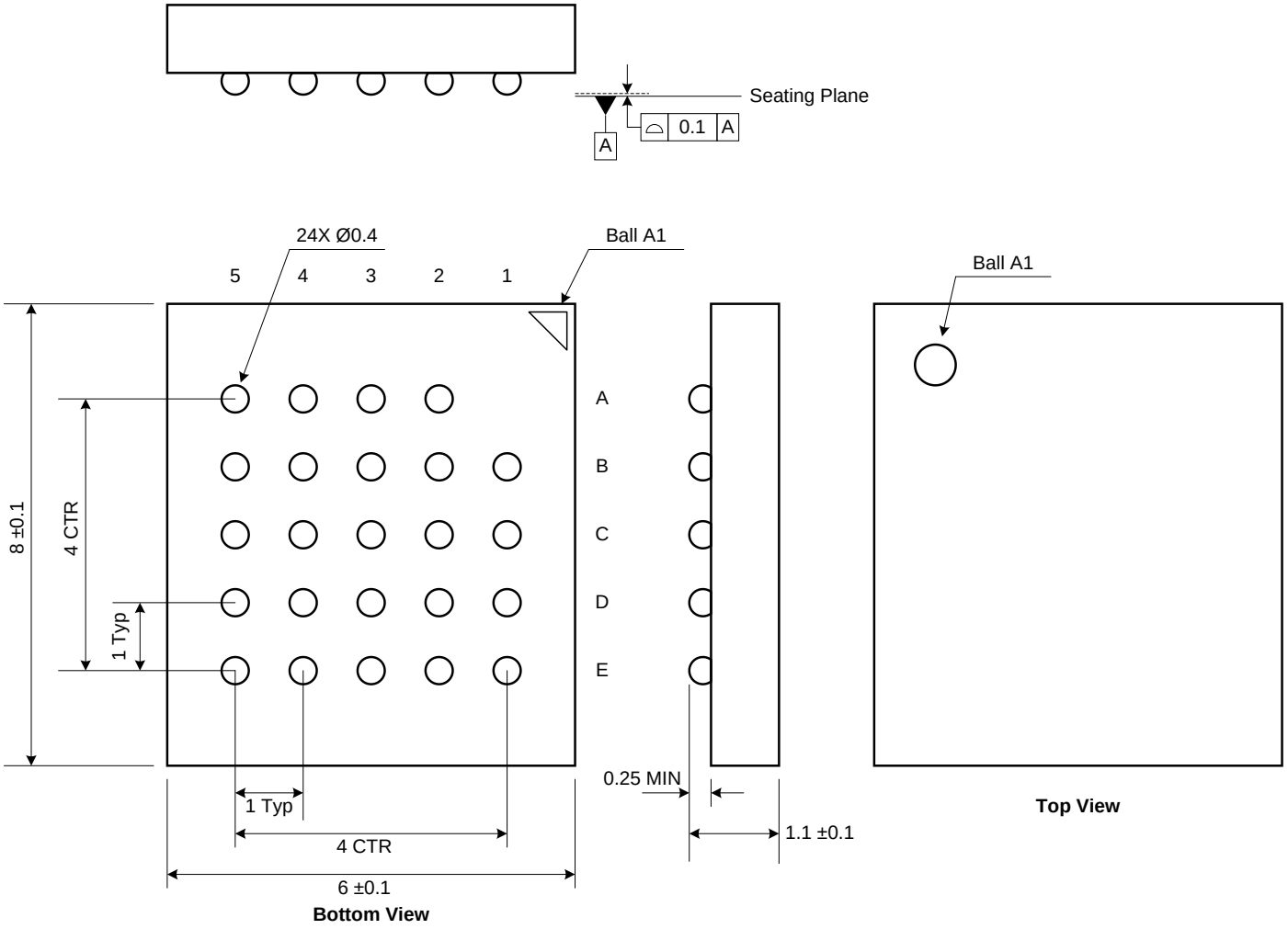


Figure 37: **DIP8(300mil) Package**

Notes:

1. All dimensions are in millimeters.
2. Dimensions apply to solder balls post-reflow on Ø0.35 SMD ball pads.

15. Revision History

The table below shows the revision history of this document.

Date	Version	Revision
Feb 04, 2021	v1.0	NeuMem initial release.

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