

N-Channel Enhancement Mode Power MOSFET

Features

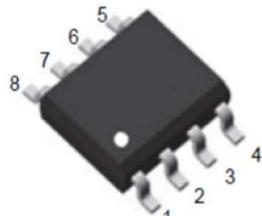
- $V_{DS} = 40V$, $I_D = 14 A$
- $R_{DS(ON)} < 10 m\Omega$ @ $V_{GS} = 10V$
- $R_{DS(ON)} < 17 m\Omega$ @ $V_{GS} = 4.5V$

General Features

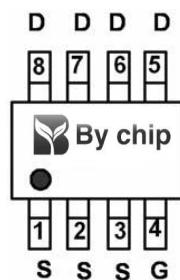
- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free and Green Available

100% UIS TESTED!

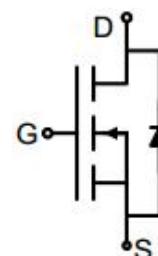
100% ΔV_{ds} TESTED!



SOP-8



pin assignment



Schematic diagram

Maximum ratings, at $T_A = 25^\circ C$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	40	V
V_{GS}	Gate-Source voltage	± 20	V
I_S	Diode continuous forward current	$T_A = 25^\circ C$	A
I_D	Continuous drain current @ $V_{GS}=10V$	$T_A = 25^\circ C$	A
		$T_A = 100^\circ C$	A
I_{DM}	Pulse drain current tested ①	$T_A = 25^\circ C$	A
P_D	Maximum power dissipation	$T_A = 25^\circ C$	W
MSL		Level 3	
T_{STG}, T_J	Storage and junction temperature range	-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead	24	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	40	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise stated)						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	40	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=40\text{V}, V_{\text{GS}}=0\text{V}$	--	--	1	μA
	Zero Gate Voltage Drain Current($T_j=125^\circ\text{C}$)	$V_{\text{DS}}=40\text{V}, V_{\text{GS}}=0\text{V}$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	--	--	± 100	nA
$V_{\text{GS}(\text{TH})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.0		3.0	V
$R_{\text{DS}(\text{ON})}$	Drain-Source On-State Resistance ^②	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=10\text{A}$	--		10	$\text{m}\Omega$
$R_{\text{DS}(\text{ON})}$	Drain-Source On-State Resistance ^②	$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=6\text{A}$	--		17	$\text{m}\Omega$
Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (unless otherwise stated)						
C_{iss}	Input Capacitance	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	1115	1315	1515	pF
C_{oss}	Output Capacitance		85	100	115	pF
C_{rss}	Reverse Transfer Capacitance		65	80	95	pF
R_g	Gate Resistance	f=1MHz	--	1.7	--	Ω
$Q_g(10\text{V})$	Total Gate Charge	$V_{\text{DS}}=20\text{V}, I_{\text{D}}=10\text{A}, V_{\text{GS}}=10\text{V}$	--	22	--	nC
$Q_g(4.5\text{V})$	Total Gate Charge		--	12	--	nC
Q_{gs}	Gate-Source Charge		--	4.5	--	nC
Q_{gd}	Gate-Drain Charge		--	4.2	--	nC
Switching Characteristics						
$t_{\text{d(on)}}$	Turn-on Delay Time	$V_{\text{DD}}=20\text{V}, I_{\text{D}}=10\text{A}, R_{\text{G}}=3.0\Omega, V_{\text{GS}}=10\text{V}$	--	7.5	--	ns
t_r	Turn-on Rise Time		--	3.8	--	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		--	24	--	ns
t_f	Turn-Off Fall Time		--	5.5	--	ns
Source- Drain Diode Characteristics@ $T_j= 25^\circ\text{C}$ (unless otherwise stated)						
V_{SD}	Forward on voltage	$I_{\text{SD}}=10\text{A}, V_{\text{GS}}=0\text{V}$	--	0.8	1.2	V
t_{rr}	Reverse Recovery Time	$T_j=25^\circ\text{C}, I_{\text{SD}}=10\text{A}, V_{\text{GS}}=0\text{V}$ $dI/dt=500\text{A}/\mu\text{s}$	--	8.5	--	ns
Q_{rr}	Reverse Recovery Charge		--	8	--	nC

NOTE:

① Repetitive rating; pulse width limited by max junction temperature.

② Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

Typical Characteristics

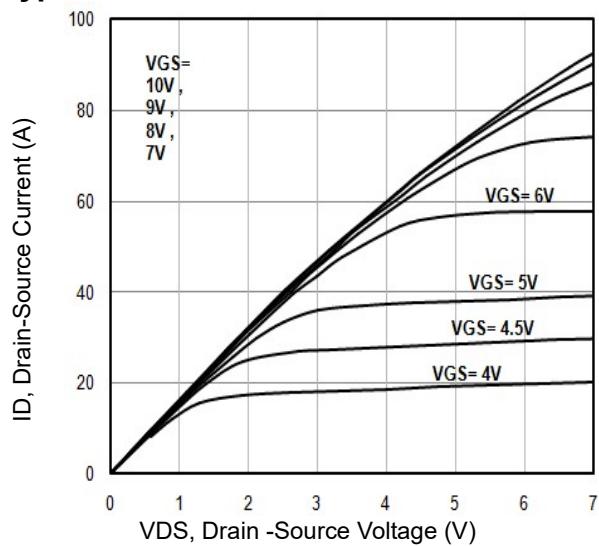


Fig1. Typical Output Characteristics

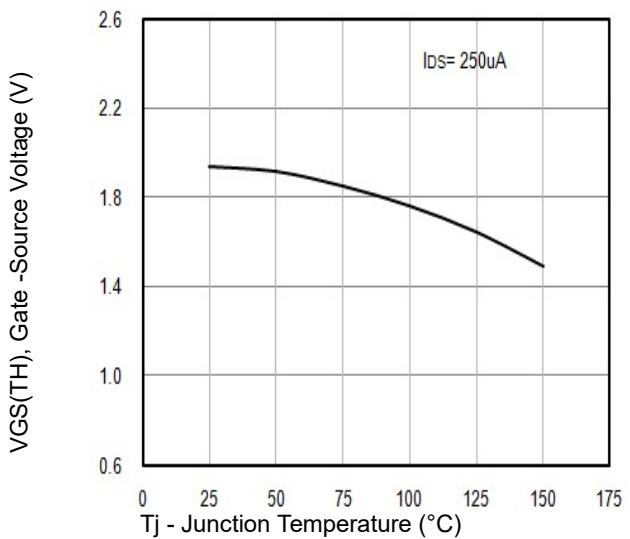


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

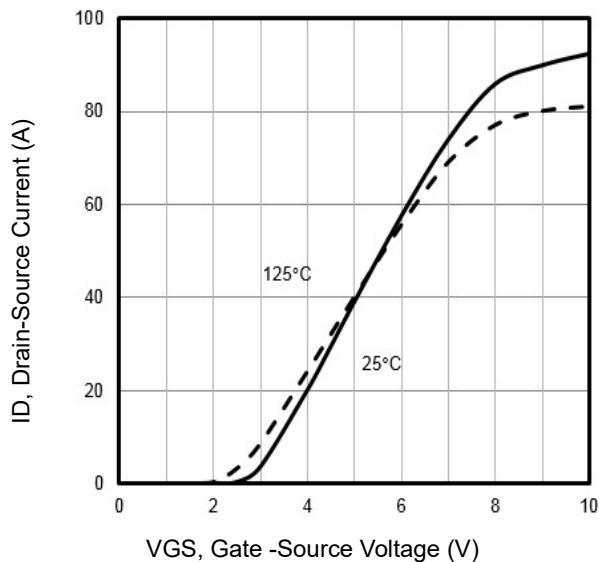


Fig3. Typical Transfer Characteristics

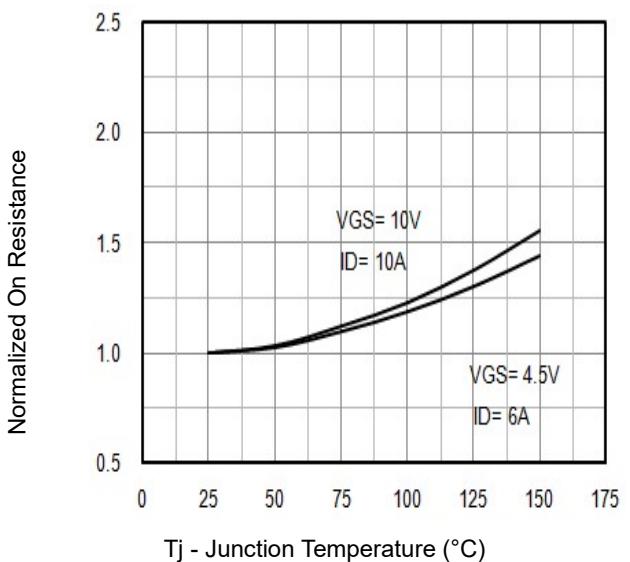


Fig4. Normalized On-Resistance Vs. T_j

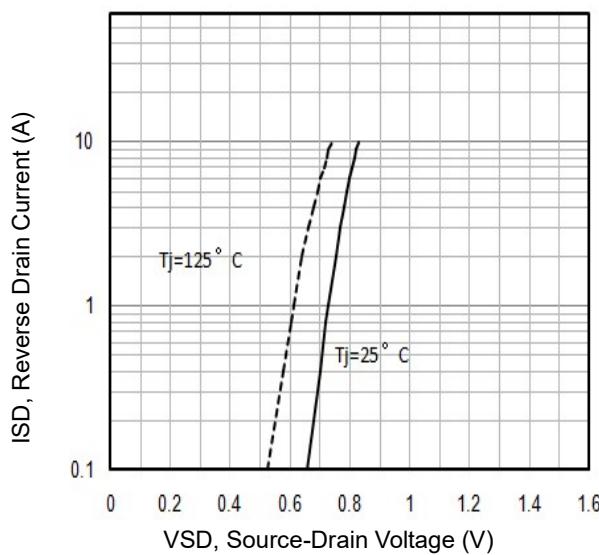


Fig5. Typical Source-Drain Diode Forward Voltage

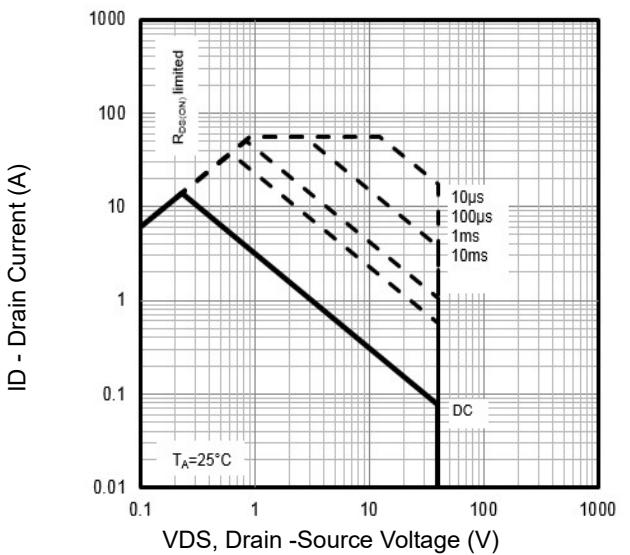


Fig6. Maximum Safe Operating Area

Typical Characteristics

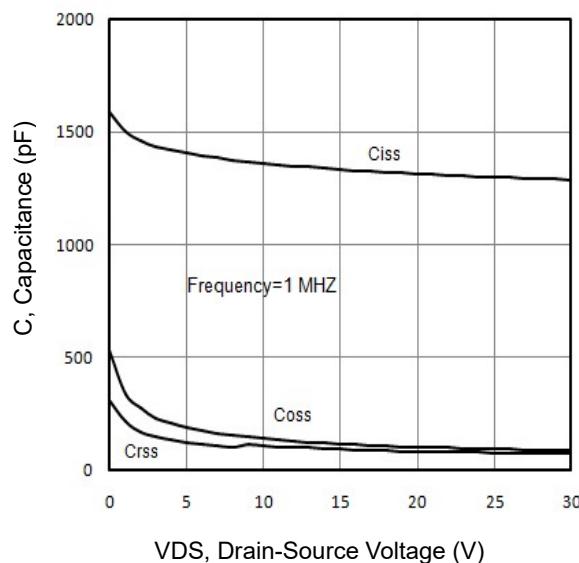


Fig7. Typical Capacitance Vs. Drain-Source Voltage

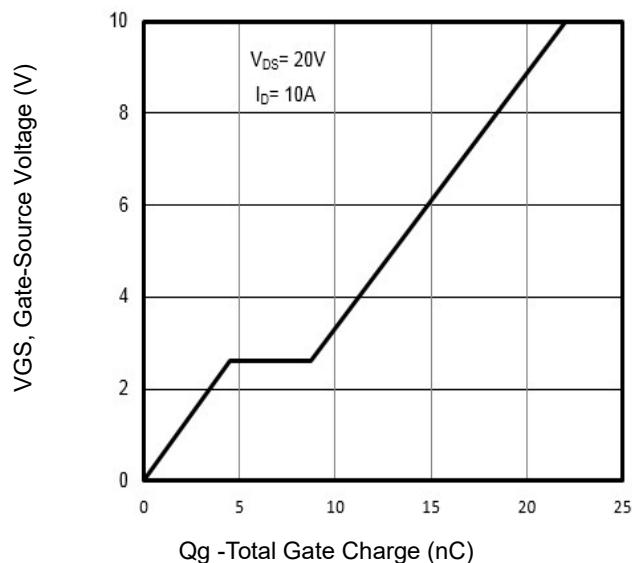


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

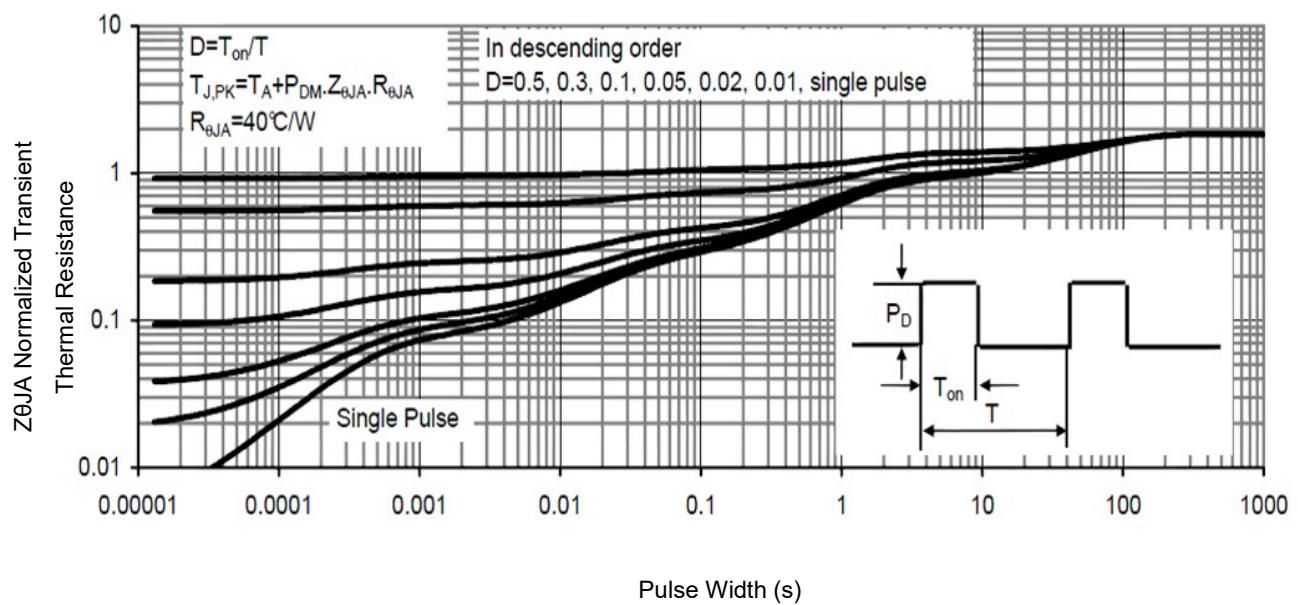


Fig9. Normalized Maximum Transient Thermal Impedance

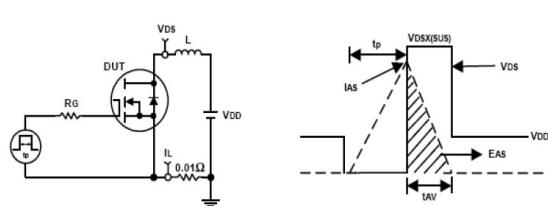


Fig10. Unclamped Inductive Test Circuit and waveforms

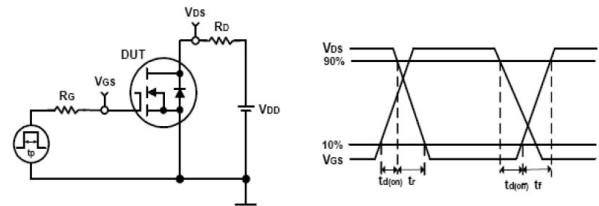


Fig11. Switching Time Test Circuit and waveforms