

## N-Channel Super Trench Power MOSFET

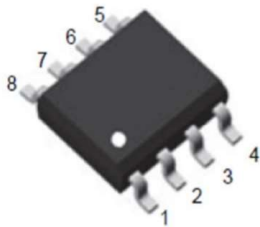
### Features

- $V_{DS} = 150V$ ,  $I_D = 5.1A$
- $R_{DS(ON)} < 55\ m\Omega$  @  $V_{GS} = 10V$
- $R_{DS(ON)} < 65\ m\Omega$  @  $V_{GS} = 4.5V$

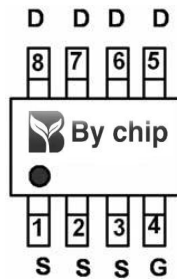
### General Features

- Advanced Trench Technology
- Provide Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free and Green Available

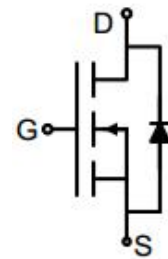
100% UIS TESTED!  
100%  $\Delta V_{ds}$  TESTED!



SOP-8



pin assignment



Schematic diagram

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	150	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V	
Drain Current-Continuous	$I_D$	5.1	A	
Drain Current-Continuous( $T_C = 100^\circ\text{C}$ )	$I_D(100^\circ\text{C})$	3.6	A	
Pulsed Drain Current <sup>(Note 1)</sup>	$I_{DM}$	20	A	
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	60	mJ	
Maximum Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	5	W
		$T_A = 25^\circ\text{C}$	3	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ\text{C}$	

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	41.7	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	25	

**Electrical Characteristics ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

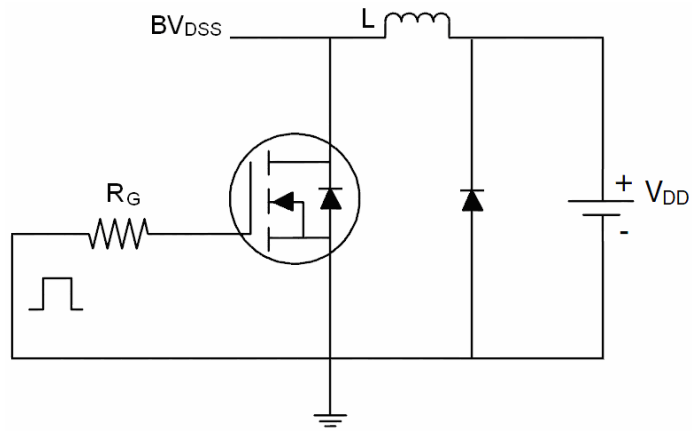
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	150	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=150V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=5.1A$	-		55	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=5.1A$	-	12.5	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	$C_{iss}$	$V_{DS}=75V, V_{GS}=0V,$ $F=1.0MHz$	-	618	850	PF
Output Capacitance	$C_{oss}$		-	81	105	PF
Reverse Transfer Capacitance	$C_{rss}$		-	6.5	9	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=75V, I_D=5.1A$ $V_{GS}=10V, R_G=3\Omega$	-	12.8	14	nS
Turn-on Rise Time	$t_r$		-	1.4	8.5	nS
Turn-Off Delay Time	$t_{d(off)}$		-	12.5	21	nS
Turn-Off Fall Time	$t_f$		-	2.5	8.0	nS
Total Gate Charge	$Q_g$	$V_{DS}=75V, I_D=5.1A,$ $V_{GS}=10V$	-	12.8	18.0	nC
Gate-Source Charge	$Q_{gs}$		-	5		nC
Gate-Drain Charge	$Q_{gd}$		-	3.6		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S=5.1A$	-	-	1.2	V
Diode Forward Current	$I_S$		-	-	5.1	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}, I_F = I_S$	-	58	95	nS
Reverse Recovery Charge	$Q_{rr}$	$di/dt = 100A/\mu s$ (Note 3)	-	69	110	nC

**Notes:**

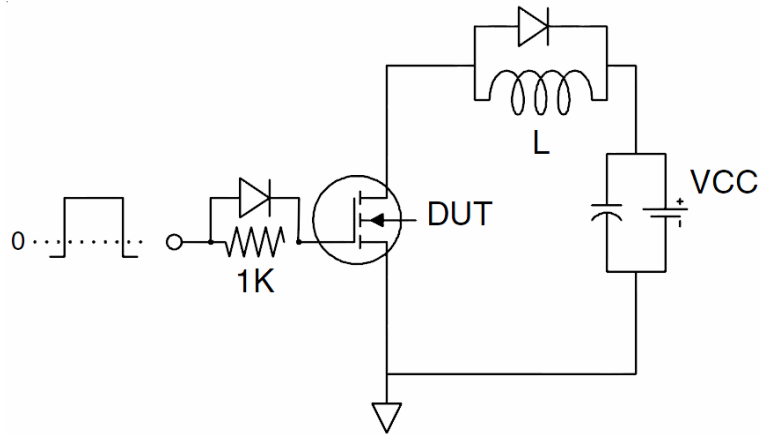
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. The value of  $R_{\theta JA}$  is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^{\circ}\text{C}$ . The value in any given application depends on the user's specific board design.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition :  $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

**Test Circuit**

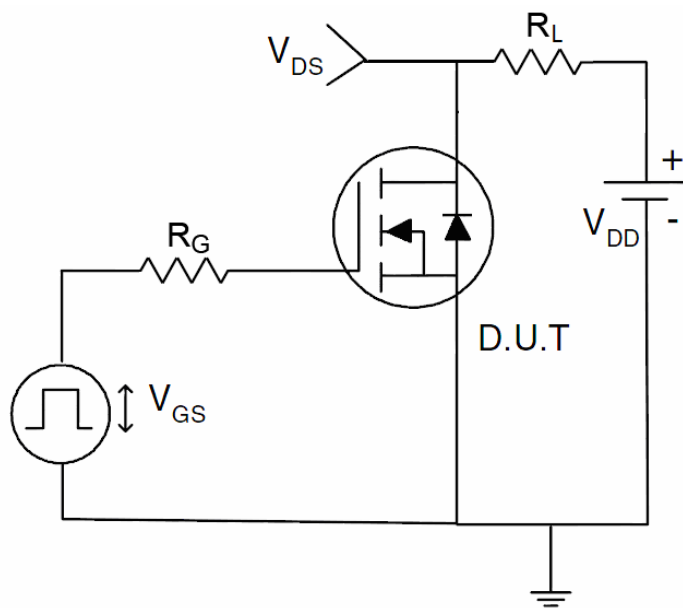
**1)  $E_{AS}$  test Circuit**



**2) Gate charge test Circuit**



**3) Switch Time Test Circuit**



Typical Electrical and Thermal Characteristics (Curves)

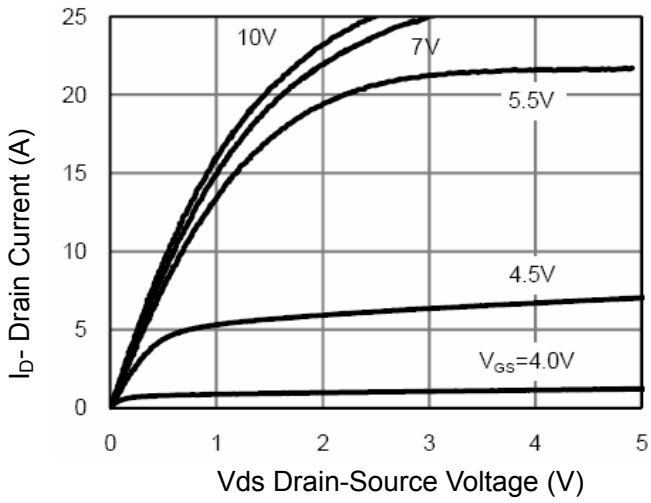


Figure 1 Output Characteristics

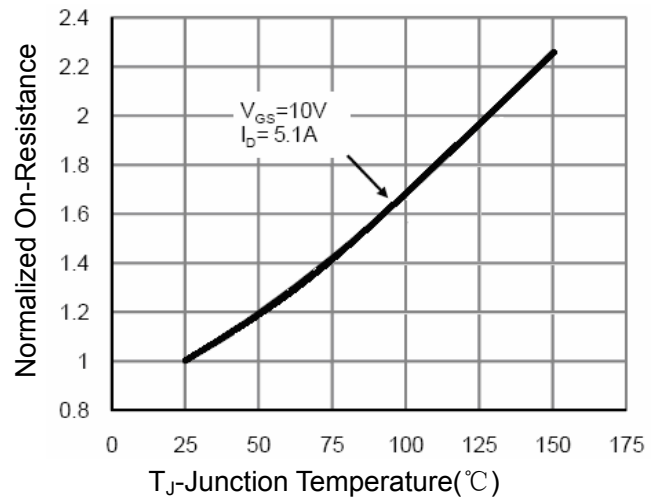


Figure 4  $R_{dson}$ -Junction Temperature

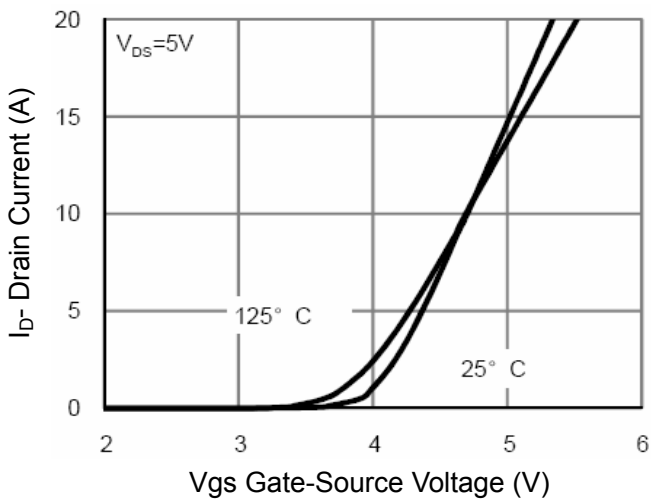


Figure 2 Transfer Characteristics

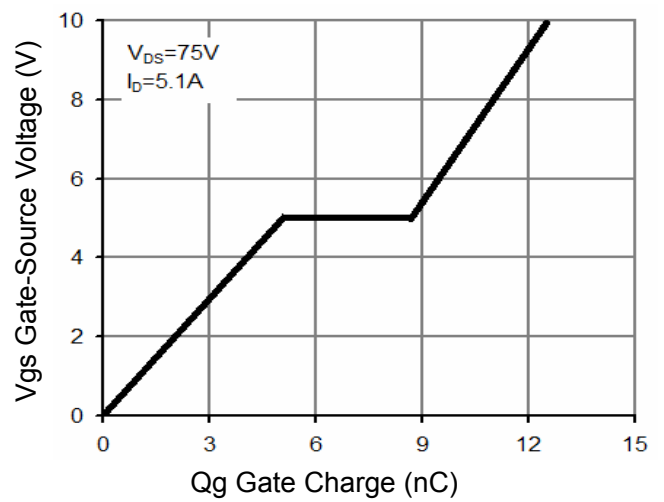


Figure 5 Gate Charge

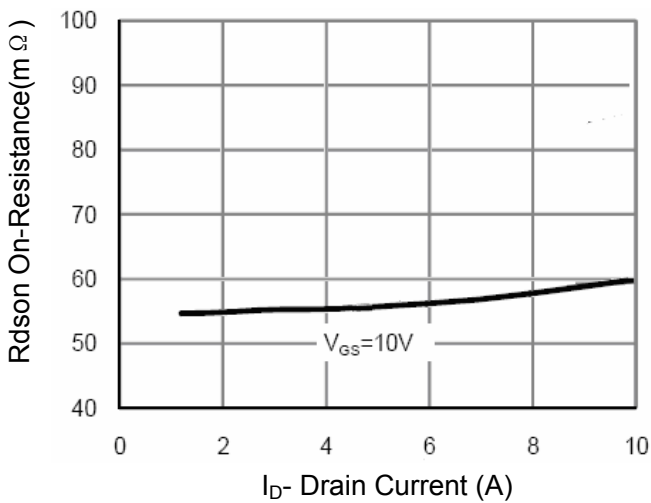


Figure 3  $R_{dson}$ - Drain Current

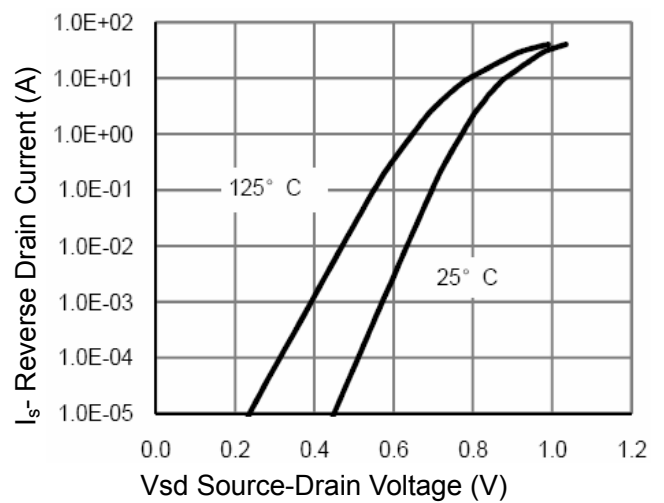


Figure 6 Source- Drain Diode Forward

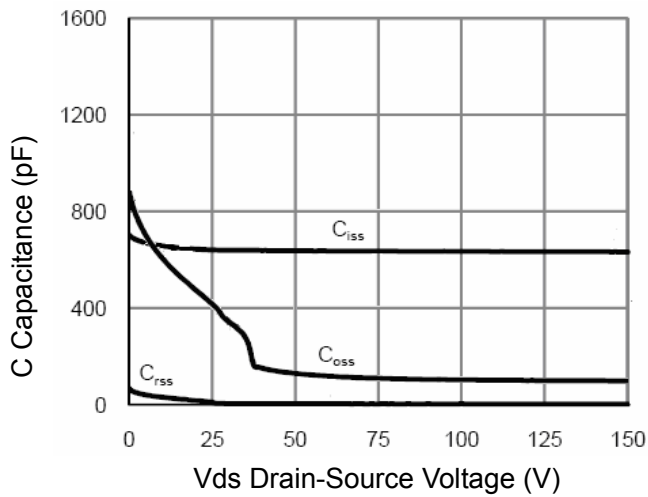


Figure 7 Capacitance vs Vds

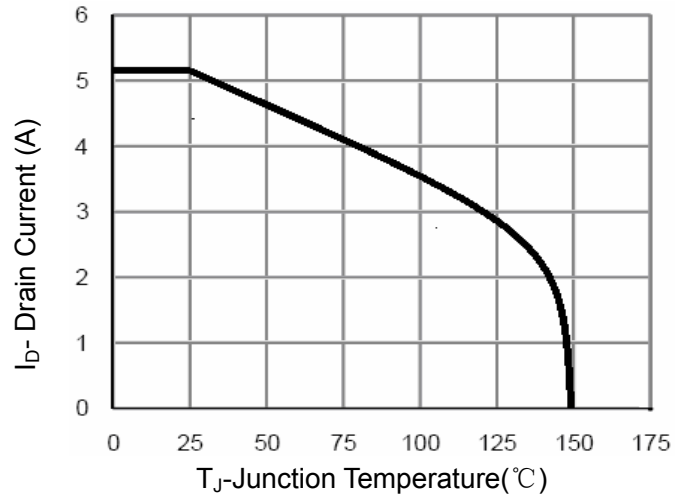


Figure 9 Current De-rating

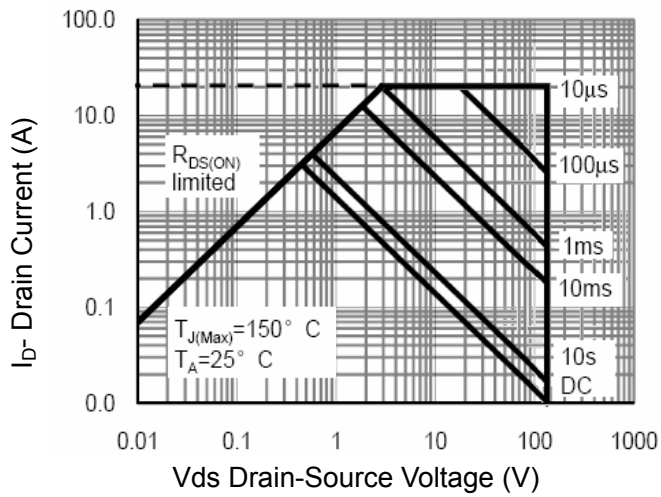


Figure 8 Safe Operation Area

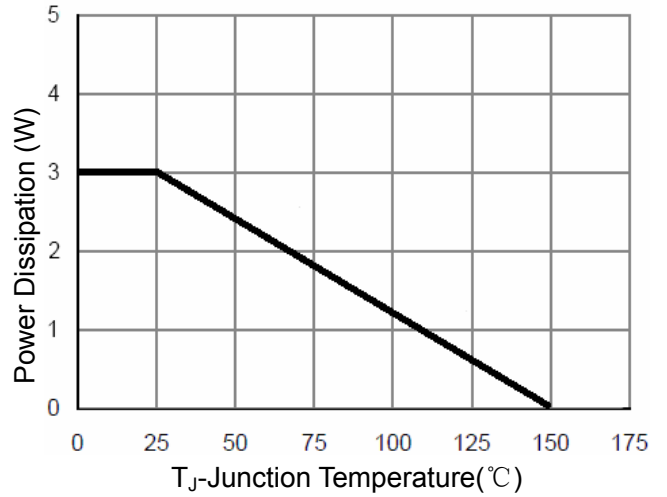


Figure 10 Power De-rating

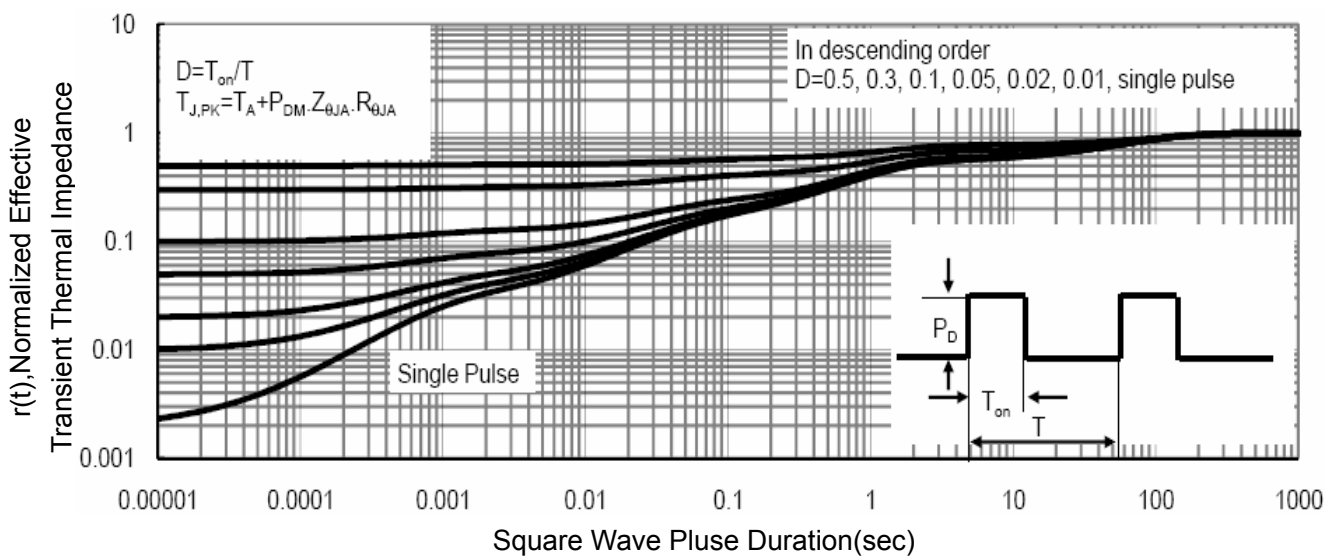


Figure 11 Normalized Maximum Transient Thermal Impedance