

## General Description

The MC14053 is a triple single-pole double-throw (SPDT) analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. Each switch has a digital select input ( $S_n$ ), two independent inputs/ outputs ( $nY_0$  and  $nY_1$ ) and a common input/ output ( $nZ$ ). All three switches share an enable input ( $\bar{E}$ ). A HIGH on  $\bar{E}$  causes all switches into the high-impedance OFF-state, independent of  $S_n$ .

$V_{DD}$  and  $V_{SS}$  are the supply voltage connections for the digital control inputs ( $S_n$  and  $\bar{E}$ ). The  $V_{DD}$  to  $V_{SS}$  range is 3 V to 9 V. The analog inputs/ outputs ( $nY_0$ ,  $nY_1$ , and  $nZ$ ) can swing between  $V_{DD}$  as a positive limit and  $V_{EE}$  as a negative limit.  $V_{DD} - V_{EE}$  may not exceed 9 V. Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input. For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to  $V_{SS}$  (typically ground).  $V_{EE}$  and  $V_{SS}$  are the supply voltage connections for the switches.

## Features

- Wide supply voltage range from 3V to 9V
- Fully static operation
- 5 V and 9V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40° C to +85° C
- Packaging information: SOP16

## Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
MC14053BDR2G	SOP-16	14053	Tape	2500Pcs/Reel

## Block Diagram And Pin Description

### Block Diagram

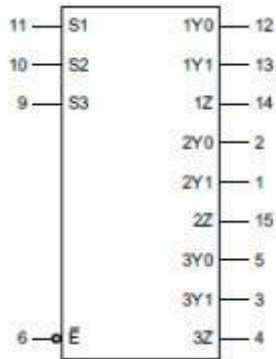


Figure 1 . Logic symbol

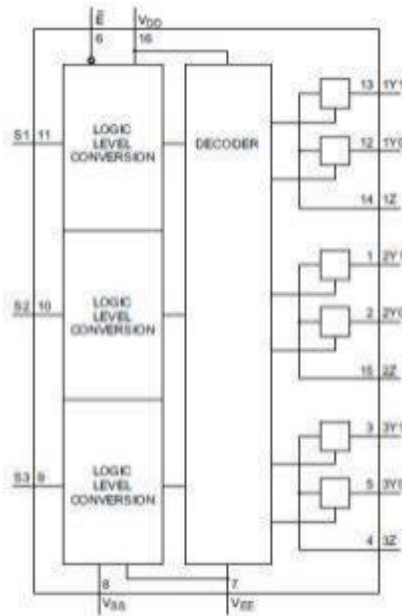


Figure 2 . Functional diagram

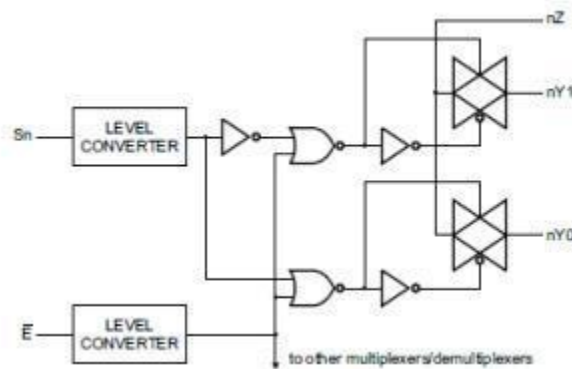


Figure 3 . Logic diagram ( one multiplexer/ demultiplexer)

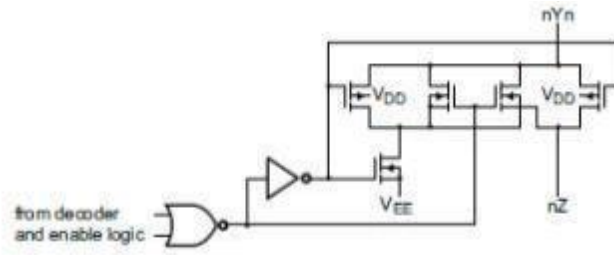
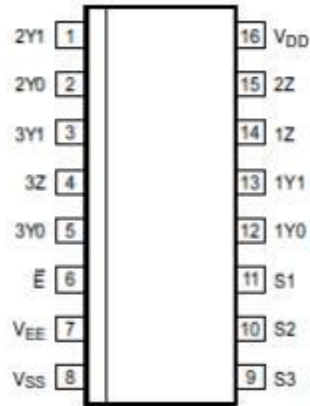


Figure 4 . Schematic diagram ( one switch)

### Pin Configurations



### Pin Description

Pin No.	Pin Name	Description
1	2Y1	independent input or output
2	2Y0	independent input or output
3	3Y1	independent input or output
4	3Z	independent output or input
5	3Y0	independent input or output
6	$\bar{E}$	enable input (active LOW)
7	$V_{EE}$	supply voltage
8	$V_{SS}$	ground (0V)
9	S3	select input
10	S2	select input
11	S1	select input
12	1Y0	independent input or output
13	1Y1	independent input or output
14	1Z	independent output or input
15	2Z	independent output or input
16	$V_{DD}$	supply voltage

### 2.4、 Function Table

Input		Channel ON
$\bar{E}$	$S_n$	
L	L	nY0 to nZ
L	H	nY1 to nZ
H	X	switches off

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

### 3 Electrical Parameter

#### Absolute Maximum Ratings

 (Voltages are referenced to  $V_{SS}$  (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	$V_{DD}$	-	-0.5	+12	V
power supply range	$V_{DD}-V_{EE}$	-	-0.5	+12	V
static current	$I_Q$	$V_{DD}-V_{EE}=12V$	-	2	uA
input voltage	$V_I$	-	-0.5	$V_{DD}+0.5$	V
output high voltage current	$ I_{IH} $	$V_{DD}=5V, V_I=V_{DD}$	-	1	uA
output low voltage current	$ I_{IL} $	$V_{DD}=5V, V_I=0V$	-	1	uA
input and output voltage range	$V_{IO}$	-	$V_{EE}-0.5$	$V_{DD}+0.5$	V
input clamping current	$I_{IK}$	$V_I < -0.5V$ or $V_I > V_{DD}+0.5V$	-	±20	mA
input and output clamp current	$I_{IOK}$	$V_{IO} < V_{EE}-0.5V$ or $V_{IO} > V_{DD}+0.5V$	-	±20	mA
switch conduction current	$I_T$	$V_O = -0.5V$ to $V_{DD}+0.5V$	-	±25	mA
VDD or GND current	$I_{DD}, I_{GND}$	-	-	±50	mA
storage temperature	$T_{stg}$	-	-65	+150	°C
total power dissipation	$P_{tot}$	-	-	500	mW
Soldering temperature	$T_L$	10s	DIP	245	°C
			SOP	250	°C

Note:

 [1] For DIP16 packages: above 70°C the value of  $P_{tot}$  derates linearly with 12mW/K.

 [2] For SOP16 packages: above 70°C the value of  $P_{tot}$  derates linearly with 8mW/K.

 [3] For (T)SSOP16 packages: above 60°C the value of  $P_{tot}$  derates linearly with 5.5mW/K.

#### Recommended Operating Conditions

 ( $T_{amb}=25^\circ C$ ;  $R_L=10k\Omega$ ;  $C_L=50pF$ ;  $\bar{E}=V_{DD}$ ;  $V_{IS}=V_{DD}=5V$ .)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	$V_{DD}$	-	3	5	9	V
ambient temperature	$T_{amb}$	in free air	-40	-	+85	°C
supply voltage	$V_{EE}$	-	-6.0	-	0	V
supply voltage	$V_{DD}-V_{EE}$	-	3.0	-	9.0	V
input voltage	$V_I$	-	0	-	$V_{DD}$	V
input and output voltage	$V_{IO}$	-	$V_{EE}$	-	$V_{DD}$	V
Input rise and fall time	$t_r, t_f$	-	-	-	1000	ns
		-	-	-	500	ns
		-	-	-	400	ns
input capacitance	$C_I$	-	-	-	7.5	pF

**Electrical Characteristics**
**DC Characteristics 1**

 ( $T_{amb}=25^{\circ}C$ , voltages are referenced to  $V_{SS}$  (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		$T_{amb}=25C$			Unit
				Min.	Typ.	Max.	
supply current	$I_{DD}$	$V_I=V_{DD}$ or $V_{SS}, I_O=0A$	$V_{DD}=5V$	-	-	20	$\mu A$
			$V_{DD}=9V$	-	-	40	$\mu A$
HIGH-level input voltage	$V_{IH}$	$ I_O <1\mu A$	$V_{DD}=5V$	3.5	-	-	V
			$V_{DD}=9V$	7.0	-	-	V
LOW-level input voltage	$V_{IL}$	$ I_O <1\mu A$	$V_{DD}=5V$	-	-	1.5	V
			$V_{DD}=9V$	-	-	3.0	V
input leakage current	$I_I$	$V_I=0V$ or $9V, V_{DD}=9V$		-	-	0.3	$\mu A$
3 state output leakage current	$I_{OZ}$	$V_{DD}=9V$	output to $V_{DD}$	-	-	1.6	$\mu A$
			output to $V_{SS}$	-	-	-1.6	$\mu A$
ON resistance (rail)	$R_{ON}$	$V_I=0V$ to $V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5V$	-	350	2500	$\Omega$
			$V_{DD}-V_{EE}=9V$	-	80	245	$\Omega$
		$V_I=0V$	$V_{DD}-V_{EE}=5V$	-	115	340	$\Omega$
			$V_{DD}-V_{EE}=9V$	-	50	160	$\Omega$
		$V_I=V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5V$	-	120	365	$\Omega$
			$V_{DD}-V_{EE}=9V$	-	65	200	$\Omega$
ON resistance mismatch between channels	$\Delta R_{ON}$	$V_I=0V$ to $V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5V$	-	25	-	$\Omega$
			$V_{DD}-V_{EE}=9V$	-	10	-	$\Omega$
OFF-state leakage current	$I_{S(OFF)}$	$V_{SS}=V_{EE}, V_{DD}-V_{EE}=9V$	all channel off; $\bar{E}=V_{DD}$	-	-	1000	nA
			any channel; $\bar{E}=V_{SS}$	-	-	200	nA

Note: On resistance waveform and test circuit see Figure 12 and Figure 13.

**DC Characteristics 2**

 ( $T_{amb}=-40^{\circ}C$  to  $+85^{\circ}C$ , voltages are referenced to  $V_{SS}$  (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		$T_{amb}=-40C$		$T_{amb}=+85C$		Unit
				Min.	Max.	Min.	Max.	
supply current	$I_{DD}$	$V_I=V_{DD}$ or $V_{SS}, I_O=0A$	$V_{DD}=5V$	-	20	-	150	$\mu A$
			$V_{DD}=9V$	-	40	-	300	$\mu A$
HIGH-level input voltage	$V_{IH}$	$ I_O <1\mu A$	$V_{DD}=5V$	3.5	-	3.5	-	V
			$V_{DD}=9V$	7.0	-	7.0	-	V
LOW-level input voltage	$V_{IL}$	$ I_O <1\mu A$	$V_{DD}=5V$	-	1.5	-	1.5	V
			$V_{DD}=9V$	-	3.0	-	3.0	V
input leakage current	$I_I$	$V_I=0V$ or $9V, V_{DD}=9V$		-	0.3	-	1.0	$\mu A$
3 state output leakage current	$I_{OZ}$	$V_{DD}=9V$	output to $V_{DD}$	-	1.6	-	12.0	$\mu A$
			output to $V_{SS}$	-	-1.6	-	-12.0	$\mu A$

### AC Characteristics 1

( $T_{amb}=25^{\circ}C$ ,  $V_{EE}=V_{SS}=0V$ ,  $t_r, t_f \leq 20ns$ ,  $C_L=50pF$ ,  $R_L=10k\Omega$ , unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
HIGH to LOW propagation delay time	$t_{PHL}$	Yn to Z; Z to Yn; see Figure 6	$V_{DD}=5V$	-	10	20	ns
			$V_{DD}=9V$	-	5	10	ns
		Sn to Yn, Z; see Figure 7	$V_{DD}=5V$	-	150	305	ns
			$V_{DD}=9V$	-	65	135	ns
LOW to HIGH propagation delay	$t_{PLH}$	Yn to Z; Z to Yn; see Figure 6	$V_{DD}=5V$	-	10	20	ns
			$V_{DD}=9V$	-	5	10	ns
		Sn to Yn, Z; see Figure 7	$V_{DD}=5V$	-	150	300	ns
			$V_{DD}=9V$	-	75	150	ns
HIGH to OFF-state propagation delay	$t_{PHZ}$	$\bar{E}$ to Yn, Z; see Figure 8	$V_{DD}=5V$	-	95	190	ns
			$V_{DD}=9V$	-	90	180	ns
LOW to OFF-state propagation delay	$t_{PLZ}$	$\bar{E}$ to Yn, Z; see Figure 8	$V_{DD}=5V$	-	100	205	ns
			$V_{DD}=9V$	-	90	180	ns
OFF-state to HIGH propagation delay	$t_{PZH}$	$\bar{E}$ to Yn, Z; see Figure 8	$V_{DD}=5V$	-	130	260	ns
			$V_{DD}=9V$	-	55	115	ns
OFF-state to LOW propagation delay	$t_{PZL}$	$\bar{E}$ to Yn, Z; see Figure 8	$V_{DD}=5V$	-	120	240	ns
			$V_{DD}=9V$	-	50	100	ns

### AC Characteristics 2

( $T_{amb}=25^{\circ}C$ ,  $V_{EE}=V_{SS}=0V$ ,  $V_i=0.5V_{DD}$  (p-p), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Square wave distortion	$d_{sin}$	see Figure 9; $R_L=10k\Omega$ ; $C_L=15pF$ ; channel ON; $f_i=1kHz$	$V_{DD}=5V$	0.25	-	-	%
			$V_{DD}=9V$	0.04	-	-	%
any two channel crosstalk	$f_{ct}$	$V_{DD}=9V$ , see note2	1	-	-	MHz	
crosstalk voltage ( $\bar{E}$ to Sn or Yn to Z)	$V_{ct}$	see Figure 10; $R_L=10k\Omega$ ; $C_L=15pF$ ; $\bar{E}$ or Sn= $V_{DD}$ (square-wave)	50	-	-	mV	
OFF frequency	$f_{OFF}$	$V_{DD}=9V$ , see note3	1	-	-	MHz	
conduction frequency	$f_{ON}$	$V_{DD}=5V$ , see note4	13	-	-	MHz	
		$V_{DD}=9V$ , see note4	40	-	-	MHz	

Note:

- [1]  $f_i$  is biased at  $0.5V_{DD}$ ;  $V_i=0.5V_{DD}$  (p-p).
- [2]  $R_L=1k\Omega$ ;  $20\log V_{os}/V_{is}=-50dB$ , see Figure 11.
- [3]  $R_L=1k\Omega$ ;  $C_L=5pF$ , channel off,  $20\log V_{os}/V_{is}=-50dB$ , see Figure 9.
- [4]  $R_L=1k\Omega$ ;  $C_L=5pF$ , channel on,  $20\log V_{os}/V_{is}=-3dB$ , see Figure 9.

## Testing Circuit

### 4.1、 AC Testing Circuit 1

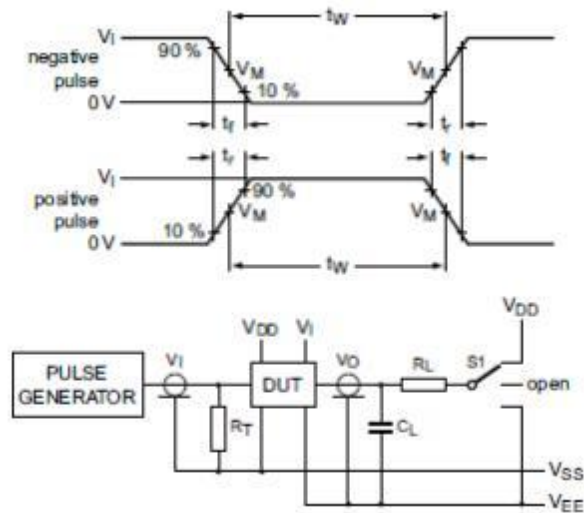


Figure 5. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

$C_L$ =Load capacitance including jig and probe capacitance.

$R_T$ =Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.  $R_L$ =Load resistance.

### AC Testing Waveforms

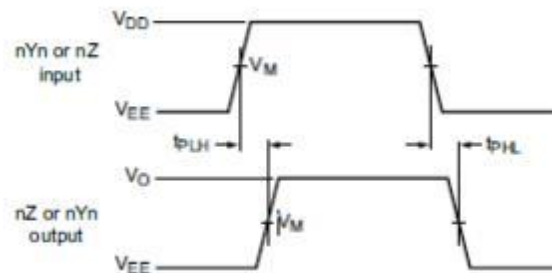


Figure 6. nYn, nZ to nZ, nYn propagation delays

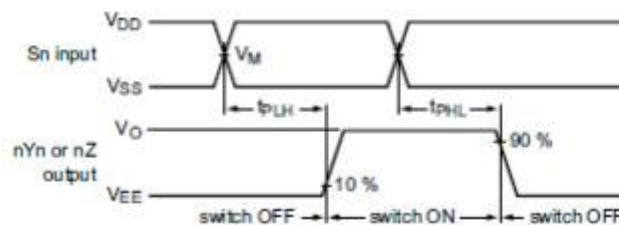


Figure 7.  $S_n$  to nYn, nZ propagation delays

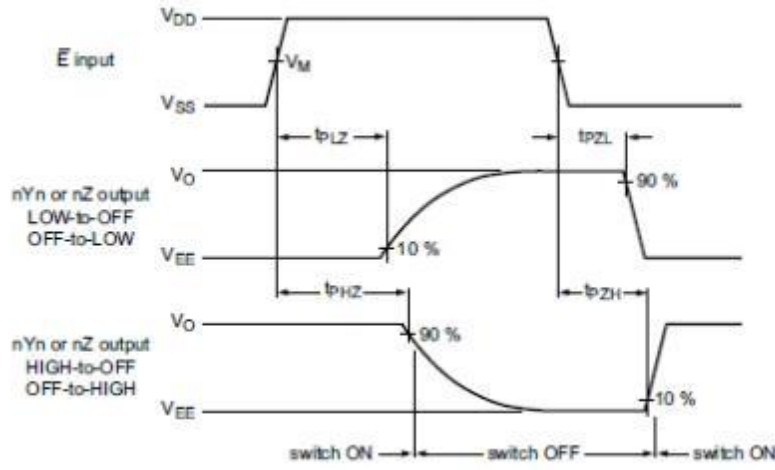


Figure 8. Enable and disable times

AC Testing Circuit 2

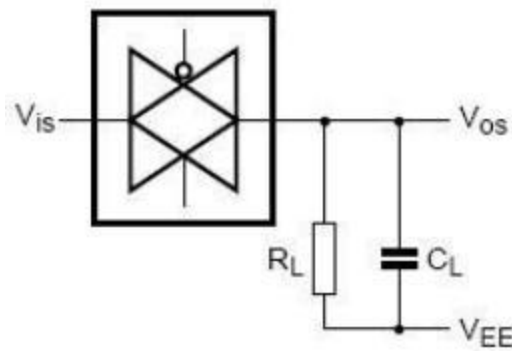


Figure 9. Square wave distortion degree of cut-off frequency and conduction frequency test pattern

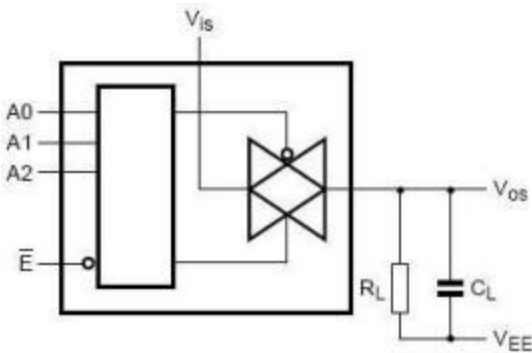


Figure 10. Crosstalk logical input/output test

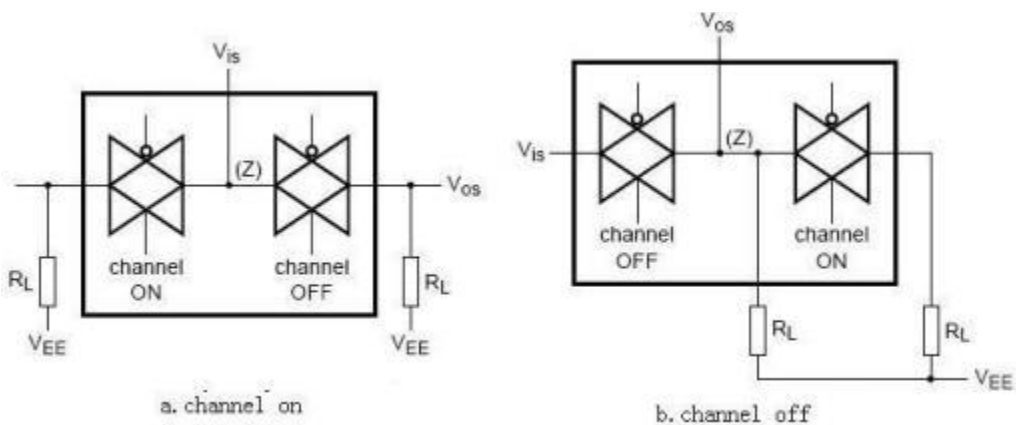


Figure 11. Inter channel Crosstalk



**On Resistance Waveform And Test Circuit**

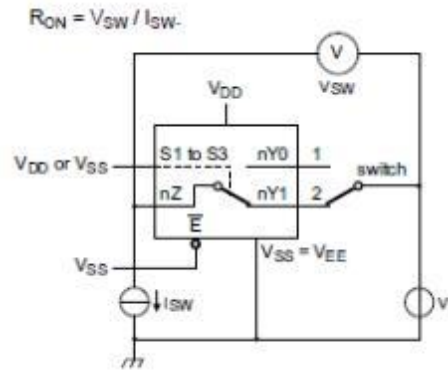


Figure 12. Test circuit for measuring  $R_{ON}$

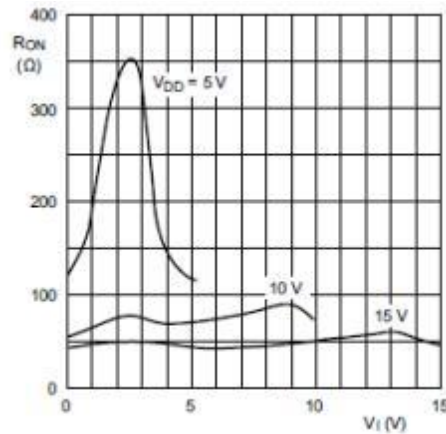


Figure 13. Typical  $R_{ON}$  as a function of input voltage

**Measurement Points**

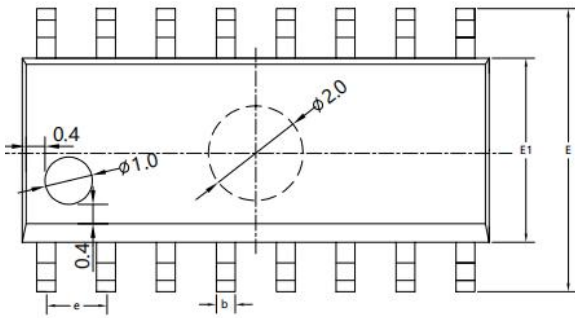
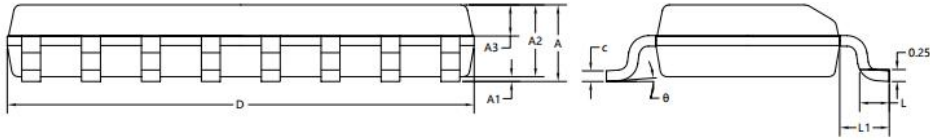
Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
3V to 9V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

**Test Data**

Test	Input		Load		Switch
	$V_{is}$	$t_r, t_f$	$C_L$	$R_L$	
$t_{PHL}$	$V_{EE}$	20ns	50pF	10k $\Omega$	$V_{DD}$
$t_{PLH}$	$V_{DD}$	20ns	50pF	10k $\Omega$	$V_{EE}$
$t_{PZH}, t_{PHZ}$	$V_{DD}$	20ns	50pF	10k $\Omega$	$V_{EE}$
$t_{PZL}, t_{PLZ}$	$V_{EE}$	20ns	50pF	10k $\Omega$	$V_{DD}$
others	pulse	20ns	50pF	10k $\Omega$	open

**Package Information**

**SOP16**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05BSC		
θ	0°	4°	8°

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